On-Chip ESD Protection Design With Substrate-Triggered Technique for Mixed-Voltage I/O Circuits in Subquarter-Micrometer CMOS Process

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***Abstract*—A new electrostatic discharge (ESD) protection design, by using the substrate-triggered stacked-nMOS device, is proposed to protect the mixed-voltage I/O circuits of CMOS ICs. The substrate-triggered technique is applied to lower the trigger voltage of the stacked-nMOS device to ensure effective ESD protection for the mixed-voltage I/O circuits. The proposed ESD protection circuit with the substrate-triggered technique is fully compatible to general CMOS process without causing the gate-oxide reliability problem. Without using the thick gate oxide, the new proposed design has been fabricated and verified for 2.5/3.3-V tolerant mixed-voltage I/O circuit in a 0.25-μm salicided CMOS process. The experimental results have confirmed that the human-body-model ESD level of the mixed-voltage I/O buffers can be successfully improved from the original 3.4 to 5.6 kV by using this new proposed ESD protection circuit.**

***Index Terms*—Electrostatic discharge (ESD), ESD protection circuit, mixed-voltage I/O circuits, substrate-triggered technique.**

I. Introduction

TO IMPROVE circuit operating speed and performance, the device dimensions of MOSFET had been shrunk in the advanced deep-submicrometer integrated circuits. In order to follow constant-field scaling requirement and to reduce power consumption, the power supply voltages in CMOS ICs have been also scaled downwards. So, most microelectronic systems require the interfacing of semiconductor chips or subsystems with different internal power supply voltages. With the mix of power supply voltages, chip-to-chip interface I/O circuits must be designed to avoid electrical overstress across the gate oxide [1], to avoid hot-carrier degradation [2] on the output devices, and to prevent undesirable leakage current paths between the chips [3], [4]. For example, a 3.3-V I/O interface is generally required for ICs realized in CMOS processes with a normal internal power-supply voltage of 2.5 or 1.8 V. The traditional CMOS I/O buffer with $V_{\rm DD}$ of 2.5 V is shown in Fig. 1(a) with output and input stages. When an external 3.3-V signal is applied to the I/O pad, the channel of the output pMOS and the parasitic drain-to-well junction diode in the output pMOS cause the leakage current paths from the I/O pad to $V_{\rm DD}$, as the dashed lines shown in Fig. 1(a). Moreover, the gate oxides of the output nMOS, the gate-grounded nMOS for input electrostatic discharge (ESD) protection, and the input inverter stage are overstressed by the 3.3-V input signal.

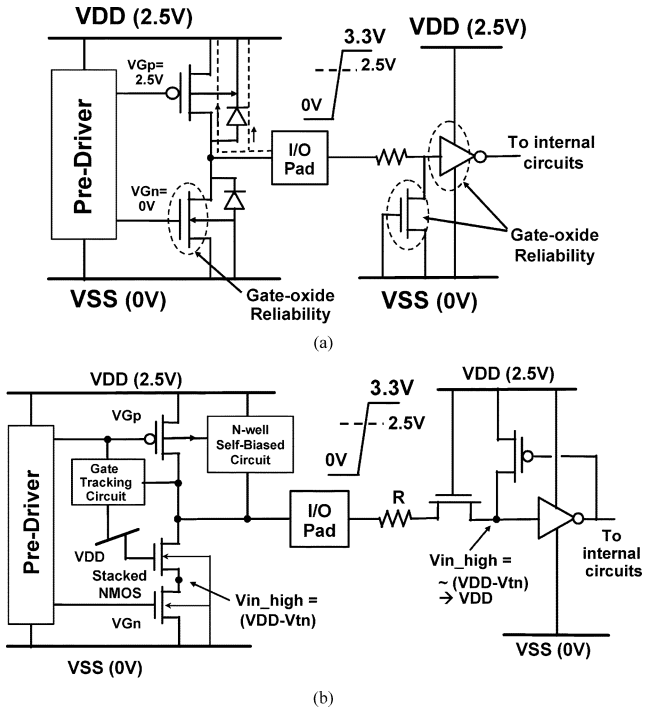

Fig. 1. Typical circuit diagrams for (a) the traditional CMOS I/O buffer, and (b) the mixed-voltage I/O buffer with the stacked-nMOS and the N-well self-biased pMOS.

To solve the gate-oxide reliability issue without using the additional thick gate oxide process (or referred to as dual-gate oxide in some CMOS processes [5], [6]), the stacked-MOS configuration had been widely used in the mixed-voltage I/O buffers [7]–[12], and in the power-rail ESD clamp circuits [13]. The typical 2.5/3.3 V-tolerant mixed-voltage I/O circuit is shown in Fig. 1(b) [8]. The pull-up pMOS, connected from the I/O pad to the $V_{\rm DD}$ power line, has the self-biased circuits for tracking its gate and n-well voltages, when the 3.3-V input signals enter the I/O pad. The maximum output voltage level of such a 2.5/3.3 V-tolerant I/O buffer is only $V_{\rm DD}$ (2.5 V).

ESD stresses on an I/O pad have four pin-combination modes: positive-to-$V_{\rm SS}$ (PS-mode), negative-to-$V_{\rm SS}$ (NS-mode), positive-to-$V_{\rm DD}$ (PD-mode), and negative-to-$V_{\rm DD}$ (ND-mode) ESD

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zapping conditions [14], [15]. To achieve high enough ESD robustness of the CMOS output buffer, the CMOS buffer is generally drawn with larger device dimensions and a wider spacing from the drain contact to the poly gate, which often occupy a larger layout area in the I/O cell. The $V_{\rm DD}$-to-$V_{\rm SS}$ ESD clamp circuits across the power lines of CMOS ICs had been reported to effectively increase ESD robustness of CMOS I/O buffers [16]–[18]. Under the positive-to-$V_{\rm SS}$ ESD stress condition, the ESD current can be discharged through the parasitic diode of pMOS and the $V_{\rm DD}$-to-$V_{\rm SS}$ ESD camp circuit to ground. Therefore, the traditional CMOS output buffer cooperating with the $V_{\rm DD}$-to-$V_{\rm SS}$ ESD clamp circuit can sustain a much higher ESD stress [18]. But, due to the leakage current issue in the mixed-voltage I/O buffer, there is no parasitic diode connected from the I/O pad to $V_{\rm DD}$ power line in the mixed-voltage I/O buffer. Because of the limitation of placing a diode from the pad to $V_{\rm DD}$ in the mixed-voltage I/O circuits, the positive-to-$V_{\rm SS}$ ESD voltage zapping on the I/O pad cannot be discharged from the pad to $V_{\rm DD}$ power line, and cannot be discharged through the additional power-rail ($V_{\rm DD}$-to-$V_{\rm SS}$) ESD clamp circuit. Such positive-to-$V_{\rm SS}$ ESD current on the I/O pad is discharged through the stacked-nMOS in the snapback breakdown condition. However, the nMOS in stacked configuration has a higher trigger voltage (V_{t1}) and a higher snapback holding voltage ($V_{\rm sb}$), but a lower secondary breakdown current (I_{t2}), as compared to the single nMOS [19]. Therefore, such mixed-voltage I/O circuits with stacked nMOS often have much lower ESD levels under the positive-to-$V_{\rm SS}$ ESD stress condition, as compared to the I/O circuits with a single nMOS [19], [20]. In addition, without the parasitic diode connected from the I/O pad to $V_{\rm DD}$ power line, the mixed-voltage I/O circuit also has a lower ESD level under the positive-to-$V_{\rm DD}$ ESD stress condition. Therefore, ESD protection design for the mixed-voltage I/O circuits is mainly focused on improving the ESD level under the positive ESD stress conditions.

To improve the turn-on uniformity among the multiple fingers of CMOS output buffer, the substrate-triggered design [21]–[24] had been reported to increase ESD robustness of the large-device-dimension nMOS. However, in the literature, the substrate-triggered technique was never reported to improve ESD robustness of the stacked-nMOS in the mixed-voltage I/O circuits. In this paper, the substrate-triggered stacked-nMOS device, which combines the substrate-triggered technique with the stacked-nMOS device, is proposed to protect the mixed-voltage I/O circuits of CMOS ICs. The proposed ESD protection circuit with the substrate-triggered technique is fully compatible to general CMOS process without causing the gate-oxide reliability problem. Without using the thick gate oxide, the new proposed design has been fabricated and verified for 2.5/3.3 V tolerant mixed-voltage I/O circuit in a 0.25-μm salicided CMOS process [25].

II. Stacked-nMOS With Substrate-Triggered Technique

A. Stacked-nMOS Device

The finger-type layout pattern and the corresponding cross-sectional view of stacked-nMOS structure in the mixed-voltage I/O circuit are shown in Fig. 2, which includes one pair of nMOS transistors connected in a stack configuration. The stacked-nMOS device is used as both of the pull-down device and ESD protection device for the I/O circuit. The nMOS transistor pair includes a first transistor (top nMOS transistor), having a drain connected to an I/O pad, and a gate (V_{G1}) connected to the $V_{\rm DD}$ power supply. A second nMOS transistor (bottom nMOS transistor) of the nMOS transistor pair is merged into the same active area of the first transistor, having a gate (V_{G2}) connected to the pre-driver of the mixed-voltage I/O circuit. The drain of the bottom nMOS transistor and the source of the top nMOS transistor are constructed together by sharing the common N+ diffusion region.

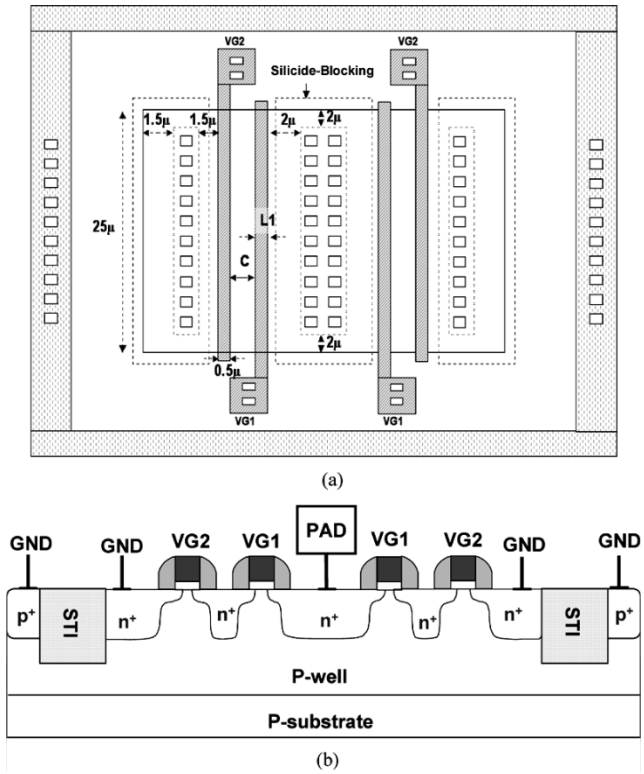

Fig. 2. (a) Finger-type layout pattern, and (b) the corresponding cross-sectional view, of the stacked-nMOS device for mixed-voltage I/O circuit in a p-substrate CMOS process.

The independent control of the top and bottom gates of stacked-nMOS device allows the device to meet reliability limits during normal circuit operation. The voltage (V_{G1}) of the top nMOS is biased at the $V_{\rm DD}$ voltage (e.g., 2.5 V in a 2.5/3.3 V mixed-voltage I/O interface). The voltage (V_{G2}) of the bottom nMOS is at $V_{\rm SS}$ provided by the predrive to avoid leakage current through the stacked-nMOS structure, when the I/O circuit has a high-voltage input signal. With a high-voltage input signal at the pad (e.g., 3.3 V in a 2.5/3.3 V mixed-voltage I/O interface), the shared common diffusion region has approximately a voltage level of $V_{\rm DD}$-$V_{\rm th}$ ($\sim$ 1.9 V). The $V_{\rm th}$ ($\sim$ 0.6 V) is the threshold voltage of nMOS device. Therefore, the stacked-nMOS can be operated within the safe range for both dielectric and hot carrier reliability limitations.

Under the positive-to-$V_{\rm SS}$ ESD stress condition, the stacked-nMOS is operated in snapback breakdown, with

the bipolar effect taking place between the drain of the top nMOS and the source of the bottom nMOS. These two diffusions act as bipolar emitter and collector, respectively. Their spacing determines the base width and turn-on efficiency of the lateral bipolar transistor. The snapback mechanism of stacked-nMOS for conducting large amounts of ESD current involves both avalanche breakdown and turn-on of the parasitic lateral bipolar transistor. The hole current ($I_{\rm sub}$) generated from drain avalanche breakdown, drifting through the effective substrate resistance ($R_{\rm sub}$) to ground, may elevate the substrate potential ($V_{\rm sub}$) of the emitter–base junction in the lateral bipolar transistor. The voltage level, where the local substrate potential is elevated, depends on the relative proximity to the avalanching junction. When the emitter–base junction of bipolar transistor begins to weakly forward bias due to the increase of local substrate potential, additional electron current through the bipolar device is acted as "seed current" to drive a significant increase in the multiplication rate and avalanche current generation at the collector–base junction of the lateral bipolar transistor. Therefore, a "snapback" is seen, and the lateral bipolar transistor enters strong bipolar conduction to discharge ESD current.

B. Substrate-Triggered Stacked-nMOS Device

The snapback operation of stacked-nMOS devices depends on the substrate current ($I_{\rm sub}$), which is created at the reverse-biased drain/substrate junction, to forward bias the source/substrate junction. Hence, the substrate resistance ($R_{\rm sub}$) and substrate current ($I_{\rm sub}$) are the important design parameters for ESD protection [26], [27]. However, the substrate-triggered technique can be used to generate the substrate current. With the substrate-triggered current, the trigger voltage (V_{t1}) of the stacked-nMOS device in mixed-voltage I/O circuits can be reduced for more effective ESD protection. In this paper, the substrate-triggered stacked-nMOS device, which combines the substrate-triggered technique with the stacked-nMOS device, is proposed to protect the mixed-voltage I/O circuits of CMOS ICs.

The finger-type layout pattern and the corresponding cross-sectional view of the new proposed substrate-triggered stacked-nMOS device are shown in Fig. 3(a) and (b), respectively. As shown in Fig. 3, a P+ diffusion is inserted into the center region of stacked-nMOS device as the substrate-triggered point. The trigger current ($I_{\rm trig}$) is provided by the special ESD detection circuit. An N-well structure is further diffused under the source region of this device to form a higher equivalent substrate resistance to improve turn-on efficiency of the parasitic lateral bipolar transistor in the stacked-nMOS device.

C. ESD Protection Circuit

The ESD protection design, which includes the substrate-triggered stacked-nMOS device and the substrate-triggered circuit for the mixed-voltage I/O circuits, is shown in Fig. 4. The substrate-triggered circuit is composed of the diode string, a pMOS device (P1), and an nMOS device (N1), to provide the substrate current for triggering on the parasitic lateral bipolar transistor in the stacked-nMOS device, while the ESD voltage is

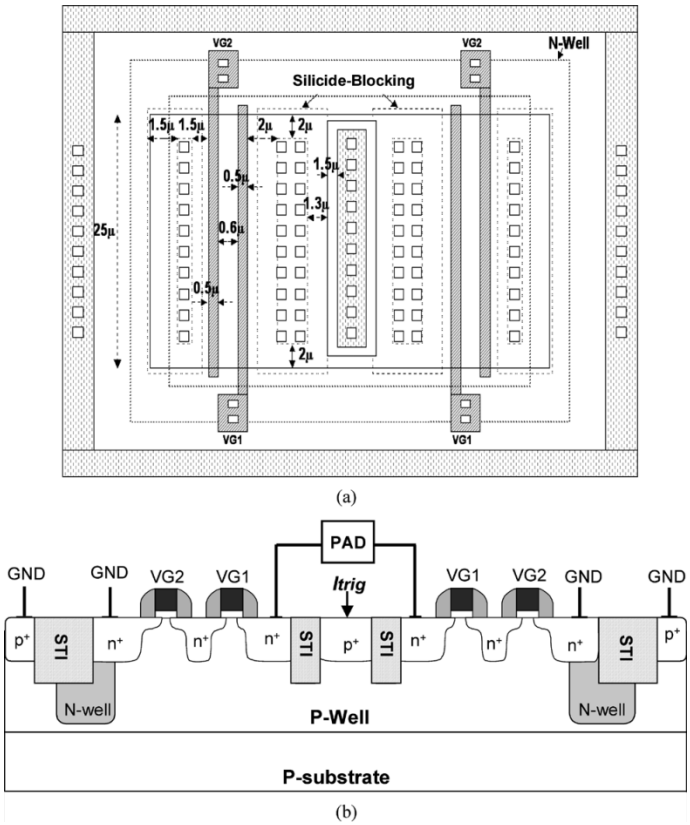

Fig. 3. (a) Finger-type layout pattern, and (b) the corresponding cross-sectional view, of the substrate-triggered stacked-nMOS device for mixed-voltage I/O circuit in a p-substrate CMOS process.

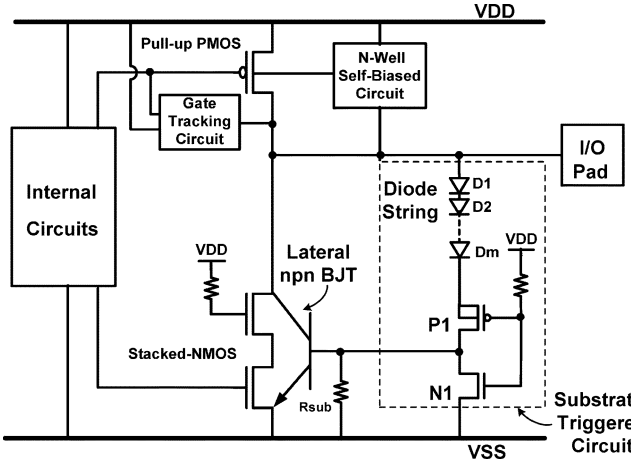

Fig. 4. Schematic circuit diagram of the substrate-triggered stacked-nMOS device with substrate-triggered circuit for the mixed-voltage I/O circuits.

applied on the I/O pad. The anode of the diode string in the substrate-triggered circuit and the collector of the parasitic bipolar transistor in the stacked-nMOS device are connected to I/O pad. The cathode of the diode string is connected to the source of P1. The emitter (the base) of the lateral bipolar transistor is connected to the $V_{\rm SS}$ power line (the drain of P1). The nMOS (N1) is connected between the base of the lateral bipolar transistor and the $V_{\rm SS}$ power line. The gates of P1 and N1 are connected together to the $V_{\rm DD}$ power line through a resistor. The resistor is realized by an N+ diffusion with a parasitic N+/P-sub diode to

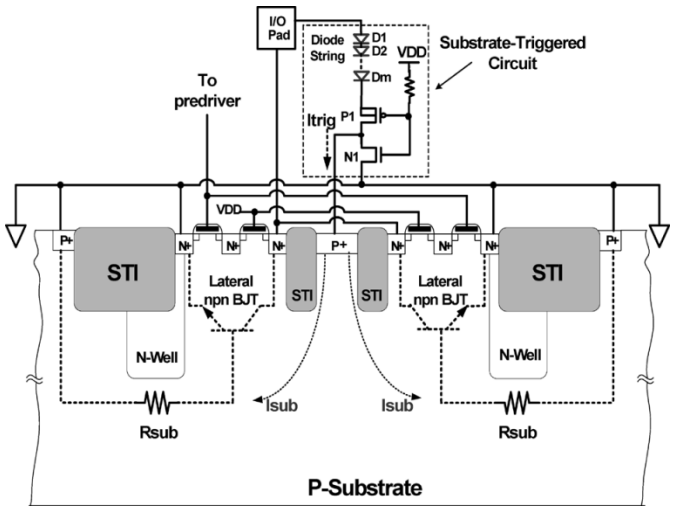

Fig. 5. Cross-sectional view of the substrate-triggered stacked-nMOS device with substrate-triggered circuit for the mixed-voltage I/O circuits.

avoid the antenna effect during the CMOS process fabrication. The diode string including in the substrate-triggered circuit is composed of individual diodes formed by using P+ diffusion in the separated n-well structure. The total voltage drop across the diode string can be expressed as [28]

$$V_{\text{string}}(I) = mV_D(I) - nV_T\left[\frac{m(m-1)}{2}\right] \times \ell n(\beta+1) \quad (1)$$

where

$V_{\text{string}}(I)$ = total voltage drop across the m diodes,
m = the number of diodes in the diode string,
n = ideality factor, and
β = the beta gain of the parasitic vertical pnp bipolar transistor in the diode structure.

During the ESD stress condition, the pMOS (P1) device is used in conjunction with the diode string to provide the substrate current to trigger the parasitic lateral bipolar transistor in the stacked-nMOS device. Once the lateral bipolar transistor in the stacked-nMOS device has been turned on, the ESD current is discharged from the I/O pad to V_{SS}.

D. Operating Principles

Fig. 5 shows the cross-sectional view of the substrate-triggered stacked-nMOS device with the substrate-triggered circuit for protecting mixed-voltage I/O circuits. In the normal circuit operating condition, the substrate-triggered circuit should remain in a nonconductive state, so that it does not interfere with the voltage levels on the I/O pad. For the 2.5/3.3 V mixed-voltage IC application, 3.3 V tolerance was desired for normal circuit operation with a 2.5-V V_{DD} supply in the chip. The turn-on voltage of the substrate-triggered circuit roughly equals to $V_{\text{pad}} \geqq V_{\text{string}}(I) + |V_{\text{tp}}| + V_{\text{DD}}$, where the V_{tp} is the threshold voltage of the pMOS (P1). The turn-on voltage can be adjusted by varying the numbers of the diodes in the diode string. To satisfy the requirement in the 2.5/3.3 V mixed-voltage application, the number of the diodes in the diode string should be adjusted to let the turn-on voltage greater than 3.3 V. When the I/O pad is applied with a high input voltage of 3.3 V, pMOS (P1) is still kept off, and the local substrate of the stacked-nMOS is biased at V_{SS} by the turned-on nMOS (N1). With the diode string to block the 3.3 V input voltage on the I/O pad, the pMOS (P1) with thin gate oxide has no gate-oxide reliability issue during the normal circuit operating condition.

The choice of a particular diode string is also determined by the specified pin leakage current at a fgiven temperature. If a lower input leakage is desired, the numbers of the diodes in the diode string should be increased. Since the diode string is not the main ESD current discharge path, its perimeter can be adjusted with less impact on ESD performance. The leakage current problem of the diode string comes from the parasitic vertical pnp bipolar transistor of each diode formed by the P+ diffusion in an n-well. The pMOS (P1) in conjunction with a diode string is used to reduce the leakage current at the I/O pad in the normal operating condition. Moreover, the nMOS (N1) with its gate biased at V_{DD} is always turned on to bypass any leakage current, which may trigger on the lateral npn bipolar transistor in the normal circuit operating condition.

Under the positive-to-V_{SS} ESD stress condition, the gate of the pMOS (P1) has an initial voltage level of $\sim$ 0 V, while the V_{SS} pin is grounded but the V_{DD} pin is floating. The substrate-triggered circuit will provide the trigger current flowing through the diode string and the pMOS (P1) into the p-substrate, when $V_{\text{pad}} \geqq V_{\text{string}}(I) + |V_{\text{tp}}|$. For a given R_{sub}, the substrate-triggered circuit must supply an enough trigger current (I_{trig}) to raise up the local substrate potential, so that $V_{\text{BE}}(= I_{\text{sub}} \times R_{\text{sub}}) > 0.6$ V for triggering on the parasitic lateral n-p-n bipolar transistor in the stacked-nMOS device. Once the lateral bipolar transistor is turned on, the ESD current is discharged from the I/O pad through the lateral bipolar transistor to the grounded V_{SS}. The I_{trig} provided by the substrate-triggered circuit is determined by the diode string and the size of pMOS (P1). With an appropriate trigger current (I_{trig}), the substrate potential is raised up to trigger on the lateral bipolar transistor and to reduce the trigger voltage of the ESD protection circuit. Therefore, ESD robustness of the mixed-voltage I/O circuits with the stacked-nMOS device can be effectively improved by this new proposed substrate-triggered design.

A modified connection on the ESD protection design with the substrate-triggered stacked-nMOS device to protect the mixed-voltage I/O circuits is shown in Fig. 6. The substrate-triggered circuit is connected from the self-biased n-well of the pull-up pMOS, where the parasitic drain-well diode D_p between the I/O pad and the n-well essentially exists in the pMOS device structure. Under the positive-to-V_{SS} ESD stress condition, the trigger current flows through the parasitic diode D_p and the substrate-triggered circuit to raise the local substrate potential for triggering on the lateral bipolar transistor in the stacked-nMOS device. The main purpose of this modified connection on the ESD protection circuit is to provide the mixed-voltage I/O buffer with a higher ESD robustness but no extra additional capacitance (generating from the ESD detection circuit) to the I/O pad. This modified design is more suitable for high-speed I/O applications, which often require a lower input loading capacitance to the I/O pad.

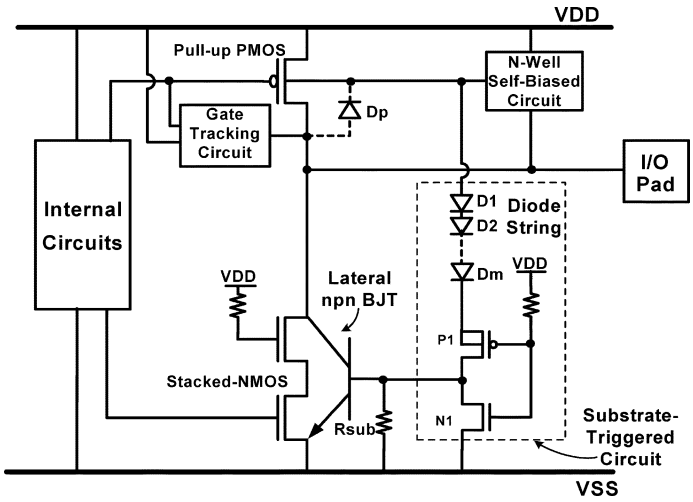

Fig. 6. Modified design of the substrate-triggered stacked-nMOS device with substrate-triggered circuit for the mixed-voltage I/O circuits without generating extra additional capacitance to the I/O pad.

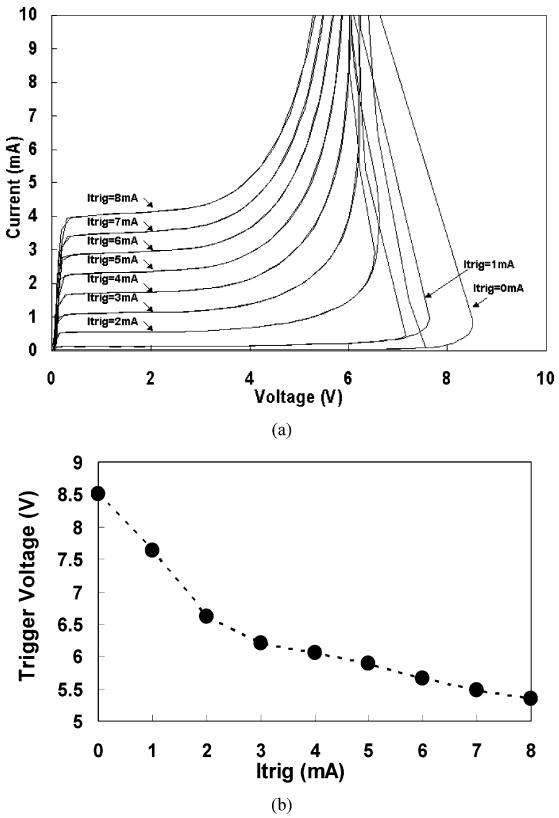

Fig. 7. (a) Measured *I–V* characteristics of the substrate-triggered stacked-nMOS device with different substrate-triggered currents ($I_{\rm trig}$). (b) The relation between the trigger voltage of the stacked-nMOS device and the substrate-triggered current ($I_{\rm trig}$).

III. Experimental Results

A. Characteristics of the Substrate-Triggered Stacked-nMOS Device

The measured current–voltage (*I–V*) characteristics of the substrate-triggered stacked-nMOS device with different substrate-triggered currents (measured by a Tek370 A curve tracer) are shown in Fig. 7(a). The relation between the trigger voltage and the substrate-triggered current ($I_{\rm trig}$) is summarized in Fig. 7(b). As shown in Fig. 7, the trigger voltage of the parasitic lateral bipolar transistor in the stacked-nMOS device is decreased while the substrate-triggered current is increased. The trigger voltage of the stacked-nMOS device without the substrate-triggered current is 8.5 V (by junction breakdown). However, the trigger voltage can be reduced to only 5.3 V when the substrate-triggered current is 8 mA.

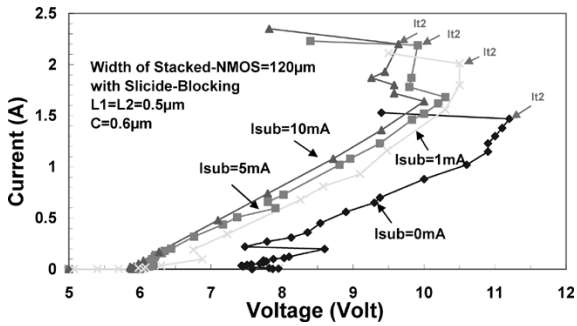

Fig. 8. TLP-measured *I–V* curves of the stacked-nMOS device with different substrate-triggered currents.

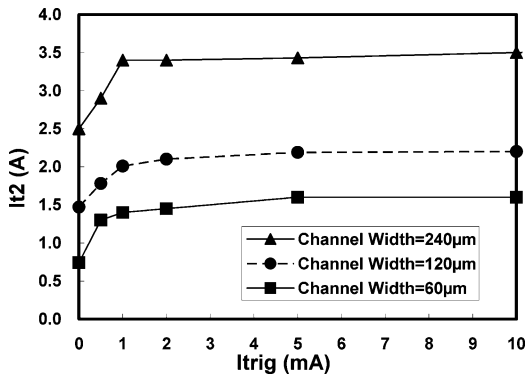

Fig. 9. Dependence of I_{t2} level on the substrate-triggered current ($I_{\rm trig}$) under the different channel widths of substrate-triggered stacked-nMOS device.

To investigate the turn-on behavior of the stacked-nMOS device during high ESD current stress, transmission line pulse (TLP) generator with a pulse width of 100 ns is used to measure the second breakdown current (I_{t2}) of the device. The TLP-measured *I–V* curves of the stacked-nMOS device with different substrate-triggered currents are shown in Fig. 8. The TLP-measured results are consistent with the measured *I–V* characteristics shown in Fig. 7. The trigger voltage of the stacked-nMOS device is decreased when the substrate-triggered current is increased. The dependence of I_{t2} level on the substrate-triggered current ($I_{\rm trig}$) under the different channel widths of substrate-triggered stacked-nMOS device is shown in Fig. 9. The I_{t2} level of the substrate-triggered stacked-nMOS device can be improved while the substrate-triggered current is increased. For example, the I_{t2} level is increased from 2.5 to 3.4 A for the stacked-nMOS device with a channel width of 240 μm, when the substrate-triggered current is increased from 0 to 2 mA. The I_{t2} level of the substrate-triggered stacked-nMOS device is saturated when the substrate-triggered current is high enough to fully trigger on the parasitic bipolar transistor in the stacked-nMOS device.

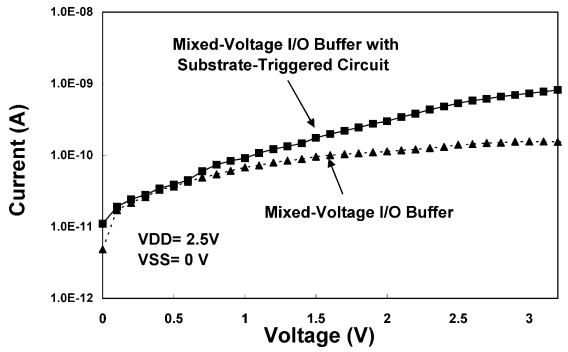

Fig. 10. Comparison of the leakage currents of the mixed-voltage I/O buffers with or without the proposed substrate-triggered circuit. The mixed-voltage I/O buffer in this measurement has a channel width of 240 μm in the stacked nMOS and a channel width of 480 μm in the pull-up pMOS.

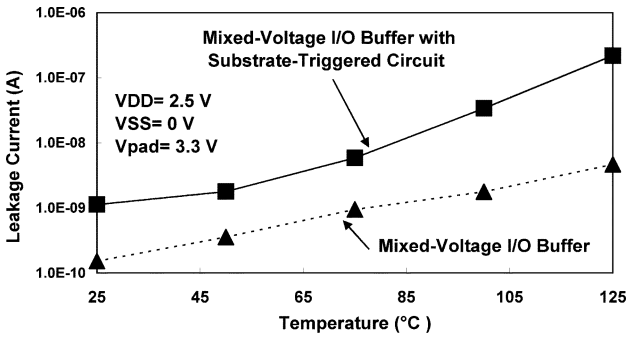

Fig. 11. Leakage currents of the mixed-voltage I/O buffers with or without the substrate-triggered circuit under different temperatures.

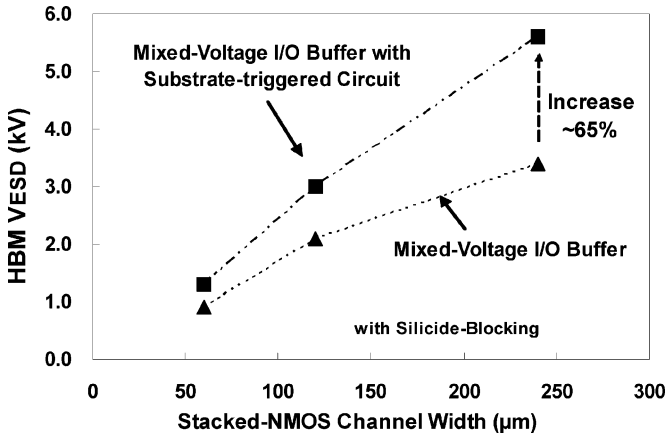

Fig. 12. Positive-to-V_{SS} (PS-mode) HBM ESD levels of the mixed-voltage I/O buffers with or without the substrate-triggered circuit, realized in a 0.25-μm CMOS process with silicide-blocking process.

TABLE I
THE HBM ESD ROBUSTNESS OF THE MIXED-VOLTAGE I/O BUFFERS WITH OR WITHOUT THE PROPOSED SUBSTRATE-TRIGGERED CIRCUIT UNDER A FIXED DEVICE DIMENSION

I/O Circuits \ HBM ESD Stress	PS-Mode VSS(+)	NS-Mode VSS(-)	PD-Mode VDD (+)	ND-Mode VDD (-)
Original Mixed-Voltage I/O Buffer	2.1kV	6.4kV	3.1kV	3.9kV
Mixed-Voltage I/O Buffer + Substrate-Triggered Circuit	3kV	6.4kV	3.3kV	4kV

Pull-up PMOS W/L = 240/0.5 (μm) Stacked-NMOS W/L = 120/0.5 (μm)
with Silicide-Blocking

Based on the experimental results, the ESD protection circuit can be designed with the special substrate-triggered circuit to generate the substrate current to reduce the trigger voltage and to further increase ESD robustness of the stacked-nMOS device in the mixed-voltage I/O buffers.

B. Leakage Current

The leakage current under normal circuit operating condition is a concern for an ESD protection device connected to an I/O pin. The leakage currents of the fabricated mixed-voltage I/O buffers with or without the proposed substrate-triggered circuit are measured and compared in Fig. 10. The leakage current is measured (using a HP4155) by applying a voltage ramp from 0 to 3.3 V to the I/O pad under the bias condition of 2.5-V V_{DD} and 0-V V_{SS} at a room temperature of 25 °C. In Fig. 10, the maximum leakage current of the mixed-voltage I/O buffer with (without) the substrate-triggered circuit under 3.3-V bias at the I/O pad is only 1.1 nA (0.2 nA), which is acceptable for general I/O applications. The mixed-voltage I/O buffer in this measurement has a channel width of 240 μm in the stacked nMOS and a channel width of 480 μm in the pull-up pMOS. The leakage currents of the mixed-voltage I/O buffer with or without the substrate-triggered circuit, under the 3.3-V voltage bias at the I/O pad at different temperatures are shown in Fig. 11. The leakage current of the mixed-voltage I/O buffer is increased while the temperature is increased. In Fig. 11, the leakage current of the mixed-voltage I/O buffer with the substrate-triggered circuit at the temperature of 25 °C (125 °C) is 1.1 nA (0.2 μA). The diode string of the substrate-triggered circuit in this investigation includes six diodes. More diodes can be added into the diode string to further reduce the leakage current of the mixed-voltage I/O buffer with the substrate-triggered circuit.

C. ESD Level

The PS-mode human-body-model (HBM) ESD levels of the mixed-voltage I/O buffers with or without the substrate-triggered circuit are measured and compared in Fig. 12. The failure criterion is defined as the leakage current of the circuits after ESD zapping is greater than 1 μA under the normal operating voltage of 3.3 V. The original mixed-voltage I/O buffers with different stacked-nMOS channel widths are also tested as a reference. As shown in Fig. 12, the HBM ESD level of the mixed-voltage I/O buffers with the substrate-triggered circuit is almost linearly increased while the stacked-nMOS channel width is increased. It implies that the parasitic lateral bipolar transistor in the stacked nMOS can be uniformly turned on to discharge ESD current by the substrate-triggered circuit. The HBM ESD level of the mixed-voltage I/O buffer (with stacked-nMOS channel width of 240 μm) can be obviously improved from the original 3.4 kV up to 5.6 kV (an increase of $\sim 65\%$) by using the substrate-triggered technique.

The HBM ESD robustness of the mixed-voltage I/O buffer, with or without the substrate-triggered circuit, under the four pin-combination modes of ESD stress on the I/O pad, is listed in Table I. The stacked nMOS of the mixed-voltage I/O buffer in this ESD test has a W/L of 120/0.5 μm, and the pull-up pMOS of the mixed-voltage I/O buffer has a W/L of 240 μm/0.5 μm.

As shown in Table I, the PS-mode ESD level of the mixed-voltage I/O buffer is worst among four ESD-zapping modes. The PS-mode ESD level for the mixed-voltage I/O buffer with substrate-triggered circuit can be obviously improved from the original 2.1 up to 3 kV. The experimental result has verified the effectiveness of the substrate-triggered design to improve ESD level of mixed-voltage I/O circuits.

IV. Conclusion

To improve ESD robustness of the stacked-nMOS device in the mixed-voltage I/O circuit, the stacked-nMOS device with new proposed substrate-triggered circuit, has been designed and successfully verified in a 0.25-μm salicided CMOS process. The *I–V* characteristics of stacked-nMOS device with substrate-triggered technique have been measured to verify its effectiveness. By using this substrate-triggered design, the trigger voltage of the stacked-nMOS device can be reduced from the original 8.5 V to become 5.3 V to ensure effective protection for the mixed-voltage I/O circuits. The HBM ESD level of the mixed-voltage I/O buffer with a stacked-nMOS of 240-μm channel width can be improved from the original 3.4 up to 5.6 kV by the substrate-triggered circuit. Without using the thick gate oxide, this new proposed ESD protection design is very useful in the sub-quarter-micrometer CMOS processes for effectively protecting the mixed-voltage interface circuits on the input and output pins.

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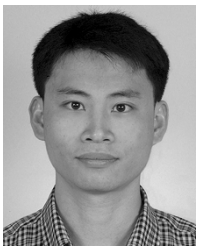

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