PAPER Special Section on Microelectronic Test Structures (ICMTS2007)

Low-Capacitance and Fast Turn-on SCR for RF ESD Protection

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SUMMARY With the smaller layout area and parasitic capacitance under the same electrostatic discharge (ESD) robustness, silicon-controlled rectifier (SCR) has been used as an effective on-chip ESD protection device in radio-frequency (RF) IC. In this paper, SCR's with the waffle layout structures are studied to minimize the parasitic capacitance and the variation of the parasitic capacitance within ultra-wide band (UWB) frequencies. With the reduced parasitic capacitance and capacitance variation, the degradation on UWB RF circuit performance can be minimized. Besides, the fast turn-on design on the low-capacitance SCR without increasing the I/O loading capacitance is investigated and applied to an UWB RF power amplifier (PA). The PA co-designed with SCR in the waffle layout structure has been fabricated. Before ESD stress, the RF performances of the ESD-protected PA are as well as that of the unprotected PA. After ESD stress, the unprotected PA is seriously degraded, whereas the ESD-protected PA still keeps the performances well.

key words: *electrostatic discharge (ESD), low capacitance (low-C), power amplifier (PA), radio-frequency (RF), silicon-controlled rectifier (SCR), waffle layout*

1. Introduction

It has been a trend to integrate the whole radio-frequency (RF) circuits into a single chip [1], [2]. CMOS technology is the leading role to integrate RF circuits. With the scaling-down feature size and lower cost, nanoscale CMOS technology has become suitable to implement RF circuits. However, the thin gate oxide in advanced CMOS processes seriously degrades the reliability of IC products. The major reliability issue for IC products is the damage caused by electrostatic discharge (ESD). Against ESD damages, on-chip ESD protection circuit must be included in IC products [3], [4]. A general concept of on-chip ESD protection for RF ICs is illustrated in Fig. 1 [5], [6]. The ESD protection devices at I/O pad and the power-rail ESD clamp circuit must be provided in RF ICs to accomplish the whole-chip ESD protection. The parasitic capacitance (C_{ESD}) of ESD protection device inevitably contributes capacitive loading to the I/O port, which will disturb the high frequency signals, induce RC delay in the signal path, and cause other degradation on the RF circuit performances [7], [8]. For a 5-GHz low-noise amplifier (LNA) in an RF receiver, a typical specification on the total input loading capacitance is in the order of 100 fF, including the ESD protection device and the bond pad [5]. Therefore, the parasitic capacitance of ESD protection device must be minimized. The device with minimized ratio of parasitic capacitance to ESD robustness is desired.

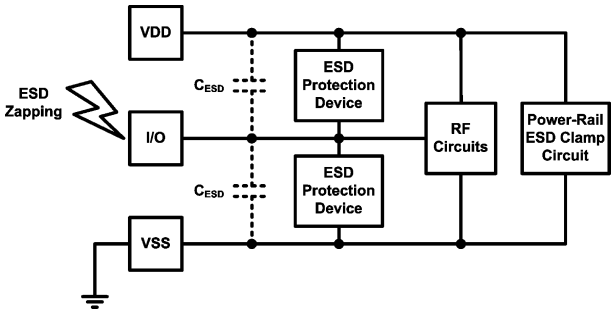

Fig. 1 A general concept of on-chip ESD protection in RF ICs.

Silicon-controlled rectifier (SCR) device had been reported as an useful RF ESD protection element [9], [10]. The SCR device has a much higher ESD robustness within a smaller device size than other ESD protection devices, such as diode, MOS, BJT, or field-oxide device, because of the low holding voltage (V_{hold}, about 1.5 V in general bulk CMOS process) and the low joule heating (power = $I_{ESD} \times V_{hold}$) of the SCR device during ESD stresses [11]. With the smaller device size, using SCR as ESD protection device introduces less parasitic capacitance. To further reduce the parasitic capacitance, the layout structure of SCR device must be considered. SCR devices with waffle layout structure that have the minimized ratio of parasitic capacitance to ESD robustness have been successfully verified in silicon chips [12]. With the minimized parasitic capacitance, the variation of the parasitic capacitance within ultra-wide band (UWB, 3.1–10.6 GHz) frequencies can also be minimized. SCR device with the minimized ratios of parasitic capacitance to ESD robustness and capacitance variation to ESD robustness is more suitable for the UWB RF applications.

In this paper, the parasitic capacitance within UWB frequencies and ESD robustness of the SCR devices with stripe and waffle layout structures have been investigated in a 0.18-μm CMOS process. To improve the turn-on efficiency of SCR devices, the fast turn-on design has also been studied. For the application of the low-capacitance and fast turn-on SCR, a fully integrated UWB RF power amplifier (PA) co-designed with SCR ESD protection circuit is shown in Sect. 6.

Manuscript received December 21, 2007.
Manuscript revised February 29, 2008.

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DOI: 10.1093/ietele/e91–c.8.1321

2. SCR-Based Devices for ESD Protection

2.1 Lateral SCR [13]

The lateral SCR device was used as the effective ESD protection device in CMOS ICs. The equivalent circuit of the lateral SCR is shown in Fig. 2(a). The lateral SCR device consists of a PNP BJT, an NPN BJT, and an N-well/P-well junction to form a 2-terminal/4-layer PNPN structure. The turn-on voltage of the lateral SCR device is dominated by the avalanche-breakdown voltage of the N-well/P-well junction, which could be as high as 15 V in a 0.18-μm CMOS process and greater than the gate oxide breakdown voltage of MOSFET realized with thin oxide in the core circuits.

2.2 Modified Lateral SCR [14]

In order to reduce the turn-on voltage of SCR device, the P+ or N+ trigger diffusion is added across the N-well/P-well junction in the modified lateral SCR to reduce the junction-breakdown voltage. The equivalent circuit of the modified lateral SCR is shown in Fig. 2(b). Because the parasitic capacitance of the lateral SCR device is mainly caused by the N-well/P-well junction, the parasitic capacitance of the modified lateral SCR device is increased due to the extra P+/N-well or N+/P-well junction contributed by the added trigger diffusion across the N-well/P-well junction. The turn-on voltage of the modified lateral SCR can be reduced to ∼10 V in a 0.18-μm CMOS process, and the layout area of the modified lateral SCR with the trigger diffusion will not be increased. Besides, the modified lateral SCR can be applied with the substrate-triggered technique to improve its turn-on efficiency [15]. When trigger diffusion serves as the trigger port, an extra trigger circuit can be designed to supply the trigger current to enhance the turn-on efficiency. Although the additional trigger circuit occupies some layout area, it does not add any loading effect at I/O pad, which will be discussed in Sect. 5.

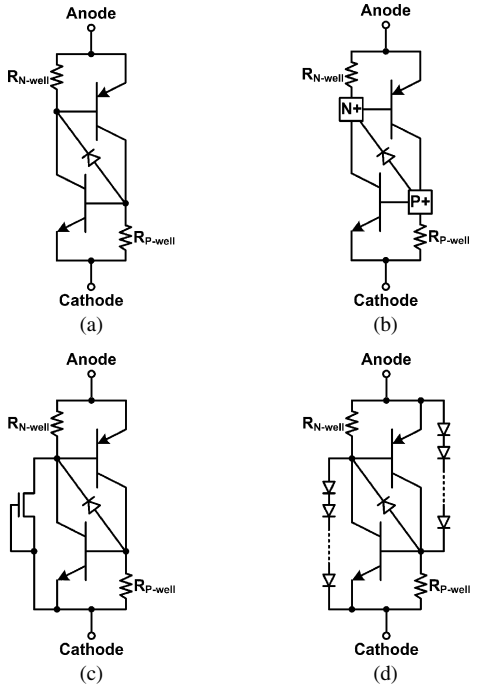


Fig. 2 Equivalent circuit of (a) lateral SCR, (b) modified lateral SCR, (c) low-voltage-triggering SCR, and (d) diode-triggered SCR.

2.3 Low-Voltage-Triggering SCR [16]

The equivalent circuit of the low-voltage-triggering SCR (LVTSCR) is shown in Fig. 2(c). A short-channel NMOS device is inserted into the lateral SCR structure. The turn-on voltage of the LVTSCR is equivalent to the drain-breakdown or punch-through voltage of the inserted NMOS device. The NMOS device in the LVTSCR is parallel with the N-well/P-well junction, so the total parasitic capacitance will become too large which is not suitable for RF applications. Other MOS-triggered SCR devices, such as gate-coupled LVTSCR, gate-grounded NMOS triggered SCR, and PMOS-trigger lateral SCR [17], [18], also have too large parasitic capacitance loading to RF circuits.

2.4 Diode-Triggered SCR [19]

The equivalent circuit of the diode-triggered SCR is shown in Fig. 2(d). The diode-triggered SCR employs a diode chain to trigger the PNP or NPN BJT to latch the SCR device, which has faster turn-on speed. The turn-on voltage of the diode-triggered SCR is approximately the voltage drop of the forward-biased diode chain. However, the large leakage current of the diode-triggered SCR during normal operating condition is a serious concern.

Among all SCR-based devices, the lateral SCR and the modified lateral SCR devices have the lower parasitic capacitances. So, in this work, the test structures on lateral SCR and modified lateral SCR devices were studied.

3. Test Structures on SCR Devices for RF ESD Protection

3.1 Stripe-Structured and Waffle-Structured SCR

Figure 3 shows the device cross-sectional view of the stripe-structured SCR (SSCR) and waffle-structured SCR (WSCR). Both devices were designed with the same size of $60.62 \times 60.62\,\mu m^2$. The SCR devices are composed of four regions of P+/N-well/P-well/N+. The anode of the SCR device is electrically connected to P+ and N+, which are formed in the N-well. The cathode is electrically connected to N+ and P+, which are formed in the nearby P-well/P-substrate. When a positive potential is applied between the anode and the cathode, the N-well/P-well junction is reverse-biased, so the SCR device is kept off under normal circuit operating conditions. When an ESD stress is zapped to the anode with cathode grounded, the SCR device will

become highly conductive to quickly discharge ESD current due to the turn-on of latchup path [20], [21]. In the SSCR, it discharges ESD current in only two directions, whereas the WSCR discharges ESD current in four directions. Thus, the ESD robustness can be improved under the same parasitic capacitance by using the SCR with waffle layout structure. In other word, the ratio of the parasitic capacitance to ESD robustness can be minimized by realizing the SCR with waffle layout structure.

3.2 Modified Stripe-Structured and Waffle-Structured SCR

Figure 4 shows the device cross-sectional view of the modified stripe-structured SCR (MSSCR) and the modified waffle-structured SCR (MWSCR). Since the large trigger diffusion increases the parasitic capacitance, the MSSCR and MWSCR were implemented with separated trigger diffusions to evaluate their ESD robustness and parasitic capacitance. The trigger diffusion areas of two MSSCR were $123.2\,\mu m^2$ and $242.48\,\mu m^2$, and those of three MWSCR are $70.24\,\mu m^2$, $140.48\,\mu m^2$, and $264.96\,\mu m^2$, respectively. All devices were designed in the same layout area of $60.62 \times 60.62\,\mu m^2$. These devices shown in Figs. 3 and 4 have been fabricated in a 0.18-μm CMOS process for experimental investigations.

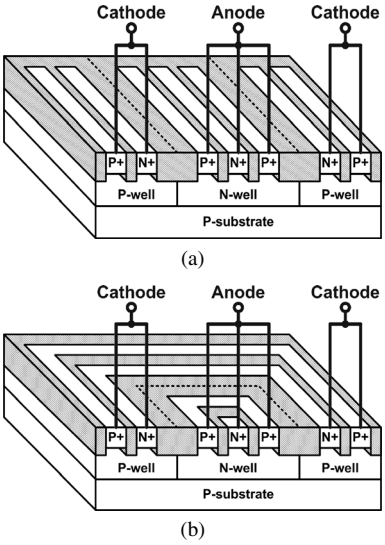


Fig. 3 Device cross-sectional view of (a) stripe-structured SCR (SSCR) and (b) waffle-structured SCR (WSCR).

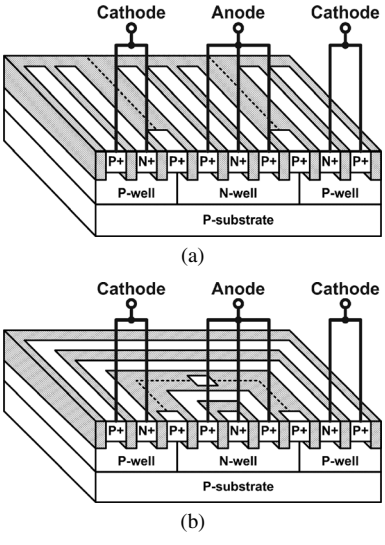


Fig. 4 Device cross-sectional view of (a) modified stripe-structured SCR (MSSCR) and (b) modified waffle-structured SCR (MWSCR).

4. Measured SCR Device Characteristics

4.1 Transmission Line Pulsing (TLP) Measurement

The turn-on voltage ($V_{turn\text{-}on}$), secondary breakdown current (I_{t2}), and turn-on resistance (R_{on}) in the holding region of the fabricated SCR devices were characterized by the TLP system. The TLP-measured I-V curves for SSCR and MSSCR are shown in Fig. 5(a). According to the measured I-V characteristics, SSCR is turned on at about 17 V. With the trigger diffusion added into the MSSCR, the turn-on voltages are reduced to about 13 V. The secondary breakdown currents of all SCR devices with stripe layout structure exceed 6 A, which is the limitation of TLP system used in this measurement. The TLP-measured turn-on resistance of the SSCR and MSSCR are about $\sim 1\,\Omega$.

The TLP-measured I-V curves for WSCR and MWSCR are shown in Fig. 5(b). WSCR is turned on

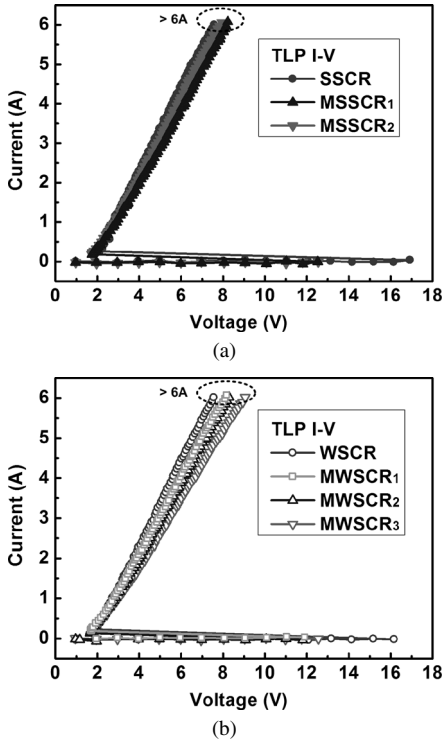


Fig. 5 TLP-measured I-V characteristics of (a) SSCR and MSSCR, and (b) WSCR and MWSCR.

Table 1 Comparisons on measured device characteristics of SCR devices with different structures.

Structure	Symbol	Trigger Diffusion Area (μm^2)	$V_{turn\text{-}on}$ (V)	$V_{turn\text{-}on}$* (V)	R_{on} (Ω)	I_{t2} (A)	V_{HBM} (kV)	V_{MM} (kV)	ΔC_{ESD} Within 3.1~10.6GHz (fF)
Stripe	SSCR	0	16.92		0.95	> 6	> 8	1.80	32.12
Stripe	$MSSCR_1$	123.2	12.52	5.711	1.09	> 6	> 8	1.63	53.41
Stripe	$MSSCR_2$	242.48	12.54	6.163	1.02	> 6	> 8	1.68	67.47
Waffle	WSCR	0	16.17		0.96	> 6	> 8	1.53	18.19
Waffle	$MWSCR_1$	70.24	11.91	5.24	1.08	> 6	> 8	1.52	29.24
Waffle	$MWSCR_2$	140.48	11.81	5.688	1.10	> 6	> 8	1.59	39.36
Waffle	$MWSCR_3$	264.96	12.55	5.696	1.22	> 6	> 8	1.56	49.13

* Turn-on voltage of CR-triggered MSSCR and MWSCR.

at about 16 V, and the MWSCR are turned on at about 12 V. The secondary breakdown currents of the WSCR and MWSCR all exceed 6 A. The turn-on resistance of each SCR device with waffle structure is about ~1 Ω. The measured results on the device characteristics of the fabricated SCR devices with different layout structures are listed in Table 1.

4.2 ESD Robustness

The human-body-model (HBM) ESD robustness of the fabricated SCR devices were evaluated by the ESD simulator. All SCR devices pass the HBM ESD test (V_{HBM}) of 8-kV, which is the measurement limitation of HBM ESD tester. In order to distinguish the ESD robustness of the SCR with stripe layout structure from the SCR with waffle layout structure, the machine-model (MM) ESD tests were performed. The MM ESD levels (V_{MM}) of all SCR devices are within the range of 1.4–1.8 kV, as listed in Table 1. Despite the MM ESD robustness of the SCR with waffle layout structure is slightly worse than that of the SCR with stripe layout structure due to the reduction of the N-well area in the waffle layout structure, the parasitic capacitance can be greatly reduced.

4.3 Parasitic Capacitance

In order to fit the devices for on-wafer two-port S-parameter measurement, the SCR devices were implemented with ground-signal-ground (G-S-G) pads, as shown in Fig. 6(a). The high-frequency S-parameters were measured under the bias of 0.9 V (VDD/2 in a 0.18-μm CMOS process) by using the vector network analyzer HP 8510C, and the Y_{11}-parameter can be obtained from the measured S-parameters by using

$$Y_{11} = \frac{(1 - S_{11})(1 + S_{22}) + S_{12}S_{21}}{Z_0\left((1 + S_{11})(1 + S_{22}) - S_{12}S_{21}\right)}, \quad (1)$$

where Z_0 is the termination resistance and equals to 50 Ω. Because the SCR devices were arranged with the pads, the intrinsic characteristics of the SCR devices in high frequency were embedded within the parasitic effects of metal interconnects and bond pads. To de-embed the intrinsic characteristics of the SCR devices, the stand-alone pad that

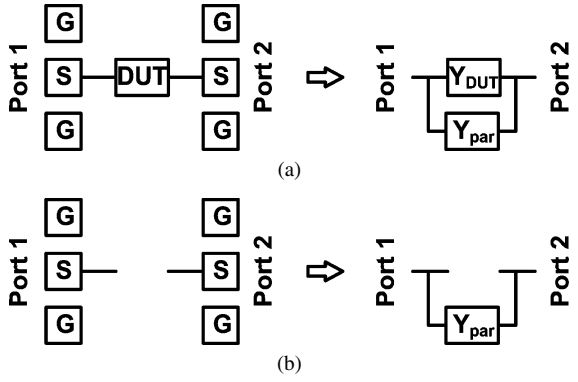


Fig. 6 Layout top view with ground-signal-ground (G-S-G) pads and equivalent model of (a) including-DUT pattern and (b) excluding-DUT pattern.

is shown in Fig. 6(b) was fabricated in the same chip. The test patterns, one including the device under test (DUT) but the other excluding the DUT, were fabricated in the same chip. The intrinsic device Y_{11}-parameter (Y_{DUT}) can be obtained by subtracting Y_{par} from Y_{meas}, where Y_{meas} is the Y_{11}-parameter of the including-DUT pattern, and Y_{par} is the Y_{11}-parameter of the excluding-DUT pattern. Finally, the parasitic capacitance of SCR device can be extracted from the Y_{DUT} by using

$$C_{ESD} = \frac{\mathrm{Im}(Y_{DUT})}{2\pi f}, \quad (2)$$

where f is the operating frequency. Figure 7 shows the extracted parasitic capacitance within UWB frequencies (3.1–10.6 GHz) of all SCR devices.

4.4 Comparison on Parasitic Capacitance and ESD Robustness

The ratios of the parasitic capacitance to MM ESD robustness (C_{ESD}/V_{MM}) within UWB frequencies of all SCR devices were evaluated and compared in Fig. 8. According to the measured result, the averaged ratios of C_{ESD}/V_{MM} of SSCR and WSCR are about 50 fF/kV and 40 fF/kV, respectively. The C_{ESD}/V_{MM} ratio of WSCR has a decrease of about 25% as compared with that ratio of SSCR. As to MSSCR and MWSCR, the averaged ratios of C_{ESD}/V_{MM}

of MSSCR and MWSCR are about 80–90 fF/kV and 60–75 fF/kV, respectively. The C_{ESD}/V_{MM} ratios are increased with the increase of the P+ trigger diffusion area. The C_{ESD}/V_{MM} ratios of MWSCR have also a decrease of about 25%, as compared with that of MSSCR.

The variation of the parasitic capacitance within 3.1–10.6 GHz (ΔC_{ESD}) of the SCR with stripe and waffle layout structures are about 30–70 fF and 15–50 fF, respectively, which are summarized in Table 1. The ratios of the capacitance variation within 3.1–10.6 GHz to MM ESD robustness ($\Delta C_{ESD}/V_{MM}$) of the SCR for stripe and waffle layout structures are compared in Fig. 9. The ratio ($\Delta C_{ESD}/V_{MM}$) of the SCR in waffle layout has also a significant decrease as compared with that of the SCR in stripe layout.

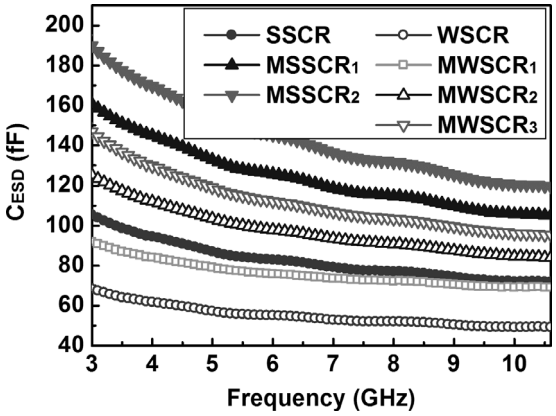


Fig. 7 Extracted parasitic capacitance within 3.1–10.6 GHz of SCR devices with different layout structures.

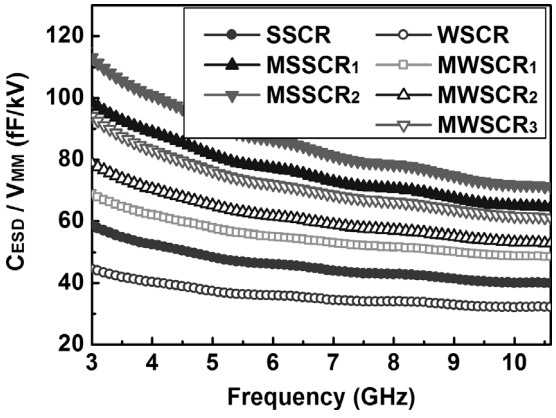


Fig. 8 Ratios of parasitic capacitance to MM ESD robustness within 3.1–10.6 GHz of SCR devices with different layout structures.

4.5 Comparison among SCR-Based Devices for RF ESD Protection

Based on the measurement results in this paper and the prior work [11], the qualitative comparisons among SCR-based devices in terms of turn-on voltage, turn-on speed, parasitic capacitance/ESD robustness, leakage current, and layout area, have been summarized in Table 2. With consideration on the merit of parasitic capacitance/ESD robustness, the proposed waffle SCR device will be a good solution for RF ESD protection.

5. Fast Turn-on Design on SCR Devices

To further reduce the turn-on voltage of MSSCR and MWSCR, the P+ trigger diffusion can be treated as the trigger port, and the trigger current can be injected to enhance the turn-on efficiency. The equivalent circuit of the triggered MSSCR and MWSCR is shown in Fig. 10. In order to build the trigger circuit to trigger MSSCR or MWSCR without

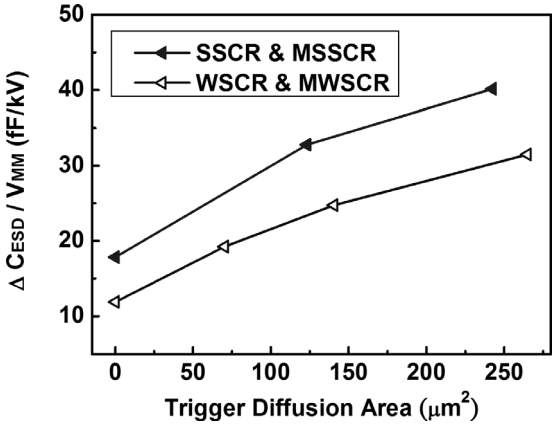


Fig. 9 Dependence of ratio of capacitance variation within 3.1–10.6 GHz to MM ESD robustness ($\Delta C_{ESD}/V_{MM}$) on trigger diffusion area of SCR devices with different layout structures.

Table 2 Comparisons among SCR-based devices for RF ESD protection.

SCR Category	Turn-on Voltage	Turn-on Speed	Parasitic Capacitance / ESD Robustness	Leakage Current	Layout Area
Traditional Lateral SCR (SSCR)	high	slow	low	low	small
Traditional Modified Lateral SCR (MSSCR)	middle	slow	low	low	small
Waffle Lateral SCR (WSCR)	high	slow	low	low	small
Waffle Modified Lateral SCR (MWSCR)	middle	slow	low	low	small
Substrate-Triggered SCR	low & tunable	fast	low	low	middle
Low-Voltage-Triggering SCR	low	middle	middle	middle	middle
Diode-Triggered SCR	low	fast	middle	high	middle

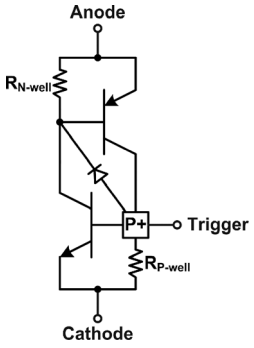


Fig. 10 Equivalent circuit of triggered MSSCR and MWSCR.

increasing the I/O loading capacitance, the new proposed ESD protection strategy for RF ICs is shown in Fig. 11. Compared this with Fig. 1, the ESD protection devices are composed of a diode from I/O to VDD and a MSSCR or MWSCR from I/O to VSS. The trigger circuit of MSSCR or MWSCR between VDD and VSS is separated from the I/O port and not adding the I/O loading. Figure 11(a) shows the discharging path under positive-to-VSS mode (PS-mode) ESD zapping, which is a worse case of ESD events [22]. During PS-mode ESD stress, ESD current will first pass through the diode to VDD, and the trigger circuit will trigger MSSCR or MWSCR. The major ESD current will be discharged by MSSCR or MWSCR from the I/O pad to VSS. Under other ESD stress modes, including positive-to-VDD (PD-mode), negative-to-VSS (NS-mode), and negative-to-VDD (ND-mode), the proposed ESD protection circuit also provides the corresponding current discharging paths with good ESD robustness, which are also shown by the dashed lines in Fig. 11. The TLP-measured I-V curves for this circuit under NS-mode ESD stresses are shown in Fig. 12, which were the I-V curves of the P-well/N-well diodes in SCRs. The I-V curve under PD-mode ESD stress was similar to the curve shown in Fig. 12, and the I-V curve for ND-mode stress was the I-V curve of a triggered SCR in series with a diode.

To demonstrate the function of the fast turn-on design on SCR devices under PS-mode stress, the experimental setup to measure the TLP I-V characteristics of the triggered MSSCR and MWSCR is shown in Fig. 13. The trigger circuit was composed of a 20-pF capacitance and a 20-kΩ resistance. The RC time constant of the trigger circuit was designed in the order of 10^{-6}–10^{-7} s to detect ESD events. Under normal circuit operation, the trigger port of the MSSCR or MWSCR was biased at VSS to be kept off. When the ESD pulse was zapping, the trigger port was coupled to high potential by the ESD energy. Therefore, the trigger current will be injected into the trigger port by the CR trigger circuit, and the MSSCR or MWSCR will be quickly turned on. The TLP-measured I-V curves for CR-triggered MSSCR and MWSCR are shown in Figs. 14(a) and 14(b), respectively. The turn-on voltage of all CR-triggered MSSCR and MWSCR ($V_{turn\text{-}on}$*) are reduced to about 6 V, as listed in Table 1. The turn-on voltages among the SCR devices under

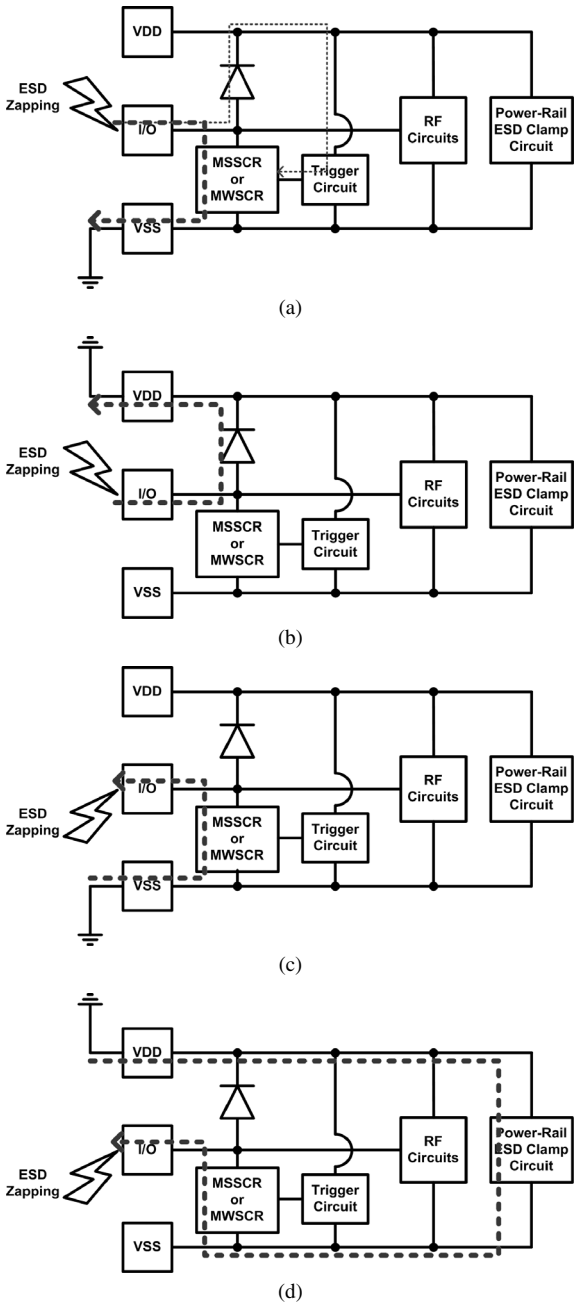


Fig. 11 Application of the proposed MSSCR or MWSCR devices in on-chip ESD protection design for RF ICs with low-capacitance consideration, and the discharging current path under (a) PS-mode, (b) PD-mode, (c) NS-mode, and (d) ND-mode ESD zapping.

different layout structures are compared in Fig. 15. The 6-V turn-on voltage of CR-triggered SCR devices is much lower than the breakdown voltage of the internal circuits in a 0.18-μm CMOS process, so the fast turn-on design is proved to be feasible.

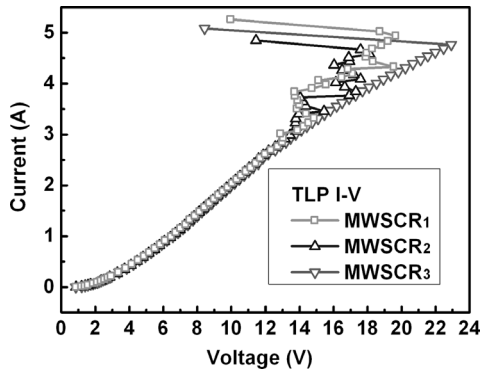


Fig. 12 TLP-measured I-V characteristics of MWSCR under NS-mode ESD stress.

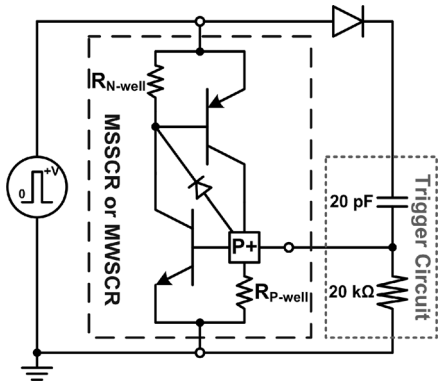
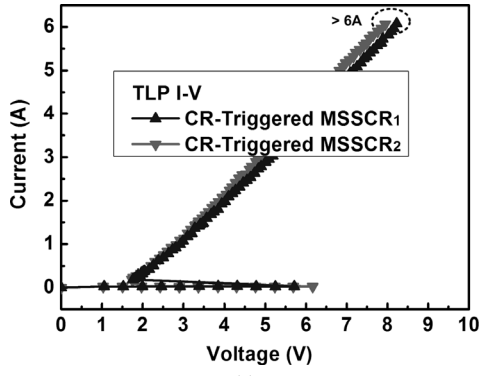
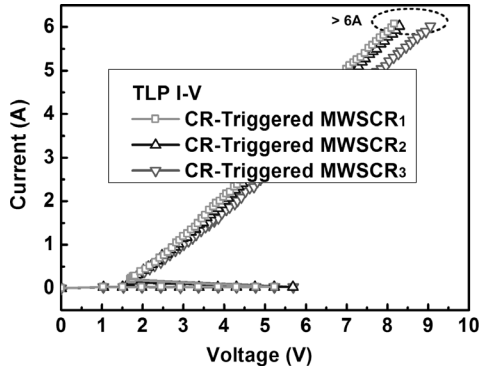


Fig. 13 Measurement setup to find I-V characteristics of CR-triggered MSSCR and MWSCR.



(a)



(b)

Fig. 14 TLP-measured I-V characteristics of CR-triggered (a) MSSCR and (b) MWSCR.

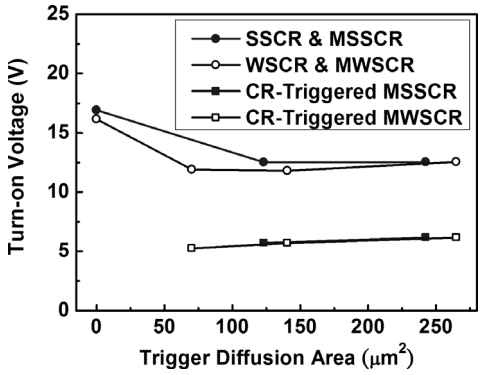


Fig. 15 Dependence of turn-on voltage on trigger diffusion area of SCR devices with different structures.

6. Application of Low-Capacitance and Fast Turn-on SCR in RF PA

6.1 UWB RF PA and ESD Protection Design

This section presents a fully integrated UWB class-AB PA co-designed with ESD protection circuit. The PA with and without the ESD protection circuit are designed and fabricated in a 0.13-μm CMOS process. The presented UWB RF PA is a three-stage distributed amplifier (DA). The UWB applications cover the frequency band from 3.1 GHz to 10.6 GHz. The DA is intrinsically suitable for this bandwidth and widely used for PA [23]. Figure 16 shows the circuit schematic of the PA. The active core devices (M1 and M2) of each stage are in cascode topology. The cascode topology provides good voltage gain and good isolation. It also prevents drain overstress since the voltage swing may approach $2 \times$ VDD at the output node. The device size and voltage/current bias of the cascode pair is designed to produce a particular current that gives the active core device with a 50-Ω loading for its optimal load-line resistance within its operational dynamic range. With such a manner, the DA can simultaneously satisfy a 50-Ω conjugate match and optimal load-line match.

The UWB RF PA with the proposed ESD protection circuit is shown in Fig. 17. It contains a waffle-structured diode string from output (O/P) to VDD, and a MWSCR from O/P to VSS with a RC-inverter as a trigger circuit. The diode string can avoid the signals leak from O/P to VDD since the voltage swing may approach $2 \times$VDD (VDD = 1.2 V in a 0.13-μm CMOS process) at the output node. Besides, another set of RC-inverter-triggered SCR acts as the power-rail ESD clamp circuit to provide the discharging path between VDD and VSS. The RC time constants of the trigger circuits were designed in the order of 10^{-6}–10^{-7} s to detect ESD events. The capacitor of each trigger circuit was composed of a MOS capacitor and was in the area of about 1700 μm^2. Under normal circuit operation, ESD protection circuits were all kept off. During PS-mode ESD stress, with ESD pulses zapping to O/P of the protected PA, ESD current will first flow through the diodes to VDD, and then flow into

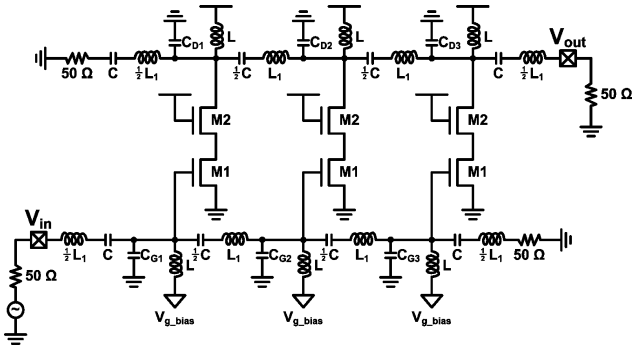


Fig. 16 Equivalent circuit of UWB RF PA (unprotected PA).

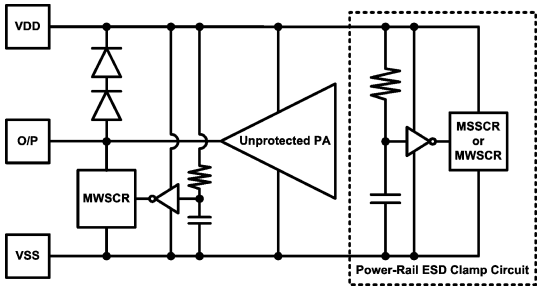


Fig. 17 Equivalent circuit of UWB RF PA with the proposed ESD protection circuit (ESD-protected PA).

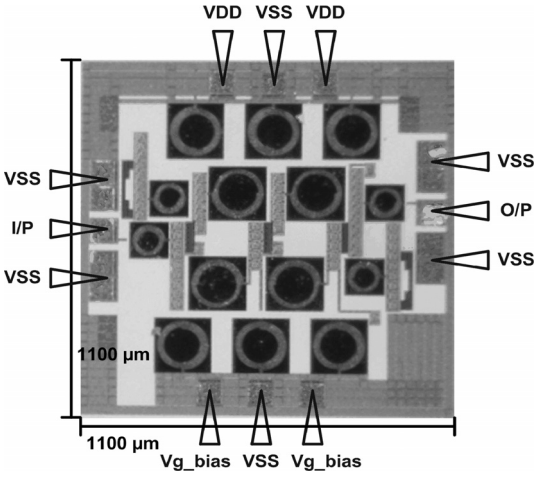
the RC-inverter to trigger the MWSCR. The ESD current will be discharged by the MWSCR from the O/P to VSS. Therefore, the ESD protection ability can be significantly improved. The die photos of the fabricated chips of the unprotected PA and ESD-protected PA are shown in Figs. 18(a) and 18(b), respectively.

6.2 Measured RF Performance after ESD Zapping

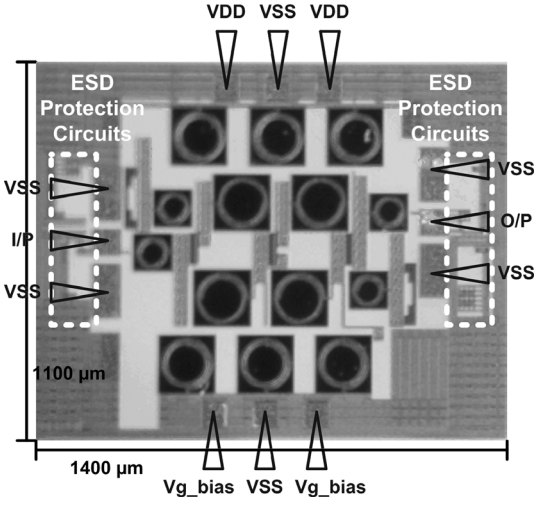
The S-parameters of the UWB RF PA were measured by using the Agilent E8364B PNA. An Agilent E4448A spectrum analyzer and an Agilent E8257D signal generator were used to evaluate the large signal characteristics of the PA. To compare the ESD protection capability between the PA with and without ESD protection circuit, the RF performance of PA was measured again after each HBM ESD zapping.

The S_{21}-parameter is the forward gain of the PA. The measured results of the S_{21} from 2 to 12 GHz of the PA without ESD protection circuit (unprotected PA) and that of the PA with ESD protection circuit (ESD-protected PA) are shown in Figs. 19(a) and 19(b), respectively. The S_{21} of the unprotected PA was severely degraded after HBM ESD zapping, as seen in Fig. 19(a). On the contrast, the S_{21} of the ESD-protected PA was still excellent matching even if the 8-kV HBM ESD test was performed (8-kV is the maximum limitation of ESD simulator). The bandwidths of the unprotected and ESD-protected PA after each HBM ESD zapping are summarized in Table 3.

The averaged large signal power gain of the unprotected and ESD-protected PA within 3.1–10.6 GHz after each HBM ESD zapping are also listed in Table 3. According to the measured data, both the bandwidth and the averaged large signal gain of the ESD-protected PA are kept fine after each HBM ESD stress, while those of the unprotected PA are seriously degraded. When the output power increases, the output swing would be compressed. The output power at 1-dB compression point (OP1dB) can be treated as the maximum linear output power capability of the PA. Figures 20(a) and 20(b) show the measured results on the OP1dB of the unprotected and ESD-protected PA, respectively. The OP1dB of the unprotected PA was seriously degraded after HBM ESD zapping. The OP1dB of the ESD-protected PA was not degraded even after 8-kV HBM ESD test.



(a)



(b)

Fig. 18 Die photos of the fabricated (a) unprotected PA and (b) ESD-protected PA.

7. Conclusion

SCR with the waffle layout structure has been verified to have the reduced parasitic capacitance under the same ESD robustness. The ratios of the parasitic capacitance to MM

Table 3 Bandwidth and gain of UWB RF PA after HBM ESD zapping.

HBM ESD Zapping	Bandwidth		Averaged Gain (3.1~10.6GHz)	
	Unprotected PA	ESD-Protected PA	Unprotected PA	ESD-Protected PA
0 V	7.8 GHz	7.3 GHz	12.4 dB	9.8 dB
1 kV	7.7 GHz	7.4 GHz	8.9 dB	9.3 dB
2 kV	8.2 GHz	7.3 GHz	-0.4 dB	9.2 dB
4 kV	0 GHz	7.4 GHz	-51.8 dB	8.5 dB
8 kV	0 GHz	7.3 GHz	-55.3 dB	9.5 dB

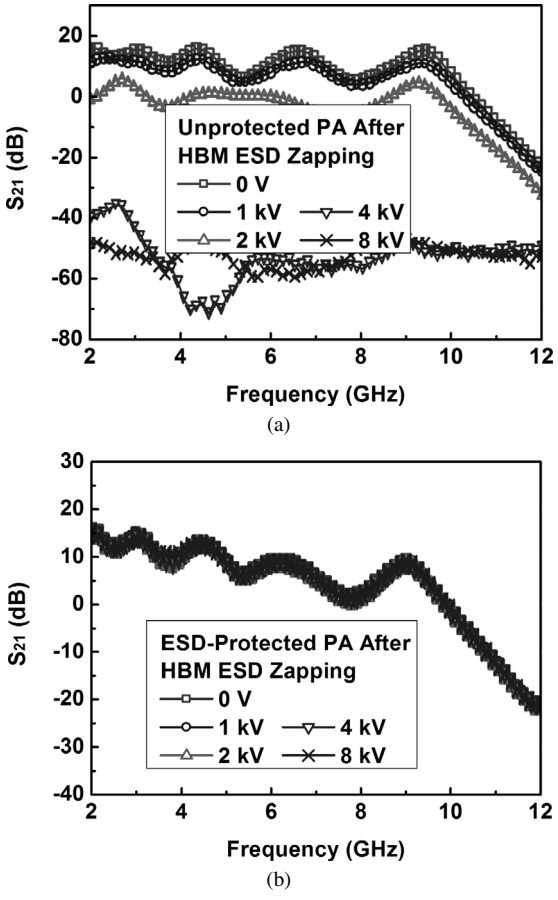


Fig. 19 Measured results on S_{21}-parameter of (a) unprotected PA and (b) ESD-protected PA, after each HBM ESD zapping.

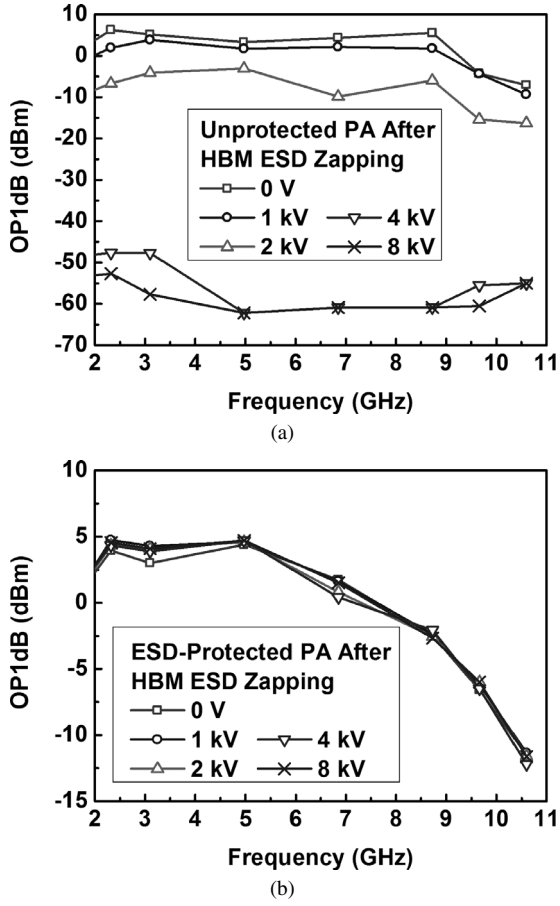


Fig. 20 Measured results of output power 1-dB compression point of (a) unprotected PA and (b) ESD-protected PA, after each HBM ESD zapping.

ESD robustness of WSCR and MWSCR have the decreases of about 25% as compared to SSCR and MSSCR. SCR with the waffle layout structure has also been verified to reduce the variation of the parasitic capacitance within UWB frequencies. Thus, SCR realized in the waffle layout structure is more suitable for on-chip ESD protection in UWB RF circuits than that realized in the stripe layout structure. Although the parasitic capacitance is increased with the added P+ trigger diffusion, the turn-on voltage can be reduced to effectively protect the RF circuits against ESD damages. The fast turn-on design on low-capacitance SCR with the waffle layout structure has also been studied and applied to the UWB RF circuit. The RF measured results have confirmed that the performance of the unprotected PA is seriously degraded after ESD zapping. The PA co-designed with the proposed ESD protection circuit can minimize the negative impact of ESD protection devices on RF circuit performance, and provide excellent ESD robustness.

Acknowledgments

This work was supported by United Microelectronics Corporation (UMC), and National Science Council (NSC), Taiwan, under Contract of NSC 96-2221-E-009-182.

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