

Design of Analog Output Buffer With Level Shifting Function on Glass Substrate for Panel Application

Tzu-Ming Wang, *Student Member, IEEE*, Ming-Dou Ker, *Fellow, IEEE*, and Sao-Chi Chen

Abstract—Two analog output buffers with level shifting function containing the digital-to-analog converter (DAC) circuit with gamma correction have been designed and verified in a 3- μm low temperature poly-silicon (LTPS) technology, which are suitable for integrated on glass substrate for panel application. The new proposed circuits utilize the DAC with gamma correction of 3-V liquid crystal (LC) specification, but it can also drive the 5-V liquid crystal to meet the desired 5-V gamma curve without re-designing the DAC with 5-V gamma correction parameters.

Index Terms—Analog output buffer, digital-to-analog converter (DAC), gamma correction, low temperature poly-silicon (LTPS), system-on-panel (SOP).

I. INTRODUCTION

LTPS TECHNOLOGY with higher mobility characteristic, which has been widely applied in active matrix liquid crystal display (AMLCD), is conceived as one of most desirable technology to accomplish system-on-panel (SOP) integration for portable systems, such as digital camera, mobile phone, personal digital assistants (PDAs), notebook, and so on. The periphery circuit blocks of LCD panel are roughly composed of four parts: display panel, timing control circuit, scan driver circuit, and data driver circuit. Display panel is constructed of the active matrix liquid crystals and the operation of the active matrixes is similar to DRAM (dynamic random access memory) which is used to charge and discharge the capacitor of the pixel. Timing control circuit is responsible for transmitting red, green, and blue (RGB) signals to the data driver and controlling the behavior of scan driver. Data driver circuit, shown in Fig. 1, is composed of shifter register (S/R), data latch, level shifter (L/S), DAC, and analog output buffer. Shifter register and data latch are used to transit and store the RGB signals while level shifter translates the RGB signal to a higher voltage level due to the higher operating voltage of active matrixes. In addition, DAC is used to convert the digital RGB signal to analog gray level with consideration of gamma correction. The LCD panel with larger panel size or higher resolution display results in larger load to this signal, so the analog output buffer is essential to provide the driving capability of the data driver [1].

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T.-M. Wang and S.-C. Chen are with the Nanoelectronics and Gigascale Systems Laboratory, Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan 300.

M.-D. Ker is with the Nanoelectronics and Gigascale Systems Laboratory, Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan 300, and also with the Department of Electronic Engineering, I-Shou University, Kaohsiung, Taiwan (e-mail: mdker@ieee.org).

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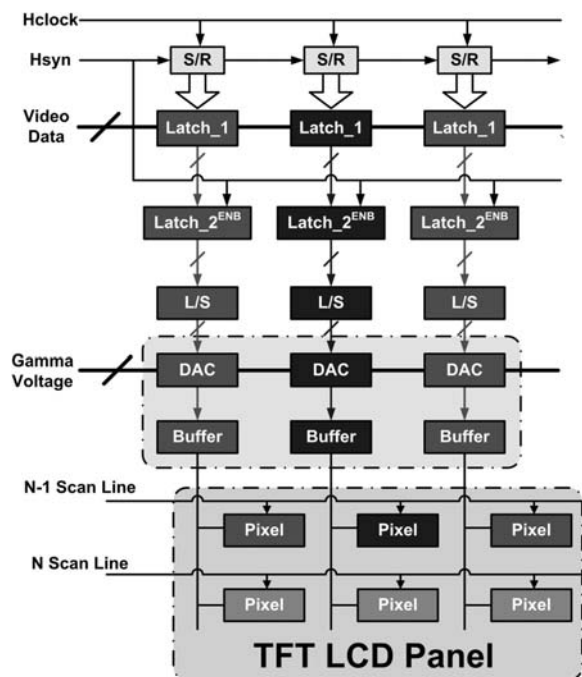


Fig. 1. Basic diagram of data driver circuit for TFT LCD panel.

SOP application has the potential to realize compact, highly reliable, and high resolution display by integrating functional circuits within a display. For a-Si TFT-LCDs, TAB-ICs are connected to the left and bottom sides of a panel as the Y driver and the X driver, respectively. Integration of the Y and X drivers with LTPS TFTs on panel requires printed circuit board (PCB) connection on the bottom of the panel only. The most common failure mechanism of TFT-LCDs, disconnection of the TAB-ICs, is therefore decreased significantly with the save in omitting the usage of ICs and all sub-circuits integrated on panel. Besides, the cost of panel becomes lower, as well as the higher yield rate can be also achieved [2]. Furthermore, some poly-Si TFT characteristics, such as high carrier mobility, low threshold voltage, high stability, and high reliability, are required to fulfill the SOP application. Such integration technology contributes to shorten the product lead time because the assemblage of CMOS ICs can be eliminated. Currently, such integration has been proceeding from simple digital circuits to the sophisticated ones. Moreover, LTPS technology is compatible with organic light emitting diode (OLEDs), which is another promising display device. Therefore, design of driving circuits for TFT-LCD in LTPS technology has been proceeding. In [3], a TFT-based 8-bit source driver for 2.0-in QVGA AMOLED panels had been proposed to reduce source driver size about 40%. In [4] and [5], the TFT devices had been reported to have large variation in

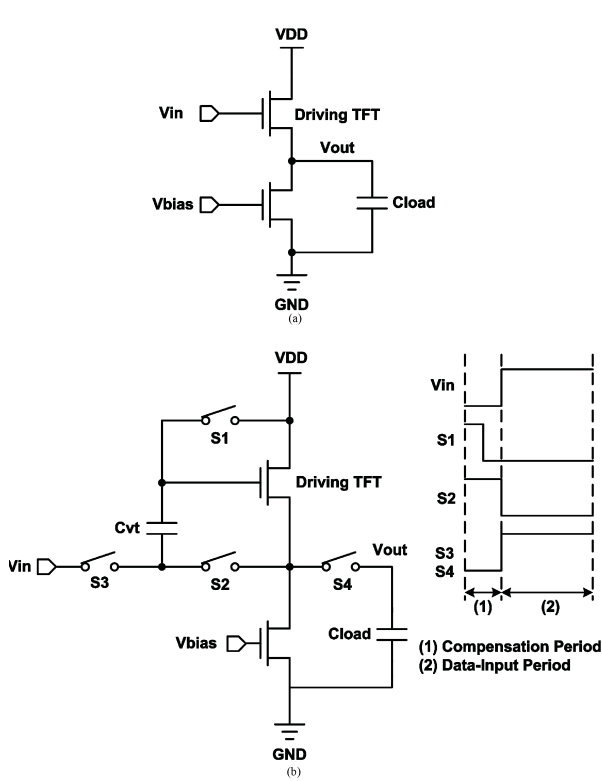


Fig. 2. (a) Conventional source follower analog output buffer with active load and (b) modified source follower analog output buffer with compensation capacitor [12].

the threshold voltage and device characteristics, so the device characteristic variation is a very important issue for analog circuit design in LTPS technology. The carrier mobility depends on the grain size of the active poly-Si layer, and the deviation of the TFT characteristics is related to the quality of the poly-Si layer [6]. Some recent works had been reported to suppress the variation of poly-Si TFT characteristics to further redeem SOP application. In [7], a class-B output buffer with offset compensation had been proposed to compensate the offset of output buffer to provide high resolution display and uniform brightness display. In [8], a new gate-bias generating technique with threshold-voltage compensation had been presented to reduce the impact of threshold-voltage variation on analog circuit performance in LTPS technology.

Some kinds of circuits had been successfully integrated on TFT-LCD substrates for SOP application. In [9], a low power consumption TFT-LCD with dynamic memory embedded in each pixel has been proposed to hold a digital data corresponding to display image in the memory, so the operation of data driver can be simplified to reduce power consumption. In [10], it reported the first LCD equipped with all the circuits to display static images continuously for up to one year powered with a button battery. In [11], an 8-bit CPU containing 13 000 TFTs on a glass substrate reported to demonstrate the feasibility of the SOP.

In this work, two analog output buffers with level shifting function containing the DAC circuit with gamma correction have been designed and verified in a 3- μm low temperature poly-silicon (LTPS) technology, which are suitable for integrated on glass substrate for panel application. The new

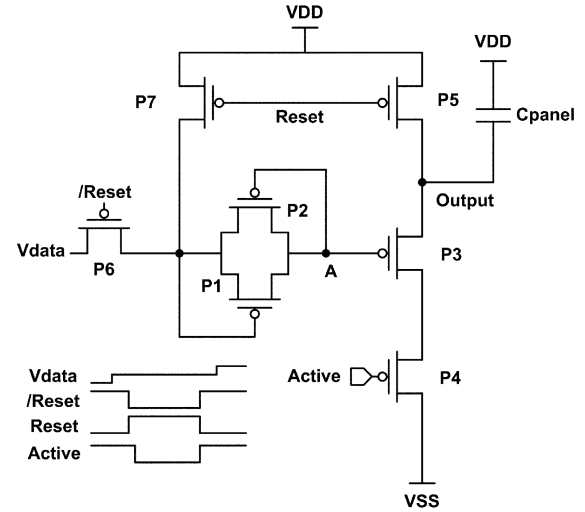


Fig. 3. Analog buffer of source follower with device matching technique and its timing diagram of operation [13].

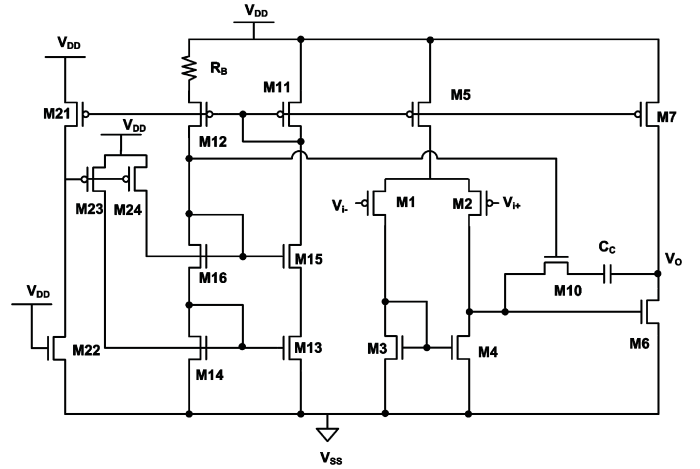


Fig. 4. Two-stage OP amp utilized for unity-gain analog output buffer [14].

proposed circuits utilize the DAC with gamma correction of 3-V liquid crystal (LC) specification, but it can also drive the 5-V liquid crystal with the desired 5-V gamma curve without re-designing the DAC with gamma correction parameters.

II. CONVENTIONAL ON-PANEL ANALOG OUTPUT BUFFERS

Source follower is one of the most popular analog output buffers integrated on the glass substrate for data driver due to its high input impedance and low output impedance. For such simple architecture, some drawbacks are found, such as smaller output swing and higher input offset voltage. Fig. 2(a) shows the conventional source follower of analog output buffer with active load [12]. The final output voltage (V_{out}) in Fig. 2(a) with different input voltage (V_{in}) is kept constant but has an offset voltage from the input level, in which the offset is determined mainly by the threshold voltage of the driving TFT. Besides, the threshold voltage may not be a constant in different panel locations due to the LTPS device variation. To balance the input offset voltage, Fig. 2(b) shows the modified source follower of analog output buffer with compensation capacitor. In the compensation period (1), S1 and S2 are turned on, so the voltage drop is stored in compensation capacitor (Cvt). In the data-input period (2), S1 and S2 are turned off while S3 and S4 are turned

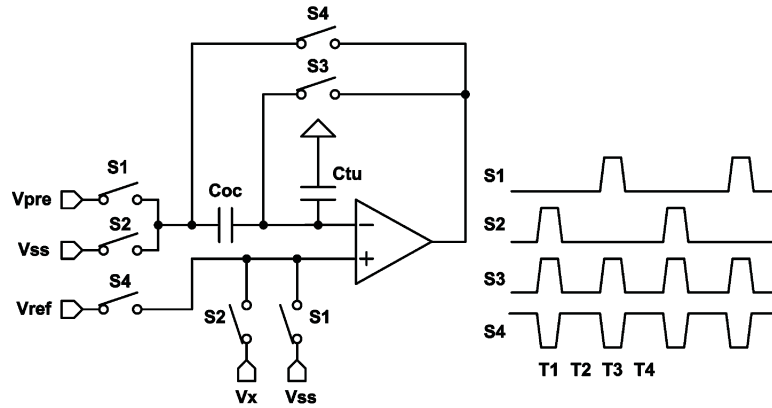


Fig. 5. Level-change analog amplifier [15].

on. At the meanwhile, the gate voltage of the driving TFT is applied with the voltage difference hold in C_{vt} added to the input voltage (V_{in}). Thus, the output voltage is compensated by the voltage stored in C_{vt} .

The offset voltage was decreased by the aforementioned compensation technique. However, the offset voltage, which is predominantly governed by the threshold voltage of TFT, may not be stored exactly in the capacitor due to the subthreshold leakage current. The subthreshold characteristic of poly-Si TFT is rather poor compared with well-known MOSFETs in the silicon CMOS technology, and the large subthreshold current of poly-Si TFTs increases the offset voltage of analog buffers [13]. In addition, compensation capacitor utilized in this technique may also consume larger area. Therefore, Fig. 3 shows the analog buffer of source follower type with device matching technique and its timing diagram of operation. When the reset signal (Reset) is low, the voltage in output loading capacitor (C_{panel}) is reset. The input signal (V_{data}) is applied when the Reset becomes high, so the voltage in node A (V_a) grows to $V_{data} + |V_{th}|$ due to the diode connection of P1. (V_{th} is the threshold voltage of p-type TFT.) After that, P4 is turned on with the active signal and V_a decreases due to bootstrapping effect, as well as V_{ss} is transferred to C_{panel} . As V_a decreases to $V_{data} - |V_{th}|$, diode-connected P2 is turned on to hold this voltage. Therefore, the source voltage of P3 is about V_{data} and the threshold voltage is compensated by device matching. This analog buffer with device matching technique can reduce the offset generated from the subthreshold current of poly-Si TFT, but without using additional capacitor to store the threshold voltage of a poly-Si TFT.

Compared with the analog output buffer of source follower type, the unity-gain analog output buffer with an OP amp has higher on-panel analog driving capability [14]. Fig. 4 shows the two-stage OP amp utilized for unity-gain analog output buffer with Miller compensation and nulling resistor (M10 and C_c). As a unity-gain buffer, the output node (V_o) is connected to the negative input node (V_{i-}) and the input signal is applied to the positive input node (V_{i+}). This output buffer comprises four parts as following. The 1st part consists of p-channel differential pair (M1 and M2) with n-channel current mirror load (M3 and M4) and a p-channel tail current source (M5). The second part is a

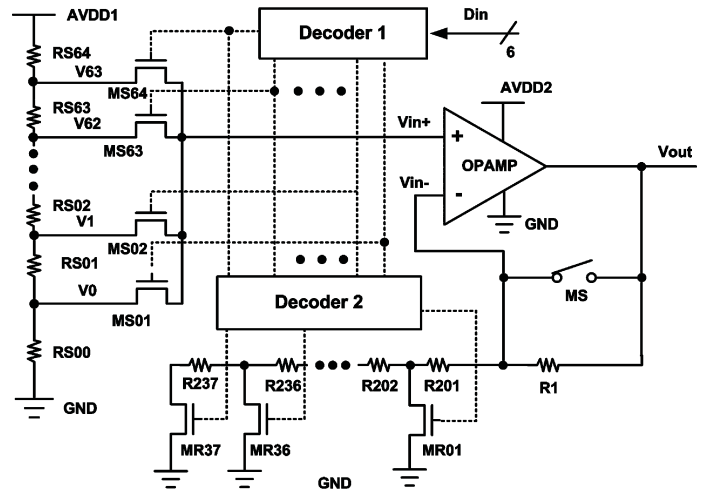
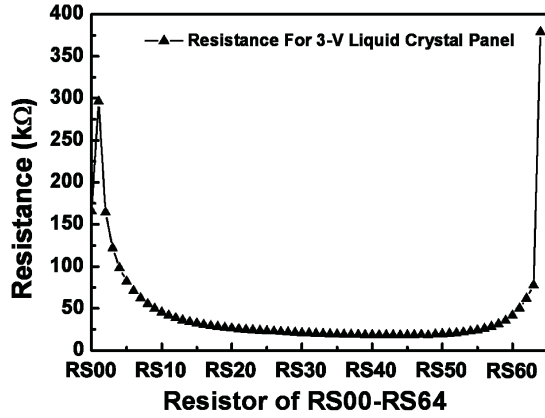


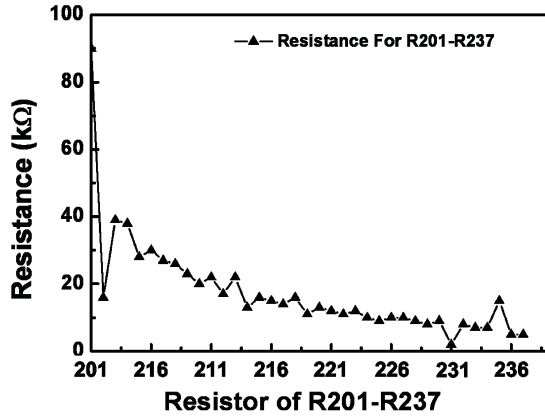
Fig. 6. New proposed analog output buffer I with level shifting function on glass substrate.

common-source amplifier stage (M6 and M7), which can improve the open-loop gain and reduce the input offset voltage. The 3rd part is a constant g_m bias circuit (M11–M16 and R_B), which can provide a more stable voltage reference. The fourth part is start-up circuit (M21–M24) to turn on the bias circuit in the beginning of power-on operation and be turned off after bias circuit working. The two stage OP amp has larger unity-gain frequency, better slew rate, lower input offset voltage, better immunity to noise, and more steady circuit performance, as comparing to the analog output buffer of source follower type. Furthermore, input offset can be further reduced by the larger open loop gain of OP amp.

Fig. 5 shows a level-change analog amplifier which maximizes monolithic circuit integration, in particular targeting the monolithic integration of high performance analog circuits [15]. This circuit consists of a differential amplifier, an offset-removing capacitor “Coc,” and one set of switches allowing connections to four voltages. At T1 and T3 period, Coc is precharged to voltage level determined by the switch settings. At T2 and T4 period, voltage level of V_{ref} is, therefore, shifted to the output decided by V_x and V_{ss} , where V_{ref} is corresponding to the image data for an LCD.



(a)



(b)

Fig. 7. Resistance utilized in the proposed circuit I for (a) RS00-RS64 and (b) R201-R237.

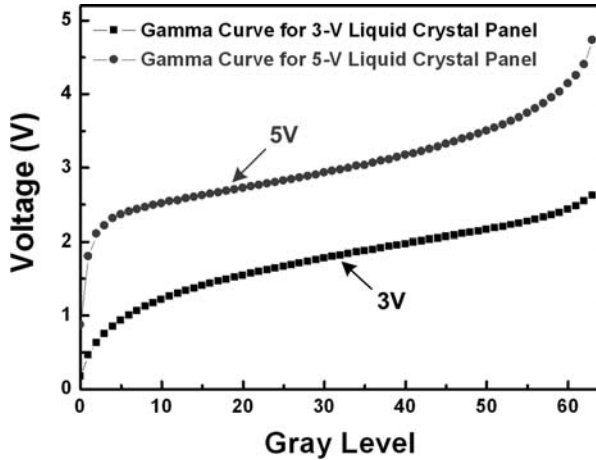


Fig. 8. Gamma curves for 3- and 5-V liquid crystal panels.

III. NEW PROPOSED ANALOG OUTPUT BUFFER WITH LEVEL SHIFTING FUNCTION

As mentioned above, DAC is used to convert the digital RGB signal to analog gray level with consideration of gamma correction. The LCD panel with larger panel size or higher resolution results in larger load to this signal, so the analog output buffer is essential to provide the driving capability of the data driver to drive the liquid crystal with appropriate analog gray level. In general, each liquid crystal under the selected operation voltage has its corresponding gamma curve. Therefore, for

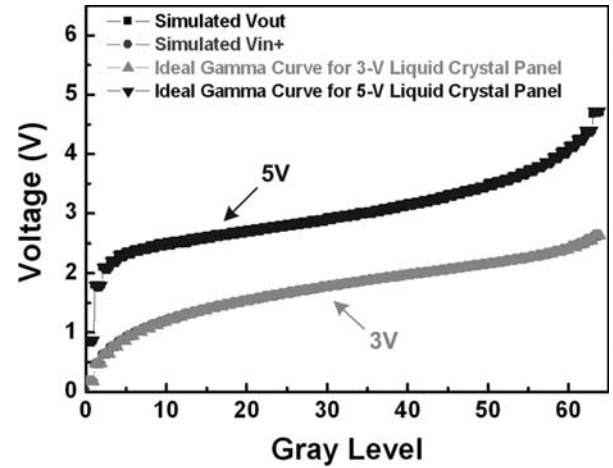


Fig. 9. Simulated gamma curves of the new proposed circuit I for the liquid crystal panel under 3-V or 5-V operations.

various liquid crystal displays, the DAC circuit is indispensable to be redesigned as well.

In this work, two new analog output buffers with level shifting function are proposed to realize the DAC with gamma correction of 3-V liquid crystal (LC) specification, and it can also drive the 5-V liquid crystal with the desired 5-V gamma curve without re-designing the DAC with 5-V gamma correction parameters. The OPAMP integrated in the two proposed analog output buffers with level shifting function is the same as that shown in Fig. 4. Fig. 6 shows the new proposed analog output buffer I with level shifting function on glass substrate for panel application in 3- μm LTPS technology with $\text{AVDD1} = 3\text{ V}$, $\text{AVDD2} = 6\text{ V}$, and $R1 = 400\text{ k}\Omega$. R-string (RS00–RS64) and decoder 1 with digital input code D_{in} are 6-bit R-string DAC circuit with gamma correction implemented by the R-string for 3-V liquid crystal panel application. When D_{in} is 000000, decoder 1 transforms the digital input code to only turn on MS01, and V_0 is assigned to V_{in+} of OPAMP in Fig. 6. In the meantime, all the other voltages ($V1$ – $V63$) are not transmitted to V_{in+} . Therefore, with proper digital input code, the corresponding voltage level can be correctly chosen to meet each gray level in V_{in+} for DAC circuit with gamma correction for 3-V liquid crystal panel application.

Fig. 7 shows the resistance utilized in the proposed circuit I for (a) RS00–RS64, which are provided by the LCD panel manufacturer, and (b) R201–R237, which are designed for converting 3-V gamma correction to 5-V application. Fig. 8 shows two gamma curves for the liquid crystal panel under different (3-V or 5-V) operating voltages. In Fig. 7(a), the larger resistance variation between RS63 and RS64 is to make $V_{63} = 2.61\text{ V}$, which is close to $\text{AVDD1} = 3\text{ V}$. In addition, RS01–RS05 also shows large resistance variation due to large voltage degradation from gray level 5 to 1 in Fig. 8. In order to meet gray level 0 close to 0 V, RS00 also shows larger resistance. In Fig. 7(b), R201 shows the largest resistance because the largest voltage variation happened at gray level 63 from converting 3-V to 5-V gamma correction. Besides, for liquid crystal under different operating voltages, such as 5-V display panel, the 5-V gamma curve is different to that under 3-V application. Since the applied voltages in each gray

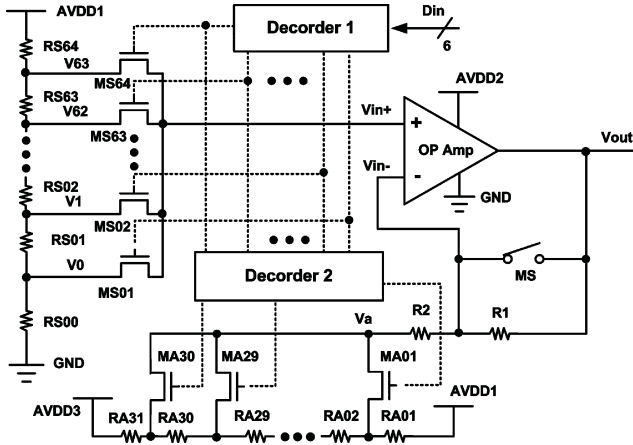


Fig. 10. New proposed analog output buffer II with level shifting function on glass substrate.

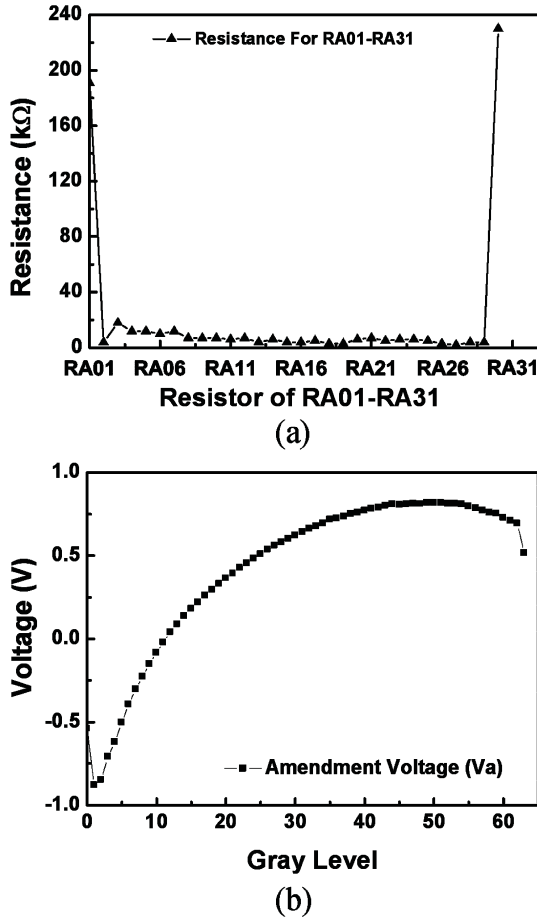


Fig. 11. (a) Resistance utilized in the proposed circuit II for RA01–RA31 and (b) the amendment voltage V_a in each gray level.

level for 5-V gamma curve cannot be simply derived from applied voltages for 3-V gamma curve by adding a constant or a linear transformation, the applied voltages for 3- and 5-V gamma curves show nonlinear relationship in each gray level. In the new proposed circuit I, 6-bit R-string DAC with gamma correction for 3-V liquid crystal display is not needed to be re-designed for 5-V operation. OPAMP, decoder 2, R1, R201–R237, and MR01–MR37 are proposed to operate the analog output buffer with level shifting function to meet 5-V

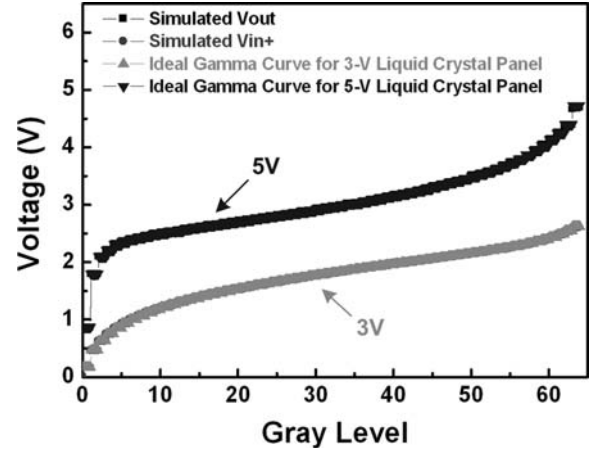


Fig. 12. Simulated gamma curves of the new proposed circuit II for the liquid crystal panel under 3-V or 5-V operations.

operation. Decoder 2 receives the input signal from decoder 1 to turn on only one switch of MR01–MR37 at the same time. For example, if MR01 is turned on, the OPAMP behaves like an non-inverting amplifier with it function shown as

$$V_{out} = V_{in} \left(1 + \frac{R1}{R201} \right) \quad (1)$$

where $V_{in} = V_{in+} = V_{in-}$ if the gain of OPAMP is large enough. Therefore, with suitable design of R201–R237, gamma curve for 5-V liquid crystal panel can be achieved without re-designing the 6-bit R-string DAC that has been realized with 3-V gamma correction parameters. Fig. 9 shows the simulated gamma curves of the proposed circuit in a 3- μm LTPS technology for liquid crystal panel under 3- or 5-V operations. V_{in+} is the output gamma curve of 3-V liquid crystal panel and V_{out} is the output gamma curve of 5-V liquid crystal panel.

In the proposed circuit I, the level shifting function is strongly depended on the absolute value of resistors (R201–R237). Although LTPS process with enlarged poly-grain size can improve device performance, it usually accompanies a random device-to-device variation on LCD panel. The harmful effects of irregular grain boundaries, gate-insulator interface defects, and incomplete ion-doping activation in thin poly-silicon channels often result in the variation on electrical characteristics of LTPS devices [16]. The absolute value of resistors (R201–R237) is therefore easily not well consistent to the simulated result after fabrication. Therefore, Fig. 10 shows the new proposed analog output buffer II with level shifting function on glass substrate for panel application in 3- μm LTPS technology with AVDD1 = 3 V, AVDD2 = 6 V, AVDD3 = -3 V, and R1 = R2 = 900 k Ω . The main idea of proposed circuit II is similar to the proposed circuit I but the level shifting function is modified below

$$V_{out} = V_{in} \left(1 + \frac{R1}{R2} \right) - V_a \left(\frac{R1}{R2} \right) \quad (2)$$

where V_a is the amendment voltage derived from RA01–RA31 and MA01–MA30. The operation of the proposed circuit II is similar to that of the proposed circuit I in the former part and RS00–RS64 are the same as that in the proposed circuit I. Nevertheless, when decoder 2 receives the input signal from

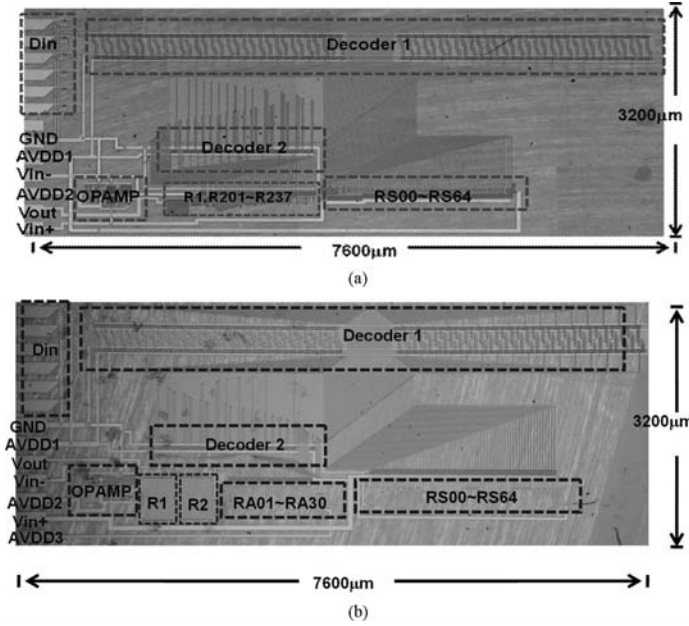


Fig. 13. Die photo of the fabricated (a) analog output buffer I and (b) analog output buffer II, with level shifting function on glass substrate in a $3\text{-}\mu\text{m}$ LTPS technology.

decoder 1, only one switch of MA01–MA37 is turned on at the same time. Therefore, suitable amendment voltage V_a is decided by the ratio of RA01–RA31. Fig. 11 shows (a) resistance utilized in the proposed circuit II for RA01–RA31 and (b) the amendment voltage V_a in each gray level for converting the 3-V gamma correction to 5-V application. In Fig. 11(a), RA01 and RA31 show the larger resistance because the amendment voltage is varied from -1 V to 1 V but AVDD3 is -3 V as well as AVDD1 is 3 V . In the proposed circuit II, the RA01–RA31 has guaranteed monotonicity to result in higher accuracy of amendment voltage V_a , because the accuracy of V_a is dependent on the ratio of resistors, not dependent on absolute resistor values. Fig. 12 shows the simulated gamma curves of the proposed circuit II in a $3\text{-}\mu\text{m}$ LTPS technology for liquid crystal panel under 3- or 5-V operations. V_{in+} is the output gamma curve of 3-V liquid crystal panel and V_{out} is the output gamma curve of 5-V liquid crystal panel. Finally, in Figs. 6 and 10, the switch MS is utilized to control the proposed circuits to be operated under 3- or 5-V application. For 5-V application, the switch MS is open, so the proposed circuits can be performed just like mentioned above. For 3-V application, the switch MS is shorted, so the output of OPAMP (V_{out}) is connected to the negative input of OPAMP (V_{in-}) to perform like a non-inverting amplifier. Therefore, the proper 3-V gamma value (V_0 – V_{63}) can be transformed to output (V_{out}) correctly.

IV. EXPERIMENTAL RESULTS AND DISCUSSION

The new proposed circuits have been designed and fabricated in a $3\text{-}\mu\text{m}$ LTPS technology. Fig. 13 shows the die photo of the fabricated analog output buffer I and analog output buffer II with level shifting function on glass substrate, where the area is $3200\text{ }\mu\text{m} \times 7600\text{ }\mu\text{m}$. Fig. 14 shows the measured results in V_{out} and its variation for the proposed circuit I with gamma

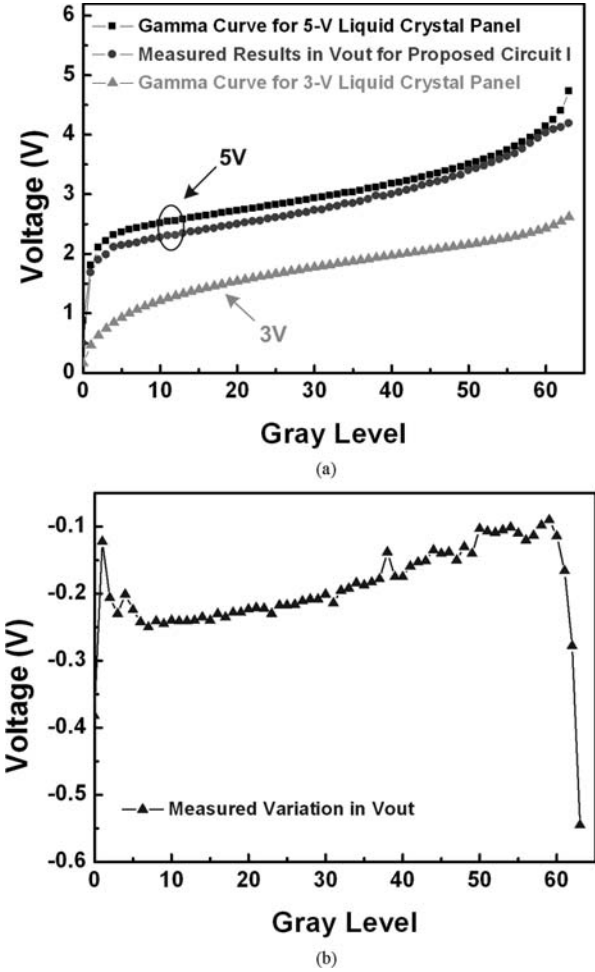


Fig. 14. Measured results for the new proposed circuit I in (a) V_{out} and (b) its variation with gamma curve for 5-V liquid crystal panel but designed with the resistance ratio of 3-V gamma correction.

curve for 5-V liquid crystal panel but designed with the resistance ratio of 3-V gamma correction. Somewhat, the measured result with its variation from -0.1 V to -0.6 V is not so well matching with the simulated result due to the variation of on-glass resistance after fabrication in LTPS process. Suitable adjustment on the layout of R-string resistance in the LTPS process, a more precise result of the proposed circuit I can be achieved. Fig. 15 shows three different layouts in resistor. The two contacts of a serpentine resistor should reside as close to one another as possible to minimize the impact of thermoelectrics. The serpentine layout style in Fig. 15(a) has large thermal variations due to an excessive separation between its contacts. In Fig. 15(b), the layout reduces thermal variability and improves matching by bringing the resistor heads into closer proximity. However, this layout is vulnerable to misalignment errors. If the resistor body shifts downward relative to the resistor heads, then the length of the resistor increases by twice the misalignment. This vulnerability can be eliminated by the layout style in Fig. 15(c) [17]. Fig. 16 shows measured results in V_{out} and its variation for the proposed circuit II with gamma curve for 5-V liquid crystal panel but designed with the resistance ratio of 3-V gamma correction. As mentioned above, RA01–RA31 has guaranteed monotonicity to result in higher accuracy of amendment voltage V_a , because the accuracy of V_a is dependent on

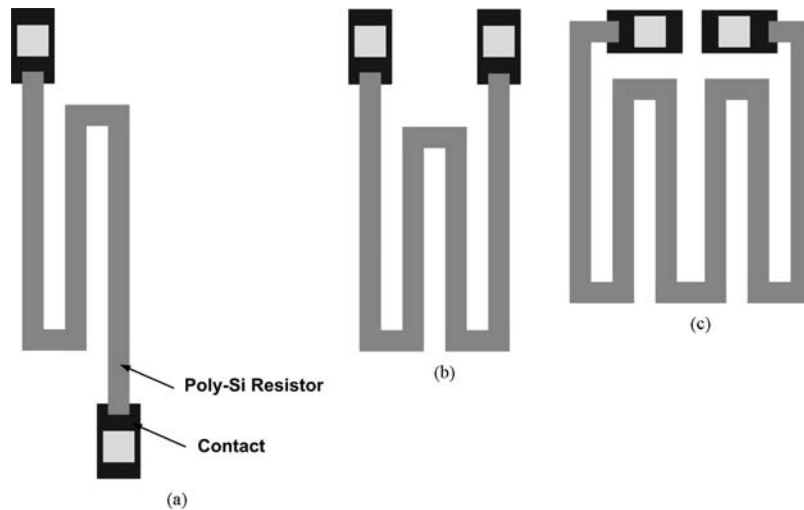


Fig. 15. Three different layouts to realize resistor.

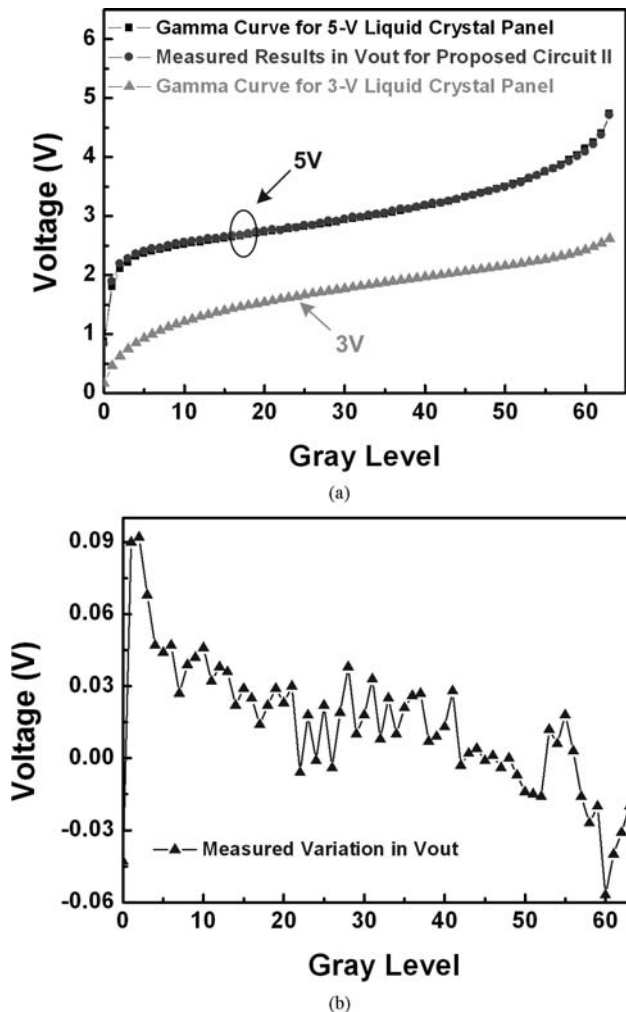


Fig. 16. Measured results for the new proposed circuit II in (a) V_{out} and (b) its variation with gamma curve for 5-V liquid crystal panel but designed with the resistance ratio of 3-V gamma correction.

the ratio of resistors, not dependent on absolute resistor values. The measured results in the proposed circuit II show better consistent and much smaller variation (about -0.06 V to 0.1 V) to the ideal gamma curve with gamma value of 2.2. However, the proposed circuit II requires another supply voltage AVDD3.

V. CONCLUSION

Two analog output buffers with level shifting function on glass substrate for panel application has been successfully designed and fabricated in a $3\text{-}\mu\text{m}$ LTPS technology. By using OPAMP, decoder 2, R1, R201–R237, MR01–MR37, and DAC with 3-V gamma correction parameters, the new proposed analog output buffer I can drive 5-V liquid crystal panel without re-designing the DAC with 5-V gamma correction parameters. By utilizing amendment voltage V_a derived from RA01–RA31 and MA01–MA30, the measured results in the new proposed analog output buffer II show better consistent to ideal gamma curve with gamma value of 2.2.

REFERENCES

- [1] Y.-H. Tai, *Design and Operation of TFT-LCD Panels*. : Wu-Nan Book, Inc, 2006.
- [2] C.-S. Tan, W.-T. Sun, S.-H. Lu, C.-H. Kuo, S.-H. Yeh, I.-T. Chang, C.-C. Chen, J. Lee, and C.-S. Yang, "A fully integrated poly-Si TFT-LCD adopting a novel 6-Bit source driver and a novel DC-DC converter circuit," in *SID Dig. Tech.*, 2004, pp. 1456–1459.
- [3] Y.-S. Park, D.-Y. Kim, K.-N. Kim, Y. Matsueda, J.-H. Choi, H.-K. Kang, H.-D. Kim, H.-K. Chung, and O.-K. Kwon, "An 8b source driver for 2.0 inch full-color active-matrix oleds made with LTPS TFTs," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2007, pp. 130–132.
- [4] W.-Y. Guo, C.-Y. Meng, A. Shih, and Y.-M. Tsai, "Reliability of low temperature poly-Si thin film transistor," in *IDMC Tech. Dig.*, 2003.
- [5] S.-C. Huang, G.-F. Peng, J.-L. Chern, and Y.-H. Tai, "Statistical investigation on the variation behavior of low-temperature poly-Si TSTS for circuit simulation," in *SID Dig. Tech.*, 2006, pp. 329–332.
- [6] S.-S. Han, K.-M. Lim, J.-S. Yoo, Y.-S. Jeong, K.-E. Lee, J.-K. Park, D.-H. Nam, S.-W. Lee, J.-M. Yoon, Y.-H. Jung, H.-S. Seo, and C.-D. Kim, "3.5 inch QVGA low-temperature poly-Si TFT LCD with integrated driver circuits," in *SID Dig. Tech.*, 2003, pp. 208–211.
- [7] M.-D. Ker, C.-K. Deng, and J.-L. Huang, "On-panel output buffer with offset compensation technique for data driver in LTPS technology," *IEEE J. Display Tech.*, vol. 2, no. 2, pp. 153–159, Jun. 2006.
- [8] J.-S. Chen and M.-D. Ker, "New gate-bias voltage-generating technique with threshold-voltage compensation for on-glass analog circuits in LTPS process," *J. Display Technol.*, vol. 3, no. 3, pp. 309–314, Sep. 2007.
- [9] H. Tokioka, M. Agari, M. Inoue, T. Yamamoto, H. Murai, and H. Nagata, "Low power consumption TFT-LCD with dynamic memory embedded in pixels," in *SID Dig. Tech.*, 2001, pp. 280–283.
- [10] M. Senda, Y. Tsutsui, R. Yokoyama, K. Yoneda, S. Matsumoto, and A. Sasaki, "Ultra-low-power polysilicon AMLCD with full integration," in *SID Dig. Tech.*, 2002, pp. 790–793.

- [11] B. Lee, Y. Hirayama, Y. Kubota, S. Imai, A. Imai, M. Katayama, K. Kato, A. Ishikawa, T. Ikeda, Y. Kurokawa, T. Ozaki, K. Mutaguch, and S. Yamazaki, "A CPU on a glass substrate using CG-silicon TFTS," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2003, Feb. 2003, pp. 164–165.
- [12] C.-C. Pai and Y.-H. Tai, "A novel analogue buffer using poly-Si TFTS for active matrix displays," in *IDMC Tech. Dig.*, 2005, pp. 483–486.
- [13] S.-H. Jung, W.-J. Nam, J.-H. Lee, and M.-K. Han, "A new analog buffer using P-type poly-Si TFTS for active matrix displays," *IEEE Electron Devices Lett.*, vol. 27, pp. 40–42, Jan. 2006.
- [14] Y.-H. Li, M.-D. Ker, C.-Y. Huang, and C.-Y. Hsu, "On-panel analog output buffer for data driver with consideration of device characteristic variation in LTPS technology," in *Asia Display Tech. Dig.*, 2007, vol. 1, pp. 210–215.
- [15] K. Maeda, T. Nagai, T. Sakai, N. Kuwabara, S. Nishi, M. Satoh, T. Matsuo, S. Kamiya, H. Katoh, M. Ohue, Y. Kubota, H. Komiya, T. Muramatsu, and M. Katayama, "The system-LCD with monolithic ambient-Light sensor system," in *SID Dig. Tech.*, 2005, pp. 356–359.
- [16] Y.-H. Tai, S.-C. Huang, W.-P. Chen, Y.-T. Chao, and G.-F. Peng, "A statistical model for simulating the effect of LTPS TFT device variation for SOP applications," *J. Display Tech.*, vol. 3, no. 4, pp. 426–433, Dec. 2007.
- [17] A. Hastings, *The Art of Analog Layout*. Upper Saddle River, NJ: Prentice-Hall, 2001.



Tzu-Ming Wang (S'06) was born in Taiwan, in 1982. He received the B.S. degree from the Department of Electronics Engineering, National Chiao-Tung University, Hsinchu, Taiwan, in 2005. He is currently working toward the Ph.D. degree at the Institute of Electronics, National Chiao-Tung University.

His current research interests include analog circuit design on glass substrate and mixed-voltage I/O circuit design in low-voltage CMOS technology.



Ming-Dou Ker (S'92–M'94–SM'97–F'08) received the Ph.D. degree from the Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan, in 1993.

During 1994–1999, he worked in the VLSI Design Division, Computer and Communication Research Laboratories, Industrial Technology Research Institute (ITRI), Hsinchu, Taiwan. Since 2004, he has been a Full Professor with the Department of Electronics Engineering and Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan.

From 2006 to 2008, he served as the Director of Master Degree Program in the College of Electrical Engineering and Computer Science, National Chiao-Tung University, as well as the Associate Executive Director of the National Science and Technology Program on System-on-Chip, Taiwan. In 2008, he was rotated to be a Chair Professor and Vice President of I-Shou University, Kaohsiung, Taiwan. In the field of reliability and quality design for circuits and systems in CMOS technology, he has published over 370 technical papers in international journals and conferences. He has proposed many inventions to improve the reliability and quality of integrated circuits, which have been granted with 146 U.S. patents and 145 R.O.C. (Taiwan) patents. His current research interests include reliability and quality design for nanoelectronics and gigascale systems, high-speed and mixed-voltage I/O interface circuits, on-glass circuits for system-on-panel applications, and biomimetic circuits and systems for intelligent prosthesis. He had been invited to teach or to consult reliability and quality design for integrated circuits by hundreds of design houses and semiconductor companies in the worldwide IC Industry.

Prof. Ker has served as the member of Technical Program Committees and the Session Chair of numerous international conferences. He ever served as the Associate Editor for the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS. He has been selected as the Distinguished Lecturer in the IEEE Circuits and Systems Society (2006–2007) and in the IEEE Electron Devices Society (2008–2009). He was the President of Foundation in Taiwan ESD Association. In 2009, he was selected as one of the top ten Distinguished Inventors in Taiwan; and one of the Top Hundred Distinguished Inventors in China. In 2008, he has been elevated as an IEEE Fellow with the citation of "for contributions to electrostatic protection in integrated circuits, and performance optimization of VLSI micro-systems".



Sao-Chi Chen was born in Taiwan, in 1982. He received M.S. degree from the Industrial Technology R & D Master Program on IC Design of ECE College, National Chiao-Tung University, Hsinchu, Taiwan, in 2008.

In 2008, he joined the Product Design and Engineering Center Macronix International Co., Ltd. (MXIC), as a Senior Engineer. His current research interests include driving circuits integrated on panel for flat panel display applications.