Design of Power-Rail ESD Clamp Circuit With Ultra-Low Standby Leakage Current in Nanoscale CMOS Technology

Chang-Tzu Wang, *Student Member, IEEE*, and Ming-Dou Ker, *Fellow, IEEE*

***Abstract*—An ultra-low-leakage power-rail ESD clamp circuit, composed of the SCR device and new ESD detection circuit, has been proposed with consideration of gate current to reduce the standby leakage current. By controlling the gate current of the devices in the ESD detection circuit under a specified bias condition, the whole power-rail ESD clamp circuit can achieve an ultra-low standby leakage current. The new proposed circuit has been fabricated in a 1 V 65 nm CMOS process for experimental verification. The new proposed power-rail ESD clamp circuit can achieve 7 kV HBM and 325 V MM ESD levels while consuming only a standby leakage current of 96 nA at 1 V bias in room temperature and occupying an active area of only 49 μm $\times$ 21 μm.**

***Index Terms*—Electrostatic discharge (ESD), gate leakage, power-rail ESD clamp circuit, silicon controlled rectifier (SCR).**

I. Introduction

With the decrease of the power supply voltage for low power applications, the thickness of the gate oxide has been also scaled down in the nanometer CMOS technologies. However, such a thin gate oxide of only $\sim$2 nm in advanced CMOS technology has been reported to result in a substantial fraction of the overall leakage current in the chip due to its gate leakage current [1]. In 45-nm generation and beyond, the metal gate technology is therefore applied to reduce the gate leakage current [2]. Nevertheless, the gate leakage issue still exists in the 90-nm and 65-nm technologies which are currently used in production without metal gate structure. The gate current has been modeled in BSIM4 MOSFET model, and the foundries have also provided the corresponding SPICE models of nanometer CMOS processes to circuit designers. Recently, some work has been reported on how to reduce the gate leakage current for digital circuits in advanced CMOS processes [3], [4].

Manuscript received August 07, 2008; revised November 17, 2008. Current version published February 25, 2009. This work was supported by National Science Council (NSC), Taiwan, R.O.C. under Contract NSC 97-2221-E-009-170, partially supported by Ministry of Economic Affairs, Taiwan, under Grant 97-EC-17-A-01-S1-104, and partially supported by United Microelectronic Corporation, Taiwan, R.O.C.

C.-T. Wang is with the Nanoelectronics and Gigascale Systems Laboratory, Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan. He is also with the ESD Engineering Department, United Microelectronics Corporation, Hsinchu, Taiwan (e-mail: ctwang@ieee.org).

M.-D. Ker is with the Nanoelectronics and Gigascale Systems Laboratory, Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan. He is also with the Department of Electronic Engineering, I-Shou University, Kaohsiung, Taiwan (e-mail: mdker@ieee.org).

Digital Object Identifier 10.1109/JSSC.2008.2012372

From the perspective on commercial IC products, to achieve the electrostatic discharge (ESD) specification is necessary for product qualification. The power-rail ESD clamp circuit to effectively protect the core circuits is traditionally implemented by RC-based ESD protection structure with a large-sized ESD clamping MOSFET [5]. Such a traditional RC-based ESD clamp circuit is shown in Fig. 1(a). However, the gate leakage current caused from the large-sized MOSFET ($\mathrm{M_{ESD}}$) and the MOS capacitor (Mc) in the traditional power-rail ESD clamp circuit becomes serious in nanoscale CMOS processes. For example, the gate current flowing through a MOS capacitor with W/L of 5 μm/5 μm under 1-V bias is as large as 2 μA in a 65-nm CMOS process. The leakage currents of MOS capacitors with different dimensions under 1-V bias in 90-nm and 65-nm CMOS processes are listed and compared in Table I. With such a leakage current in the MOS capacitor, the ESD clamping MOSFET ($\mathrm{M_{ESD}}$) cannot be completely turned off under the power-on condition due to the malfunction of the ESD detection circuit caused by gate leakage current and in turn to induce extra large leakage current through $\mathrm{M_{ESD}}$. Such a leaky ESD protection circuit is barely tolerable in portable products with low power requirements. High-voltage-tolerant power-rail ESD clamp circuits with only thin-oxide devices have been reported to overcome the gate-oxide reliability issue [6]–[8]. However, the prior designs did not consider the effect of gate leakage current if such circuits are further implemented in nanometer CMOS processes. To solve the problem of malfunction in the traditional RC-based ESD detection circuit, the modified ESD clamp circuit with the timer level restorer was ever reported as that re-drawn in Fig. 1(b) [9]. But, the experimental result in that work still showed a high standby leakage current in the order of several micro-amperes in a 130-nm CMOS process at a high temperature of 125 °C [9]. New designs of the power-rail ESD clamp circuit need to be developed to further reduce such standby leakage current in nanometer CMOS processes.

In this work, a power-rail ESD clamp circuit with ultra-low standby leakage current is proposed. The new proposed ESD clamp circuit has an efficient ESD detection circuit to improve the turn-on efficiency of the ESD clamping device. By using the new proposed circuit solution with only thin gate-oxide devices, the standby leakage current of the proposed power-rail ESD clamp circuit can be successfully reduced under the normal circuit operating condition. The proposed power-rail ESD clamp circuit has been successfully verified in a 1-V 65-nm CMOS process.

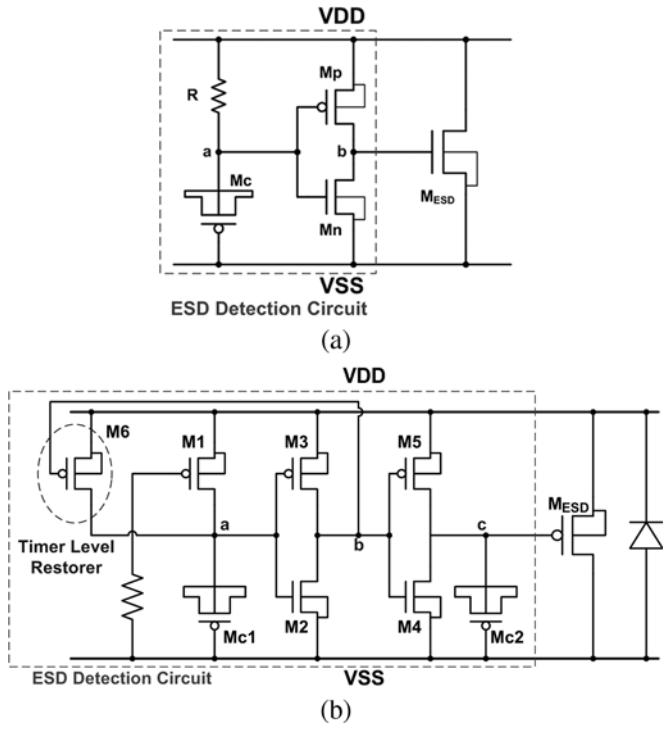


Fig. 1. (a) The traditional RC-based power-rail ESD clamp circuit [5]. (b) The modified power-rail ESD clamp circuit with timer level restorer [9].

TABLE I
GATE CURRENT OF MOS CAPACITOR UNDER 1-V BIAS IN DIFFERENT CMOS TECHNOLOGIES

Process	Dimension	
	5μm/5μm	10μm/10μm
90nm	61.3nA	247nA
65nm	2.04μA	8.32μA

II. POWER-RAIL ESD CLAMP CIRCUIT WITH CONSIDERATION OF GATE LEAKAGE CURRENT

A. Gate Leakage Current in Nanoscale CMOS

The gate leakage current cannot be neglected when the gate oxide thickness is scaled down to 3 nm and below. In BSIM4 model [10], the components of gate tunneling current include the tunneling current between gate and bulk (Igb), the current between gate and channel (Igc), and the current between gate and source/drain diffusion regions (Igs and Igd).

For a MOS capacitor, the source, drain, and bulk terminals are connected to the same node. Therefore the total gate-to-source current $(Igcs + Igs)$, the total gate-to-drain current $(Igcd + Igd)$, and the gate-to-bulk current (Igb) of a MOS capacitor with W/L of 5 μm/5 μm can be simulated with foundry provided SPICE parameters. The corresponding currents are 1.02 μA, 1.02 μA, and 89 pA, respectively, in a 65-nm CMOS process under 1-V bias. Compared with gate-to-source current and gate-to-drain current, the component of gate-to-bulk current in a MOS capacitor is quite small in comparison to the simulated results.

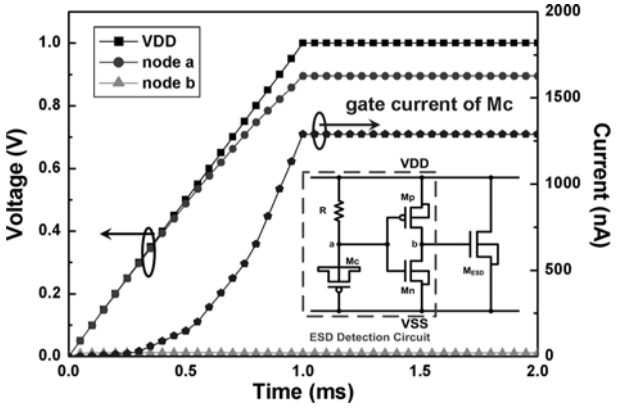


Fig. 2. HSPICE-simulated voltage on the nodes of the ESD detection circuit and the gate current flow through the MOS capacitor Mc in the traditional RC-based power-rail ESD clamp circuit under the normal power-on condition with VDD of 1 V in a 65-nm CMOS process.

B. Traditional RC-Based ESD Clamp Circuit With Gate Current Consideration

The traditional RC-based ESD clamp circuit is shown in Fig. 1(a). Based on BSIM4 gate current model, the MOS capacitor with a large-sized gate oxide will induce a large amount of gate current from node a to VSS under the normal circuit operating condition. Such gate current causes a voltage drop across the resistor R, and therefore the PMOS Mp in the ESD detection circuit cannot be completely turned off. With a non-turned-off PMOS, node b is charged up to some voltage level higher than VSS, and that in turn causes the main ESD clamping MOSFET $(\mathrm{M_{ESD}})$ operating in sub-threshold region under the normal circuit operating condition. The ESD clamping MOSFET $(\mathrm{M_{ESD}})$ drawn with large device dimension in sub-threshold region further generates a large amount of standby leakage current.

Fig. 2 shows the Hspice-simulated voltages on the nodes of the ESD detection circuit and the gate current of the MOS capacitor Mc under the normal power-on condition with a rise time of 1 ms in a 65-nm CMOS process. The dimensions of R, Mc, Mp, and Mn are 60 kΩ, 5 μm/5 μm, 80 μm/0.12 μm, and 5 μm/0.12 μm. When the VDD reaches 1 V, the gate current of Mc is as large as 1290 nA, so that the voltage level at node a cannot reach 1 V due to the voltage drop across R. The PMOS Mp with a Vsg of $\sim$0.1 V cannot be fully turned off and in turn a leakage current path is generated from VDD through the inverter (Mp and Mn) to VSS. The ESD clamping MOSFET with several hundred micro-meters device width in sub-threshold region will cause a considerable leakage current of several micro-Amperes under the normal circuit operating condition with VDD of 1 V in a 65-nm CMOS process.

C. Modified ESD Clamp Circuit With Gate Current Consideration

To solve the malfunction of the ESD detection circuit that results in a large amount of leakage current from the ESD

TABLE II
DIMENSIONS OF DEVICES IN THE ESD DETECTION CIRCUIT OF THE MODIFIED ESD CLAMP CIRCUIT WITH TIMER LEVEL RESTORER FOR HSPICE SIMULATION

Devices	Dimension (W/L)
Mc1	5μm/5μm
Mc2	5μm/5μm
M1	0.3μm/20μm
M2	5μm/0.12μm
M3	10μm/0.12μm
M4	20μm/0.12μm
M5	5μm/0.12μm
M6	0.3μm/20μm

clamping MOSFET $(\mathrm{M_{ESD}})$ in sub-threshold region, one modified design with the additional timer level restorer was reported in Fig. 1(b) [9]. Under the normal power-on condition, node a is initially pulled high by the turned-on PMOS M1. However, with a leaky gate MOS capacitor Mc1, node a cannot be pulled to a full VDD voltage level. Afterward node b is pulled down to VSS by NMOS M2 and in turn the timer level restorer can be turned on, pulling node a to a full VDD voltage level. Therefore, the function of the ESD detection circuit is guaranteed to keep the main ESD clamping MOSFET $(\mathrm{M_{ESD}})$ in off state under the normal circuit operating condition. However, node a in this ESD detection circuit is kept at the voltage level of VDD, so that the voltage difference between the gate and bulk of MOS capacitor Mc1 still causes a significant leakage current path from VDD through M1 and Mc1 to VSS in nanoscale CMOS process.

From HSPICE simulation result based on BSIM4 model, under the normal operating condition with VDD of 1 V, the standby leakage current in the ESD detection circuit of Fig. 1(b) is around 1.5 μA at 25 °C in a 65-nm CMOS process, where the dimensions of devices are chosen appropriately and listed in Table II. The simulation result excludes the leaky large-sized ESD clamping MOSFET $(\mathrm{M_{ESD}})$. Even if the timer level restorer can solve the malfunction problem in the ESD detection circuit, the standby leakage current of such modified power-rail ESD clamp circuit is still too large for portable application with low-power requirements.

To overcome the gate leakage current in the thin gate oxide, one solution is to use the thick gate-oxide device to implement the MOS capacitor in the ESD detection circuit. In this work, a power-rail ESD clamp circuit designed with only thin gate-oxide devices to achieve ultra-low standby leakage current is proposed. By using the new proposed circuit solution with only thin gate-oxide devices, the standby leakage current of the power-rail ESD clamp circuit can be successfully reduced under the normal circuit operating condition.

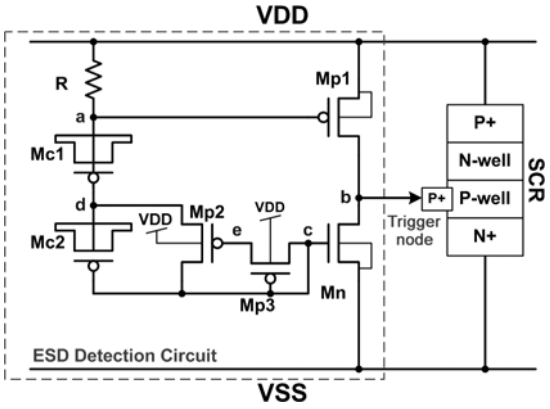


Fig. 3. The proposed ultra-low-leakage power-rail ESD clamp circuit with p-type substrate-triggered SCR device as ESD clamp device, where the ESD detection circuit is designed with consideration of gate leakage current.

III. NEW PROPOSED ULTRA-LOW-LEAKAGE POWER-RAIL ESD CLAMP CIRCUIT

The proposed ultra-low-leakage power-rail ESD clamp circuit is shown in Fig. 3. The p-type substrate-triggered silicon-controlled rectifier (SCR) device is used as the main ESD clamping device [11]. The SCR device, which is composed of cross-coupled n-p-n and p-n-p BJTs with regenerative feedback loop, with a low holding voltage can sustain a high ESD level within a small silicon area in CMOS process. Moreover, the SCR device without poly gate structure has good immunity against the gate leakage problem. However, there are some disadvantages of using the SCR device as the ESD clamp device, such as the slow turn-on speed and the high triggered voltage. Therefore, the ESD detection circuit is used to improve the turn-on speed of the SCR device with substrate-triggered design. The new ESD detection circuit is designed with consideration of the gate current in this work. Utilizing the gate current to bias the ESD detection circuit and to reduce the voltage difference across the gates of the MOS capacitors, the gate leakage current through the MOS capacitor under the normal circuit operating condition can be further reduced. The total leakage current resulted from the MOS capacitor in the ESD detection circuit can be minimized. Therefore, the leakage currents through the ESD clamping device and the ESD detection circuit can be well controlled and minimized by this new proposed design.

In the proposed ESD detection circuit, the PMOS Mp1 is used as substrate driver to generate the substrate-triggered current into the trigger node of the SCR device during the ESD stress event, but Mp1 is kept off under the normal circuit operating condition. The NMOS Mn is used to keep the voltage level at the trigger node (node b in Fig. 3) at VSS, so the ESD clamping device (SCR) is guaranteed to be turned off during the normal circuit operating condition. The RC time constant from R, Mc1, Mc2, and the parasitic gate capacitance of Mn is designed around the order of $\sim \mu$s to distinguish ESD stress event from the normal power-on condition. The diode-connected Mp2 and Mp3 are acted as a start-up circuit with initial gate-to-bulk current from VDD into the ESD detection circuit, and in turn to conduct some gate current of Mc1 to bias the nodes c, d,

and e. After that, the voltage level at node d will be biased at a voltage level to reduce the voltage difference across the gate of Mc1 and to minimize the gate leakage current through the MOS capacitors.

The gate voltage of Mn should be designed higher than its threshold voltage under the normal circuit operating condition. Realized in a 65-nm CMOS process with VDD of 1 V, the voltage level at node c is chosen as 0.45 V to keep Mn in turned-on state but without generating too much gate leakage current from node c to VSS under the normal circuit operating condition. While designing the dimensions of the devices in the ESD detection circuit, the voltage levels at node a and node b are assumed to be kept at VDD and VSS, respectively, under the normal circuit operating condition. With consideration of the RC time constant, Mc1 and Mc2 are designed with the same device dimension, so that the voltage level at the node d is chosen as 0.7 V. The gate current of Mc1 will be slightly larger than that of Mc2, and the different parts of the gate current can be conducted by Mp2. From Kirchhoff's Current Law, the current equation at the node c, d, and e can be expressed as

$$Igd_{Mn} + Igs_{Mn} = Isg_{Mc2} + Idg_{Mc2} + Id_{Mp2} + Igd_{Mp2} + Id_{Mp3} + Isg_{Mp3}, \quad (1)$$

$$Isg_{Mc1} + Idg_{Mc1} = Isg_{Mc2} + Idg_{Mc2} + Id_{Mp2} + Isg_{Mp2}, \text{ and} \quad (2)$$

$$Isg_{Mp2} = Id_{Mp3} + Isg_{Mp3}, \quad (3)$$

where Igd_{Mn} means the total gate-to-drain current of Mn including $Igcd$ and Igd defined in [10]. The total gate current of Mc1 is equal to the total gate current through the oxide of Mn, which can be derived as

$$Isg_{Mc1} + Idg_{Mc1} = Igd_{Mn} + Igs_{Mn}. \quad (4)$$

The voltage differences between the source and drain (Vds) of both Mc1 and Mn are 0 V, so that the gate-to-drain current and the gate-to-source current should be the same. Therefore, (4) can be simplified to the component of only gate-to-source current for Mc1 and Mn, which can be derived as

$$Isg_{Mc1} = Igs_{Mn}. \quad (5)$$

The total gate-to-source current of Mc1 (Isg_{Mc1}) in the (5) can be solved by the given voltage Vsg_{Mc1} of 0.3 V with the device parameters provided from foundry, which can be roughly calculated as

$$Isg_{Mc1} \approx W_{eff} \cdot (L_{eff} \cdot 492 + 3 \times 10^{-5})(\text{A}). \quad (6)$$

With consideration of the RC time constant, the W/L of MOS capacitor Mc1 is chosen as 5 μm/5 μm, and the total gate-to-source current of Mc1 can be determined by (6). Therefore, the device dimension of Mn can also be determined by (5). Likewise, the dimension of each device in the proposed ESD detection circuit can be derived through the (1)–(3). With fine tuning on the voltage level at the nodes c, d, and e to achieve a minimized overall standby leakage current, the final dimension for each device in the proposed ESD detection circuit implemented in a given 65-nm CMOS process is shown in Table III, where the device dimension of Mp1 can be adjusted with different triggering current capability to turn on the main ESD clamping device (SCR). With a large device dimension of Mp1, the substrate-triggered current generated by Mp1 can be increased to accelerate the turn-on speed of the SCR device during ESD event. The discussion on the design flexibility is described in Section IV.

TABLE III
DIMENSIONS OF DEVICES IN THE ESD DETECTION CIRCUIT OF THE PROPOSED POWER-RAIL ESD CLAMP CIRCUIT

Devices	Dimension (W/L)
Mc1	5μm/5μm
Mc2	5μm/5μm
Mn	5μm/1μm
Mp1	80μm/0.12μm
Mp2	0.2μm/10μm
Mp3	0.2μm/10μm

A. Operation Under Normal Circuit Operating Condition

Under the normal power-on condition with VDD of 1 V and grounded VSS, the gate voltage of Mp1 is biased at around 1 V through the resistor R with a low gate current of MOS capacitor Mc1 in the new proposed ESD detection circuit, so that Mp1 can be kept off and no trigger current is generated from the ESD detection circuit to the SCR device. In addition, node c in Fig. 3 is biased at some voltage level (∼0.45 V) to turn on Mn which in turn keeps the trigger node of SCR grounded. Fig. 4 shows the Hspice-simulated voltage waveforms on the nodes of the proposed ESD detection circuit and the gate current through the MOS capacitor Mc1 under the normal power-on condition with a rise time of 1 ms and VDD of 1 V (VSS of 0 V). The gate current of Mc1 is only around 23 nA and the voltage level at node a is almost kept at 1 V (overlapped with VDD in Fig. 4), so that Mp1 is kept in off state.

B. Operation Under ESD Transient Event

When a positive fast-transient ESD voltage is applied to VDD with VSS grounded, the RC delay in the ESD detection circuit keeps the gate of Mp1 at a relatively low voltage level compared to the fast rising voltage level at VDD. The Mp1 can be quickly turned on by the ESD energy to generate the substrate-triggered current into the trigger node (node b) of the SCR device. Finally, the SCR device can be fully turned on into holding state to discharge ESD current from VDD to VSS. Fig. 5 shows the simulated voltage and substrate-triggered current of the new proposed ESD detection circuit under the ESD transition, where a 0-to-5 V voltage pulse with a rise time of 10 ns is applied to VDD to simulate the fast transient voltage

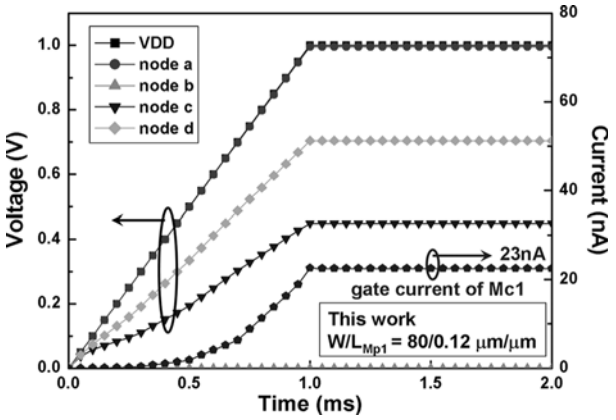


Fig. 4. HSPICE-simulated voltage on the nodes of the ESD detection circuit and the gate current flow through the MOS capacitor Mc1 in the proposed ultra-low leakage ESD clamp circuit in a 65-nm CMOS process under the normal power-on condition.

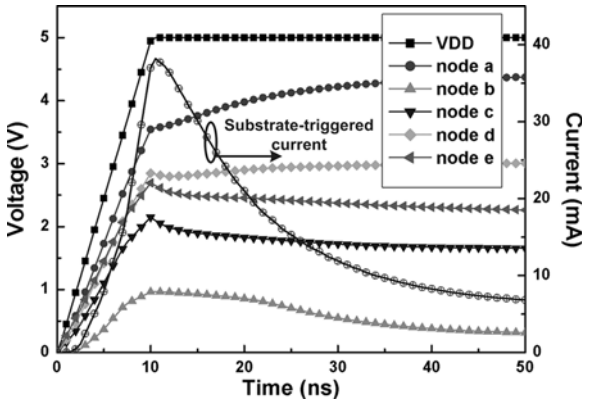
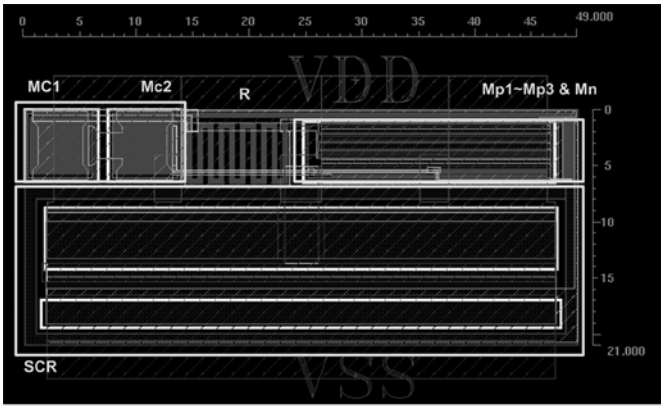
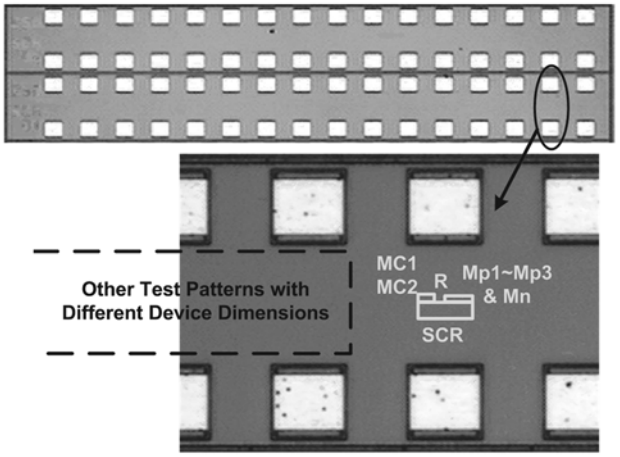


Fig. 5. Hspice-simulated voltages on the nodes of the ESD detection circuit and the substrate-triggered current which flows into the SCR device under 0-to-5 V ESD-like transition on VDD.



(a)



(b)

Fig. 6. (a) Layout view of the proposed power-rail ESD clamp circuit. (b) Chip photograph of the test patterns of the proposed power-rail ESD clamp circuit. The chip has been fabricated in a 65-nm CMOS process with 1-V devices.

of human-body-model (HBM) ESD event [12]. With a limited voltage height of 5 V in the voltage pulse, the voltage transition on each node in the ESD detection circuit can be simulated to check the desired circuit function before device breakdown. With the proposed ESD detection circuit, the SCR device should be triggered on before device breakdown.

IV. Experimental Results

The new proposed power-rail ESD clamp circuit has been fabricated in a 65-nm CMOS process. All devices used in this design are 1-V fully-silicided devices, including the SCR device. The active area of the whole ESD clamp circuit (including the SCR width of 45 μm) is only 49 μm$\times$ 21 μm, and the layout view is shown in Fig. 6(a). The widths of SCR device as ESD clamping device are varied in 30 μm, 45 μm, 60 μm, and 90 μm in the test chip to verify the corresponding ESD robustness. The chip photograph of the test patterns of the proposed power-rail ESD clamp circuit is shown in Fig. 6(b).

A. Turn-on Verification

The turn-on behavior of SCR devices is an important index for ESD protection, which had been evaluated in the literature [13]–[15]. To verify the turn-on efficiency of the proposed ultra-low-leakage ESD clamp circuit, a square-type voltage pulse with a rise time of $\sim$10 ns and a pulse height of 5 V is used to simulate the rising edge of a positive-to-VSS HBM ESD pulse. When the positive voltage pulse is applied to VDD of the proposed ESD clamp circuit with VSS grounded, the sharp-rising edge of the ESD-like voltage pulse will start the ESD detection circuit to generate the substrate-triggered current to trigger on the SCR device, and in turn to provide a low-impedance path between VDD and VSS. The voltage waveform clamped by the ESD clamp circuit on the VDD pad is shown in Fig. 7, where the voltage waveform of the applied ESD-like 0-to-5 V pulse is measured into an open to show its original pulse shape. The applied 5-V voltage pulse is clamped down quickly to a stable low voltage level ($\sim$2 V) by the proposed ESD clamp circuit with a SCR device width of 45 μm. From the measured voltage waveform, the excellent turn-on efficiency of the proposed ESD clamp circuit during the ESD stress event has been successfully verified.

B. ESD Robustness

To investigate the turn-on behavior of the ESD clamping device with ESD detection circuit during the ESD stress event, transmission line pulse (TLP) generator with a pulse width of

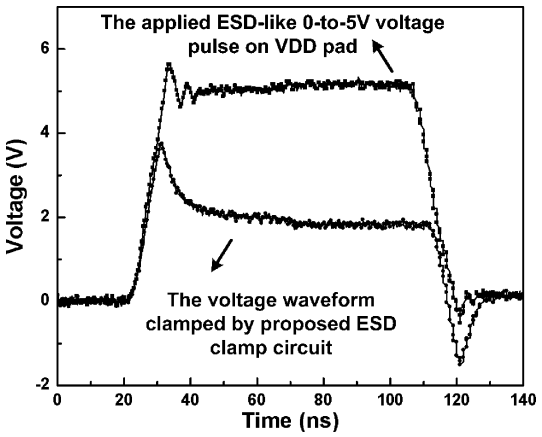


Fig. 7. The measured voltage waveforms clamped by the proposed ESD clamp circuit by applying a 0-to-5 V voltage pulse to VDD pad.

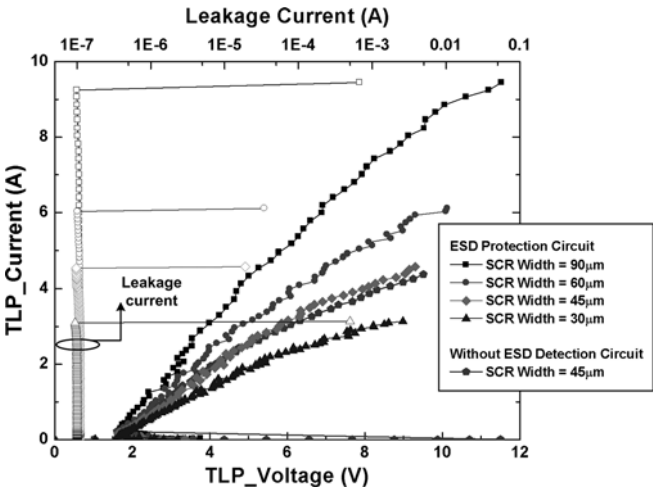


Fig. 8. The TLP-measured I-V characteristics of the proposed power-rail ESD clamp circuit with SCR device of different widths under positive-to-VSS ESD stress. The TLP-measured I-V curve of the stand-alone SCR device without ESD detection circuit is also included in this figure.

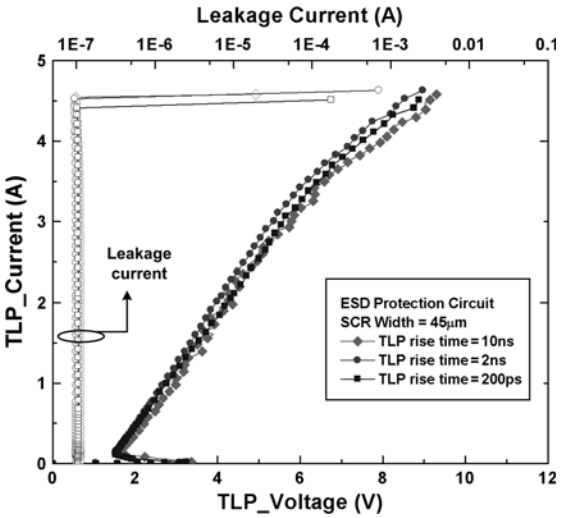


Fig. 9. The TLP-measured I-V characteristics of the proposed power-rail ESD clamp circuit with SCR device of 45 μm under different TLP rise times of 10 ns, 2 ns, and 200 ps.

100 ns and a rise time of ~10 ns is used to measure the second breakdown current (It2) of the ESD clamp circuit. The TLP-measured I-V characteristics of the ESD clamp circuit with SCR device of different widths are shown in Fig. 8, where the device dimension of the substrate driver Mp1 is kept at 80 μm/0.12 μm. The ESD clamp circuit with SCR widths of 45 μm, 60 μm, and 90 μm can achieve It2 of 4.54 A, 6.03 A, and 9.24 A, respectively. Without any triggered current, the original trigger voltage of the SCR device is as high as 11.5 V, as shown in Fig. 8. However, with the proposed ESD detection circuit in this work, the trigger voltage of the SCR device is reduced to only around 3 to 4 V. Therefore, the low trigger voltage and high It2 value of the ESD clamp circuit can ensure the effective ESD protection capability. The holding voltage of the SCR device is around 1.6 V. Such holding voltage is higher than the voltage level of VDD (1 V) under the normal circuit operating condition. Even if the SCR device is mis-triggered due to the noise disturbance, it will automatically recover to the normal condition after the noise source is removed. Therefore, the new proposed power-rail ESD clamp circuit is free from latchup issues. To evaluate the effectiveness of the proposed ESD protection circuit in faster ESD-transient events, the TLP-measured I-V characteristics of the ESD protection circuit with SCR width of 45 μm under the TLP rise times of 10 ns, 2 ns, and 200 ps are compared in Fig. 9. There is no obvious difference in the TLP-measured I-V characteristics under different TLP rise times. The proposed ESD detection circuit is fast enough to turn on the SCR device even under a fast-transient pulse with only 200 ps rise time.

The human-body-model (HBM) ESD levels and machine-model (MM) [16] ESD levels of the proposed ESD clamp circuit with SCR of different widths under positive-to-VSS ESD stress are listed in Table IV. The corresponding second breakdown current (It2) measured by TLP is also listed in Table IV. The failure criterion is defined as the I-V characteristic curve shifting over 20% from its original curve after three continuous ESD zaps at every ESD test level. The HBM and MM ESD levels of the proposed ESD clamp circuit with SCR width of only 45 μm can achieve 7 kV and 325 V, respectively, in a 65-nm CMOS process. The dependence of It2 and MM ESD levels on SCR widths is shown in Fig. 10. From Fig. 10, the It2 performance of the SCR with different widths is almost a straight line, so that the turn-on uniformity of the SCR device can be verified. However, there is some degradation of the MM ESD level compared with the expected dash line when SCR width increases to 90 μm. With a limited driving capability from the same dimension of substrate driver (Mp1) in the ESD detection circuit, the SCR device with a larger device width might be not turned on as efficiently as that with a smaller device width under a faster rising MM ESD stress.

C. Standby Leakage and Design Flexibility

The standby leakage current under 1-V bias of the whole ESD clamp circuit with SCR of 45 μm is only 96 nA at 25 °C.

TABLE IV
ESD ROBUSTNESS OF THE PROPOSED POWER-RAIL ESD CLAMP CIRCUIT WITH SCR DEVICE OF DIFFERENT WIDTHS

SCR Width (μm)	It2 (A)	HBM ESD Level (V)	MM ESD Level (V)
30	3.10	4750	225
45	4.54	7000	325
60	6.03	> 8000	400
90	9.24	> 8000	525

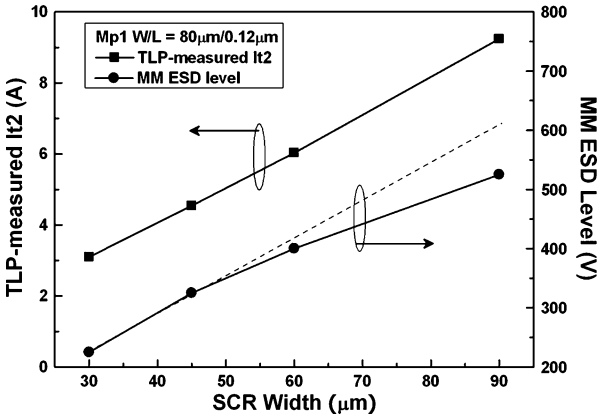


Fig. 10. The dependence of TLP-measured It2 and MM ESD levels on SCR device of different widths.

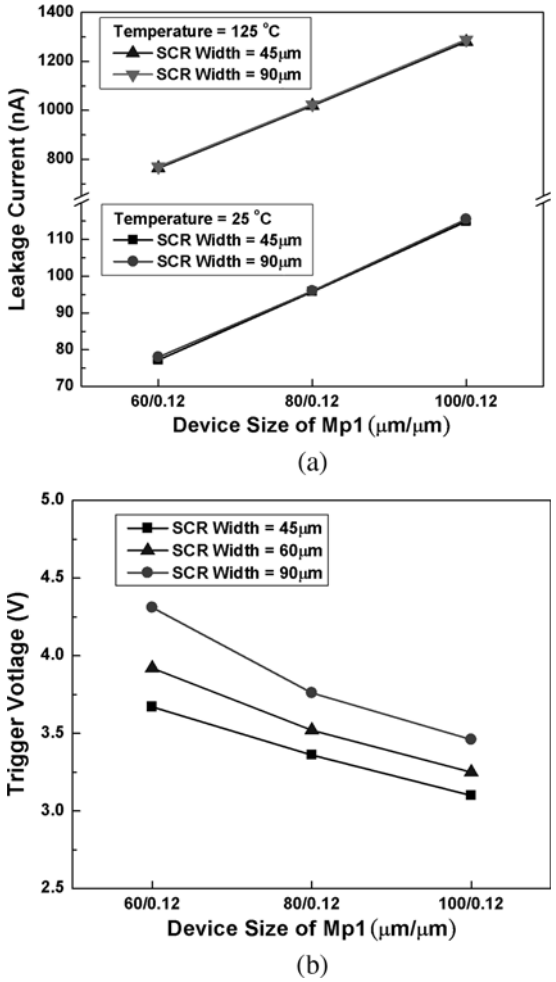


Fig. 11. The dependence of (a) the standby leakage current under 1-V bias of the whole ESD clamp circuit at different temperatures, and (b) the TLP-measured trigger voltage of the SCR device, on the device size of Mp1 under SCR device of different widths.

The standby leakage current of the proposed ESD clamp circuit is dominated by Mp1 in the ESD detection circuit while the leakage current contributed by the MOS capacitor is only ~23 nA from simulation result. Increasing the device dimension of Mp1 can improve the turn-on speed of the SCR device with a reduced trigger voltage, but it results in a larger standby leakage current under the normal circuit operating condition. The measured results of the standby leakage current and the trigger voltage of the proposed power-rail ESD clamp circuit with different dimensions for Mp1 and the SCR device are shown in Fig. 11(a) and (b). From Fig. 11(a), the standby leakage currents of the proposed power-rail ESD clamp circuit with SCR of 45 μm and 90 μm are similar, because there is a quite small leakage current (less than 1 nA at 25 °C) generated from the SCR device. While the device dimension of Mp1 increases from 80 μm/0.12 μm to 100 μm/0.12 μm, the standby leakage current of the whole power-rail ESD clamp circuit increases from 96 nA to 115 nA at 25 °C (1.02 μA to 1.28 μA at 125 °C) under 1-V bias, as shown in Fig. 11(a). However, the corresponding trigger voltage of the SCR of 45 μm can be reduced from 3.7 V to 3.1 V when the dimension of Mp1 is increased, as shown in Fig. 11(b). Therefore, the standby leakage current of the whole ESD clamp circuit and the turn-on speed of the SCR device can be adjusted to meet different application requirements.

D. Discussion

Table V shows the performance comparison among the traditional RC-based power-rail ESD clamp circuit, the modified ESD clamp circuit with timer level restorer, and the new proposed design of this work. The traditional RC-based power-rail ESD clamp circuit was also fabricated in the same 65-nm CMOS process. The standby leakage currents under 1-V bias of the traditional RC-based ESD clamp circuit with the ESD clamping MOSFET ($\mathrm{M_{ESD}}$) of $\mathrm{W/L} = 400\ \mu\mathrm{m}/0.12\ \mu\mathrm{m}$ at 25 °C and 125 °C are as large as 3.74 μA and 44.8 μA, respectively. Even if the leaky ESD clamping MOSFET ($\mathrm{M_{ESD}}$) is excluded, the standby leakage current of the stand-alone ESD detection circuit is still as large as 26.9 μA at 125 °C. The standby leakage current of the modified ESD detection circuit of Fig. 1(b) is simulated as around 1.5 μA with the appropriate device dimensions shown in Table II under the same bias condition (VDD of 1 V with VSS grounded) at 25 °C. Since the high temperature models from the foundry might not be accurate enough, the standby leakage current of the modified ESD detection circuit at 125 °C is not available by simulation. The standby leakage currents under 1-V bias of

TABLE V
COMPARISON AMONG THE PROPOSED POWER-RAIL ESD CLAMP CIRCUIT AND PRIOR WORKS

	Traditional RC-based ESD protection (Fig. 1(a))		Modified ESD clamp circuit with timer level restorer (Fig. 1(b))	This work (Fig. 3)
	ESD Detection Circuit Only	With M_{ESD} W = 400μm L = 0.12μm	ESD Detection Circuit Only	W_{Mp1} = 80μm W_{SCR} = 45μm
Standby leakage current under 1-V bias at 25°C	2.33 μA	3.74 μA	~1.5 μA (simulation)	96 nA
Standby leakage current under 1-V bias at 125°C	26.9 μA	44.8 μA	n/a	1.02 μA
HBM ESD level	n/a	3250 V	n/a	7000 V
Function of ESD detection circuit	poor		good	good
Overall performance	poor		middle	excellent

the proposed ESD clamp circuit with SCR of 45 μm and Mp1 of 80 μm/0.12 μm at 25 °C and 125 °C are only 96 nA and 1.02 μA, respectively. The HBM ESD level of the traditional RC-based ESD clamp circuit with the ESD clamping MOSFET $(\mathrm{M_{ESD}})$ of $\mathrm{W/L} = 400\ \mu\mathrm{m}/0.12\ \mu\mathrm{m}$ is 3.25 kV. However, the HBM ESD level of the proposed ESD clamp circuit with SCR width of 45 μm in this work can achieve 7 kV. With consideration of ESD robustness and standby leakage current, the new proposed ESD clamp circuit of this work has provided an excellent ESD solution in advanced nanoscale CMOS technologies.

V. CONCLUSION

A power-rail ESD clamp circuit with ultra-low standby leakage current and high robust ESD performance has been successfully verified in a 65-nm CMOS process. The proposed ESD detection circuit designed with consideration of gate leakage current has been verified with a standby leakage current of only 96 nA under 1-V bias at 25 °C. Compared with the traditional power-rail ESD clamp circuit, the new proposed power-rail ESD clamp circuit achieves high ESD robustness in a small layout area with an ultra-low standby leakage current and is an excellent circuit solution for on-chip ESD protection design in nanometer CMOS technologies.

REFERENCES

[1] L. K. Han, S. Biesemans, J. Heidenreich, K. Houlihan, C. Lin, V. McCahay, T. Schiml, A. Schmidt, U. P. Schroeder, M. Stetter, C. Wann, D. Warner, R. Mahnkopf, and B. Chen, "A modular 0.13 μm bulk CMOS technology for high performance and low power applications," in *Symp. VLSI Technology Dig. Papers*, 2000, pp. 12–13.

[2] Z. Krivokapic, W. Maszara, K. Achutan, P. King, J. Gray, M. Sidorow, E. Zhao, J. Zhang, J. Chan, A. Marathe, and M.-R. Lin, "Nickel silicide metal gate FDSOI devices with improved gate oxide leakage," in *IEDM Tech. Dig.*, 2002, pp. 271–274.

[3] K. Sathyaki and P. Paily, "Leakage reduction by modified stacking and optimum ISO input loading in CMOS devices," in *Proc. IEEE Int. Conf. on Advanced Computing and Communications*, 2007, pp. 220–225.

[4] M. Agarwal, P. Elakkumanan, and R. Sridhar, "Leakage reduction for domino circuits in sub-65-nm technologies," in *Proc. IEEE Int. SOC Conf.*, 2006, pp. 164–167.

[5] M.-D. Ker, "Whole-chip ESD protection design with efficient VDD-to-VSS ESD clamp circuit for submicron CMOS VLSI," *IEEE Trans. Electron Devices*, vol. 46, no. 1, pp. 173–183, Jan. 1999.

[6] T. Maloney and W. Kan, "Stacked PMOS clamps for high-voltage power supply protection," in *Proc. EOS/ESD Symp.*, 1999, pp. 70–77.

[7] M.-D. Ker and W.-J. Chang, "ESD protection design with on-chip ESD bus and high-voltage-tolerant ESD clamp circuit for mixed-voltage IO buffers," *IEEE Trans. Electron Devices*, vol. 55, no. 6, pp. 1409–1416, Jun. 2008.

[8] M.-D. Ker and C.-T. Wang, "ESD protection design by using only 1×VDD low-voltage devices for mixed-voltage I/O buffers with 3×VDD input tolerance," in *Proc. IEEE Asian Solid-State Circuits Conf.*, 2006, pp. 287–290.

[9] S. S. Poon and T. Maloney, "New considerations for MOSFET power clamps," in *Proc. EOS/ESD Symp.*, 2002, pp. 1–5.

[10] BSIM Model, Berkeley Short-Channel IGFET Model. [Online]. Available: http://www-device.eecs.berkeley.edu/~bsim3/bsim4.html

[11] M.-D. Ker and K.-C. Hsu, "Latchup-free ESD protection design with complementary substrate-triggered SCR devices," *IEEE J. Solid-State Circuits*, vol. 38, no. 8, pp. 1380–1392, Aug. 2003.

[12] ESD Association Standard Test Method ESD STM5.1-2001, for Electrostatic Discharge Sensitivity Testing—Human Body Model (HBM)—Component Level. 2001.

[13] M.-D. Ker and K.-C. Hsu, "SCR device fabricated with dummy-gate structure to improve turn-on speed for effective ESD protection in CMOS technology," *IEEE Trans. Semicond. Manufact.*, vol. 18, no. 5, pp. 320–327, May 2005.

[14] J. D. Sarro, K. Chatty, R. Gauthier, and E. Rosenbaum, "Evaluation of SCR-based ESD protection devices in 90 nm and 65-nm CMOS technologies," in *Proc. IEEE Int. Reliability Physics Symp. (IRPS)*, 2007, pp. 348–358.

[15] G. Wybo, S. Verleye, B. V. Camp, and O. Marchial, "Characterizing the transient device behavior of SCRs by means of VFTLP waveform analysis," in *Proc. EOS/ESD Symp.*, 2007, pp. 366–375.

[16] ESD Association Standard Test Method ESD STM5.2-1999, for Electrostatic Discharge Sensitivity Testing—Machine Model (MM)—Component Level. 1999.

Chang-Tzu Wang (S'06) was born in Taiwan in 1983. He received the B.S. degree from the Department of Electronics Engineering, National Chiao-Tung University (NCTU), Hsinchu, Taiwan, in 2005.

In 2006, He joined the ESD Engineering Department, Reliability Technology and Assurance Division, United Microelectronic Corp. (UMC), as a Senior Engineer. He is currently working toward the Ph.D. degree in the Institute of Electronics, NCTU. His current research interests include on-chip ESD protection circuit design for mixed-voltage I/O circuits and low-power applications.

Ming-Dou Ker (S'92-M'94-SM'97-F'08) received the Ph.D. degree from the Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan, R.O.C., in 1993.

He was the Department Manager with the VLSI Design Division, Computer and Communication Research Laboratories, Industrial Technology Research Institute, Hsinchu. Since 2004, he has been a Full Professor with the Nanoelectronics and Gigascale Systems Laboratory, Department of Electronics Engineering and Institute of Electronics, National Chiao-Tung University. From 2006 to 2008, he served as the Director of Master Degree Program with the College of Electrical Engineering and Computer Science, National Chiao-Tung University, as well as the Associate Executive Director of the National Science and Technology Program on System-on-Chip (NSoC Office), Taiwan. In 2008, he served as the Chair Professor and the Vice President of I-Shou University, Kaohsiung, Taiwan. In the field of reliability and quality design for circuits and systems in CMOS technology, he has published over 350 technical papers in international journals and conferences. He has proposed many inventions to improve the reliability and quality of integrated circuits, which have been granted with 137 U.S. patents and 144 R.O.C. (Taiwan) patents. He had been invited to teach and/or to consult the reliability and quality design for integrated circuits by hundreds of design houses and semiconductor companies in the worldwide IC industry. His current research interests include reliability and quality design for nanoelectronics and gigascale systems, high-speed and mixed-voltage I/O interface circuits, on-glass circuits for system-on-panel applications, and biomimetic circuits and systems for intelligent prosthesis.

Prof. Ker has served as a member of the Technical Program Committee and the Session Chair of numerous international conferences. He served as the Associate Editor for the IEEE TRANSACTIONS ON VLSI SYSTEMS. He has been selected as the Distinguished Lecturer in the IEEE Circuits and Systems Society (for year 2006–2007) and in the IEEE Electron Devices Society (since 2008). He was the President of Foundation in the Taiwan ESD Association. In 2005, one of his patents on ESD protection design has been awarded with the National Invention Award in Taiwan. In 2008, he has been elevated as an IEEE Fellow "for his contributions to the electrostatic protection in integrated circuits and the performance optimization of VLSI microsystems."