Design of Mixed-Voltage-Tolerant Crystal Oscillator Circuit in Low-Voltage CMOS Technology

Tzu-Ming Wang, *Student Member, IEEE*, Ming-Dou Ker, *Fellow, IEEE*, and Hung-Tai Liao

***Abstract*—In the nanometer-scale CMOS technology, the gate-oxide thickness has been scaled down to provide higher operating speed with lower power supply voltage. However, regarding compatibility with the earlier defined standards or interface protocols of CMOS ICs in a microelectronics system, the chips fabricated in the advanced CMOS processes face the gate-oxide reliability problems in the interface circuits due to the voltage levels higher than normal supply voltage (1 × VDD) required by earlier applications. As a result, mixed-voltage I/O circuits realized with only thin-oxide devices had been designed with advantages of less fabrication cost and higher operating speed to communicate with the circuits at different voltage levels. In this paper, two new mixed-voltage-tolerant crystal oscillator circuits realized with low-voltage CMOS devices are proposed without suffering the gate-oxide reliability issues. The proposed mixed-voltage crystal oscillator circuits, which are one of the key I/O cells in a cell library, have been designed and verified in a 90-nm 1-V CMOS process, to serve 1-V/2-V tolerant mixed-voltage interface applications.**

***Index Terms*—Crystal oscillator, gate-oxide reliability, mixed-voltage I/O.**

I. Introduction

With new generations of CMOS technologies, the device dimension of transistors has been scaled toward the nanometer region to reduce the silicon cost as well as to increase circuit performance and operating speed. The power supply voltage of chips in the nanoscale CMOS process has been also decreased for low power consumption [1]. Therefore, the maximum tolerable voltage across the transistor terminals (i.e., drain, source, gate, and bulk) should be correspondingly decreased to ensure lifetime. The normal lifetime is typically ∼10 years with continuous operation under specified worst case operating conditions. The circuits or transistors should be operated correctly without function error or leakage issue at least for ∼10 years under the normal power supply voltage (1 × VDD).

The shrunken device dimension, however, makes the chip area smaller to save silicon costs and the lower power supply voltage results in lower power consumption. Therefore, chip design quickly migrates to the lower voltage level with the advancement of the nanoscale CMOS technology. Nevertheless, some peripheral components or other ICs in a microelectronic system could be still operated at some higher voltage levels for compatibility to the earlier interface specifications. In other words, the interface circuits between two chips have to deal with the I/O signals at different voltage levels [2]–[4].

A complete I/O library includes the digital and analog I/O cells, power/ground cells, and crystal oscillator cells. The design of mixed-voltage I/O circuits has been discussed and reported in some literatures [5]–[8], but the mixed-voltage- tolerant crystal oscillator circuit was never mentioned before.

A conventional crystal oscillator circuit is connected with a crystal between the output (XO) pad and the input (XI) pad for oscillation to generate the stable clock signal for chip operations. In some applications, the clock signal will be directly provided from the external clock sources and sent into the chip through the input (XI) pad with the output (XO) pad floating. However, the conventional crystal oscillator circuit designed with 1 × VDD CMOS devices is unsuitable to receive the external clock signal with voltage level over VDD, due to the gate-oxide reliability issue [9], [10] and the hot-carrier degradation issue [11].

In this paper, two new 2 × VDD-tolerant crystal oscillator circuits realized with only low-voltage (1 × VDD) CMOS devices are proposed without suffering the gate-oxide reliability issue. The proposed mixed-voltage crystal oscillator circuits have been designed and verified in a 90-nm 1-V CMOS process to serve 1-V/2-V-tolerant mixed-voltage interface applications.

II. Pierce Oscillator

The theory and application of crystal oscillator circuits had been reported in [12]. The Pierce-type crystal oscillator circuit is one of examples with source-grounded configuration for high-precision application. The conventional Pierce-type crystal oscillator circuit is shown in Fig. 1 [13], where the crystal is expected to oscillate in parallel resonant mode.

The equivalent circuit of a crystal is shown in Fig. 2. $\mathrm{R_s}$ is the effective series resistance in the crystal, and $\mathrm{L_s}$ and $\mathrm{C_s}$ are the motional inductance and capacitance of the crystal. $\mathrm{C_p}$ is the parasitic shunt capacitance due to the electrodes. Fig. 3 shows the reactance-frequency plot of a crystal. When the crystal is operating at series resonance, it performs purely resistively, and the series resonance frequency $(\mathrm{f_s})$ is given by

$$\mathrm{f_s} = \frac{1}{2\pi\sqrt{\mathrm{L_s C_s}}} \tag{1}$$

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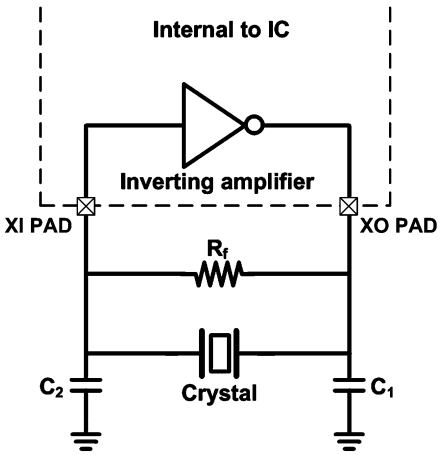

Fig. 1. Pierce-type crystal oscillator circuit.

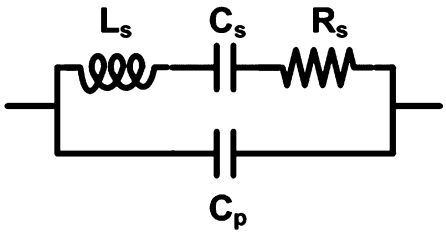

Fig. 2. Equivalent circuit of a crystal.

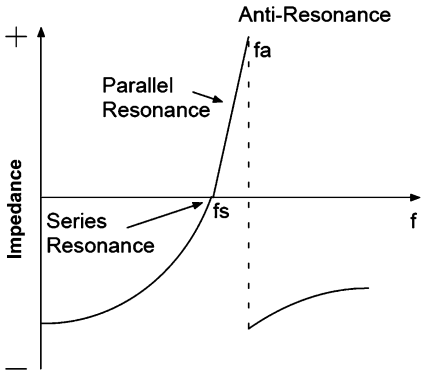

Fig. 3. Reactance-frequency plot of a crystal.

When the crystal is operating in parallel resonant mode, it looks inductive and the frequency $(\mathrm{f_a})$ of oscillation is given by

$$\mathrm{f_a} = \frac{1}{2\pi\sqrt{\mathrm{L_s}\frac{\mathrm{C_L C_P}}{\mathrm{C_L}+\mathrm{C_P}}}} \tag{2}$$

where the $\mathrm{C_L}$ is

$$\mathrm{C_L} = \frac{\mathrm{C_1}\cdot\mathrm{C_2}}{\mathrm{C_1}+\mathrm{C_2}} + \mathrm{Cstray} \tag{3}$$

and Cstray is the stray capacitance on the printed circuit board. The crystal can be designed to oscillate between $\mathrm{f_s}$ and $\mathrm{f_a}$ by varying the load of the crystal.

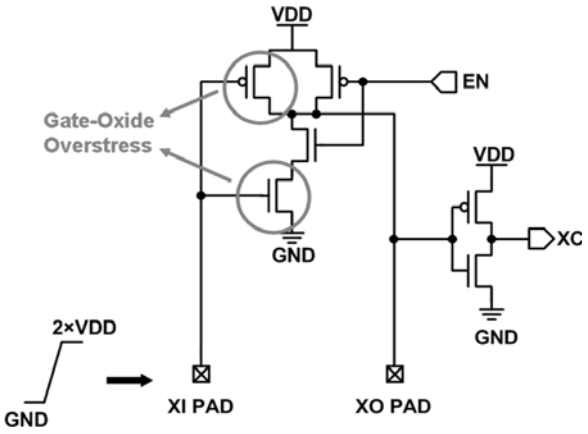

Fig. 4. Conventional crystal oscillator circuit (realized with $1\times$ VDD devices) suffering the gate-oxide reliability issue when it receives a $2\times$ VDD external input clock signal.

III. Gate-Oxide Reliability Issue

In the advanced CMOS process, the devices with thinner gate oxide can be operated at a higher operating speed under a lower VDD supply voltage. The power supply voltage level has been decreased from higher voltage level (around 2-V or higher) to lower voltage level (around 1 V or below) to maintain the gate-oxide reliability and to overcome the hot-carrier degradation in ICs fabricated by 90-nm CMOS technology. However, other components on the printed circuit board or in the microelectronics system could be still operated at higher voltage level. Therefore, the I/O interface circuit should be designed for such mixed-voltage applications.

Fig. 4 shows the conventional crystal oscillator circuit realized with $1\times$ VDD devices. When this circuit is utilized in the mixed-voltage I/O interface, it suffers from the gate-oxide reliability issues [6], [7]. When the EN signal is kept at VDD and the $2\times$ VDD external input clock signal is received at the XI pad, the pull-up pMOS and pull-down nMOS (marked with circles in Fig. 4) suffer the gate-oxide overstress problem. In order to avoid the gate-oxide reliability issue, the devices which suffer the gate-oxide overstress could be replaced by the thick-oxide devices. However, with both of the thick-oxide and thin-oxide devices in a chip, the fabrication cost of CMOS process is increased. The circuit solution to solve such mixed-voltage ($2\times$ VDD-tolerant) applications with only thin-oxide ($1\times$ VDD) devices is highly requested by IC industry.

IV. New Proposed Mixed-Voltage-Tolerant Crystal Oscillator Circuit I

Fig. 5 shows the new proposed mixed-voltage-tolerant crystal oscillator circuit I realized with only thin gate-oxide ($1\times$ VDD) devices [14]. XI pad and XO pad are the input and output pads of the proposed circuit I with EN and PA signals controlled by the internal circuits of IC. XC is the clock signal sending to internal circuits, which is produced by crystal oscillator circuit or by the external clock signal. In this study, this XC signal is especially connected to a bond pad for monitoring/verifying its voltage

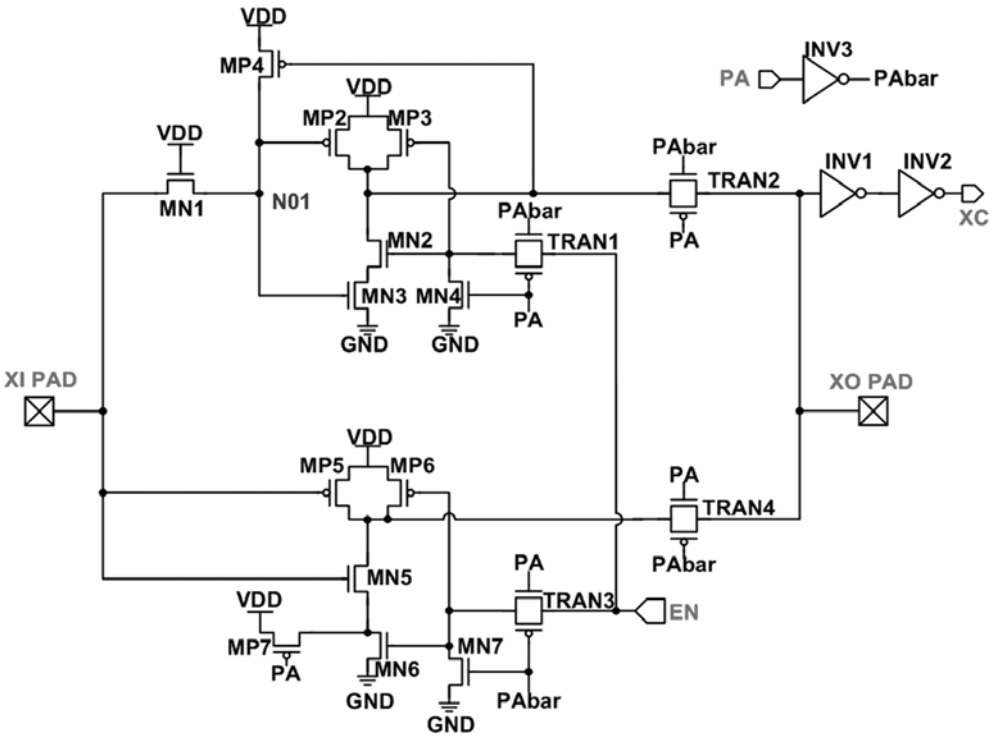

Fig. 5. New proposed mixed-voltage-tolerant crystal oscillator circuit I.

waveform. In order to solve gate-oxide reliability issue in receiving mode, the conventional crystal oscillator circuit is modified with upper and lower paths by adding some transmission gates to pass signal in receiving and oscillation mode, respectively. By nMOS-blocking [7] and level-restoring techniques, MN1 is added in the upper path before the NAND gate to solve gate-oxide reliability issue as well as MP4 is utilized to pull the N01 node to full VDD when the input signal is logic "1." In the meanwhile, MP7 is added to keep the lower path from gate-oxide reliability issue. The detail operation is shown in the following.

A. Oscillation Mode

When the voltage level of PA is VDD, the proposed mixed-voltage-tolerant crystal oscillator circuit I is operated with crystal and two load capacitances to generate the sinusoidal-wave signal at both XI and XO pads. In this operating condition, transmission gates TRAN1 and TRAN2 are turned off, as well as TRAN3 and TRAN4 are turned on, so that the sinusoidal-wave signal can only pass through the lower path of this circuit from XI pad to XO pad. In the upper path, in order to keep the output terminal of the upper NAND gate at VDD, MN4 is turned on to keep MN2 off and MP3 on. Besides, the gate terminal of MP4 is directly connected to the output terminal of the upper NAND gate, so MP4 is turned off. The input node (N01) of the upper NAND gate will follow the voltage level of XI pad, while the output node of upper NAND gate keeps at VDD. The signal EN can be transmitted to one input node of the lower NAND gate to enable $(\mathrm{EN} = \mathrm{VDD})$ or disable $(\mathrm{EN} = \mathrm{GND})$ the lower NAND gate. In the lower path, MN7 and MP7 are turned off while the gate terminals of MN6 and MP6 are connected to VDD, so the generated sinusoidal-wave signal will pass through the lower path of this circuit from XI pad to XO pad.

B. Receiving Mode

When the voltage level of PA signal is GND, the proposed mixed-voltage-tolerant crystal oscillator circuit I is operated to receive an external clock input signal whose voltage level could be $1 \times$ VDD or $2 \times$ VDD. TRAN1 and TRAN2 are turned on and the external clock signal passes through the upper path from XI pad to XC. In the upper path, MN4 is turned off, as well as MN1 and MP4 with upper NAND gate are used to transfer the external clock signal from the XI pad to the XO pad. MN1 is used to limit the voltage level of external clock input signal reaching to the gate oxide of the upper NAND gate. Because the gate terminal of MN1 is connected to the power supply voltage (VDD), the input (N01) voltage of the upper NAND gate is limited to VDD-Vt when the voltage level of external clock signal is even up to $2 \times$ VDD. Then, transistor MP4 further pulls the input node (N01) of the upper NAND gate up to VDD, when the output node of the upper NAND gate is pulled down near to GND. The external clock signal can be successfully transferred into the internal input node XC. Meanwhile, TRAN3 and TRAN4 are turned off. MN7 is turned on to keep MN6 off and MP6 on in order to keep the output terminal of the lower NAND gate at VDD.

MP7 is also turned on to keep the node between MN5 and MN6 at VDD. Thus, when the XI pad is with the input signal voltage level of $2 \times$ VDD, any voltage drop between the gate terminal and source/drain terminal of MN5 and MP5 is still limited to VDD. Therefore, the new proposed crystal oscillator circuit I can receive the external clock signal of $2 \times$ VDD without suffering the gate-oxide overstress issue.

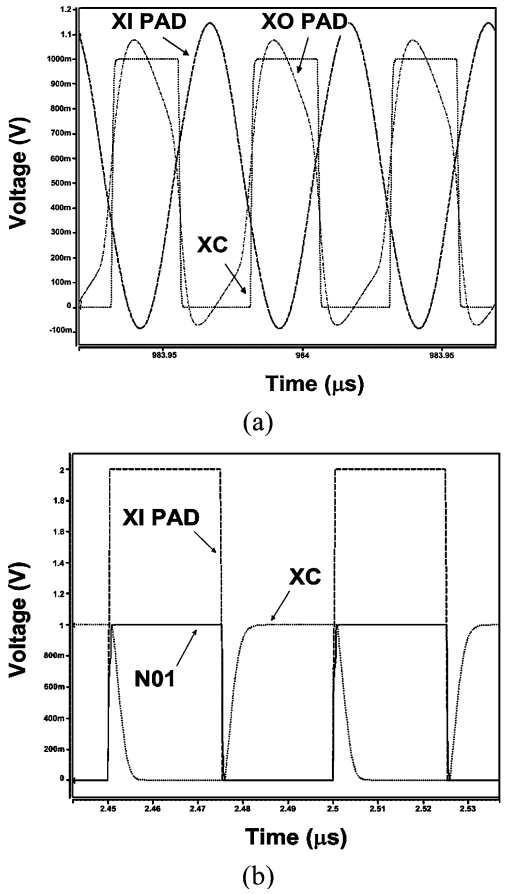

Fig. 6. Simulated waveforms of the new proposed crystal oscillator circuit I with (a) a crystal of 20-MHz fundamental frequency and load capacitance of 20 pF ($\mathrm{PA} = \mathrm{VDD}$) and (b) 20-MHz external clock signal with voltage level of $2 \times$ VDD into XI pad ($\mathrm{PA} = \mathrm{GND}$).

C. Simulations

Fig. 6 shows the simulated waveforms of the proposed mixed-voltage-tolerant crystal oscillator circuit I in a 90-nm 1-V CMOS process to serve 1-V/2-V-tolerant mixed-voltage interface. In Fig. 6(a), the proposed mixed-voltage crystal oscillator circuit I with the crystal of 20-MHz fundamental frequency and a load capacitance of 20 pF at the pad can successfully generate the clock signal of 20 MHz at the XC node under the power supply of $1 \times$ VDD. As shown in Fig. 6(b), with the 20-MHz external clock signal of $2 \times$ VDD into XI pad, the input (N01) voltage of the upper NAND gate can be limited and biased at the desired voltage level (1 V). The final signal voltage level reaching to the XC node is successfully shifted down to $1 \times$ VDD. In addition, the power consumption in the oscillation mode with 20-MHz fundamental frequency is 0.46 mW, whereas the power consumption is 0.42 mW in the receiving mode with 20-MHz external clock signal of $2 \times$ VDD. From the simulated results, the desired functions of this mixed-voltage-tolerant crystal oscillator circuit I have been verified without suffering the gate-oxide reliability issue.

D. Layout

Fig. 7 shows the layout view of the proposed mixed-voltage-tolerant crystal oscillator circuit I implemented in a 90-nm CMOS process. The cell size of XI, as well as XO, is only 190.5 μm $\times$ 60 μm (including the bond pad), which is the same as that of digital and analog I/O cells in a given standard I/O cell library. Feedback resistance $\mathrm{R_f}$ is also included and implemented by the poly resistance in the cell.

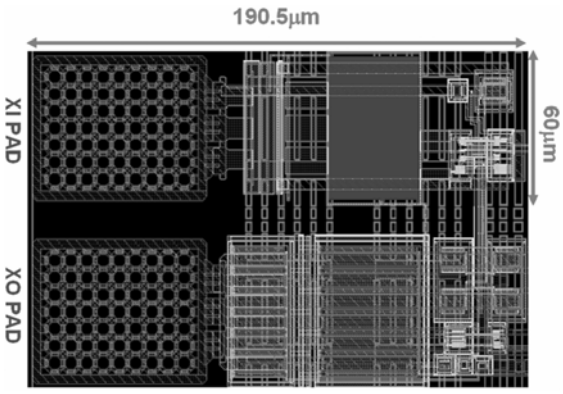

Fig. 7. Layout view of new proposed mixed-voltage-tolerant crystal oscillator circuit I in a 90-nm CMOS process.

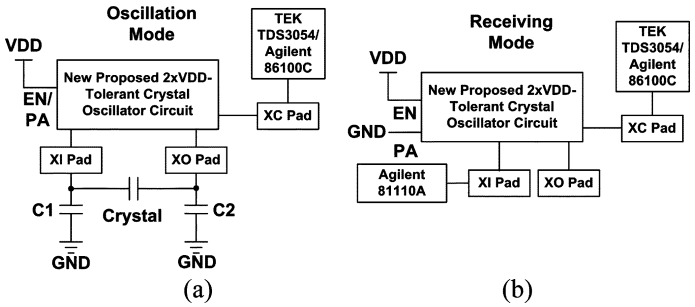

Fig. 8. Measurement setups for (a) the oscillation mode and (b) the receiving mode.

E. Measured Results

The measurement setups for oscillation mode and receiving mode are shown in Fig. 8(a) and (b), respectively. Agilent 86100C is utilized to measure jitter performance, TEK TDS3054 can observe the output waveforms, and Agilent 81110A is used to generate the external clock signal. The measured voltage waveforms of the new proposed mixed-voltage-tolerant crystal oscillator circuit I, which has been fabricated in a 90-nm CMOS process, in the oscillation mode with 4-MHz and 20-MHz crystals are shown in Fig. 9(a) and (b), respectively. As shown in Fig. 9, the clock signals of 4 and 20 MHz can be successfully generated at the XC node by the sinusoidal voltage waveforms at the XO pad. The degraded voltage waveforms measured at XI, XO, and XC nodes are due to the large parasitic capacitive loading at the bond pad with on-chip ESD protection device and the limited output driving capability of circuit in the test chip.

The voltage waveforms of the new proposed mixed-voltage-tolerant crystal oscillator circuit I operating in the receiving mode with the external 4-MHz input clock signals of 0–1 V and 0–2 V are measured in Fig. 10(a) and (b), respectively. Fig. 11 shows the measured voltage waveforms of the proposed circuit I operated in the receiving mode with the external 20-MHz input clock signals of 0–1 V and 0–2 V. As shown in Figs. 10 and 11, the input clock signals can be correctly received and shifted to

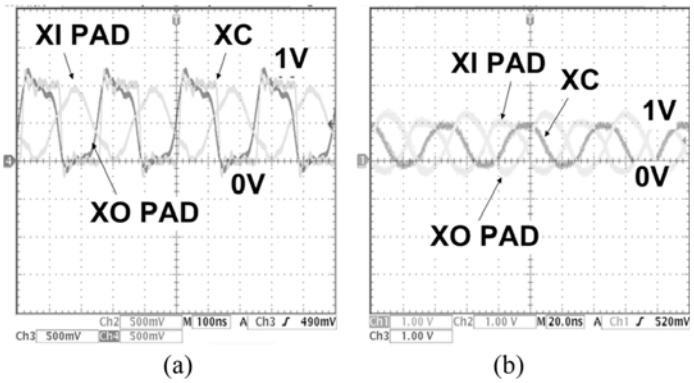

Fig. 9. Measured voltage waveforms of the new proposed mixed-voltage-tolerant crystal oscillator circuit I with a crystal of fundamental frequency at (a) 4 MHz and (b) 20 MHz.

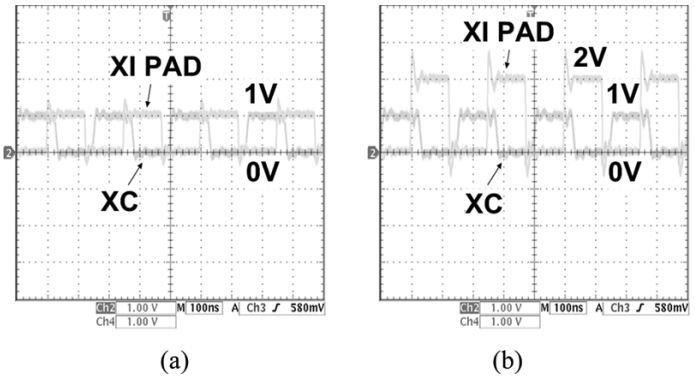

Fig. 10. Measured voltage waveforms of the new proposed mixed-voltage-tolerant crystal oscillator circuit I with a 4-MHz external input clock signal under the voltage levels of (a) 0-to-1 V and (b) 0-to-2 V.

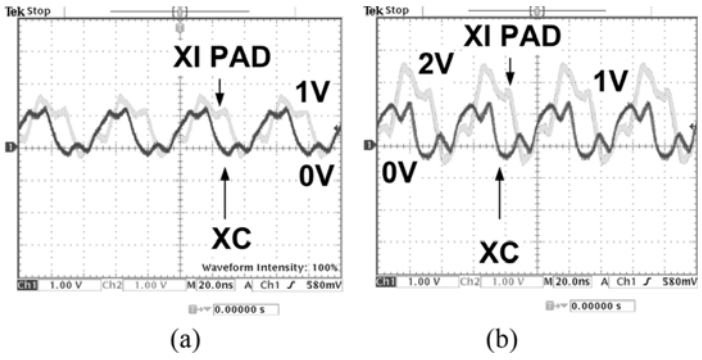

Fig. 11. Measured voltage waveforms of the new proposed mixed-voltage-tolerant crystal oscillator circuit I with a 20-MHz external input clock signal under the voltage levels of (a) 0-to-1 V and (b) 0-to-2 V.

the 0–1-V signal at the XC node. Fig. 12 shows the jitter performance of the proposed circuit I in oscillation mode at 20 MHz, where the standard deviation (std dev) and peak-to-peak (p-p) jitter are 358 ps and 3.83 ns in this measurement. Fig. 13 shows the jitter performance of the proposed circuit I in receiving mode with 20-MHz external clock signal of 2 × VDD, where the standard deviation and peak-to-peak jitter are 265 ps and 2.2 ns. From the measured results, the new proposed mixed-voltage-tolerant crystal oscillator circuit I can be operated correctly.

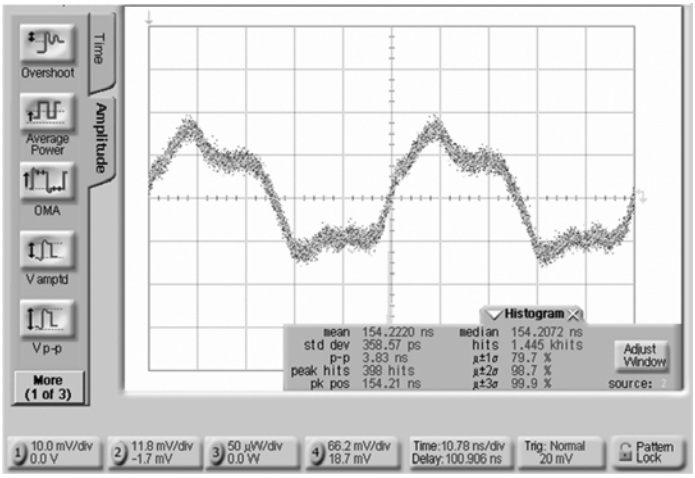

Fig. 12. Measured jitter of the new proposed mixed-voltage-tolerant crystal oscillator circuit I with a crystal of fundamental frequency at 20 MHz.

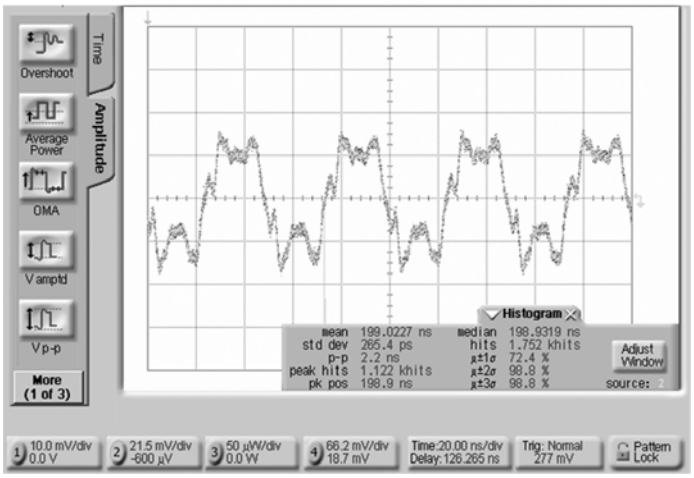

Fig. 13. Measured jitter of the new proposed mixed-voltage-tolerant crystal oscillator circuit I with a 20-MHz external input clock signal under the voltage level of 0-to-2 V.

V. New Proposed Mixed-Voltage Tolerant Crystal Oscillator Circuit II

Fig. 14 shows anther new proposed 2 × VDD-tolerant crystal oscillator circuit II realized with only 1 × VDD thin-oxide devices [15]. Compared with the proposed circuit I, the signal PA is no longer needed. XI and XO pads are the input and output pads of the proposed circuit, respectively. Signal EN is controlled by the internal circuits of IC, and XC is the clock signal which is produced by crystal oscillator circuit or received from the external clock signal. The transistors MN2, MN3, MP2, and MP3 form the inverting amplifier of the proposed circuit. Inverters INV4 and INV5 can transform the sinusoidal-wave signal to a square signal or to pass the external clock signal into the internal node XC.

Compared with the proposed circuit I, the proposed circuit II solves the gate-oxide reliability issue with only single path and no additional control signal PA is needed. In order to combine the two paths of the proposed circuit I into single one, floating N-well technique [5] is applied to keep MN1 and MP1 from gate-oxide reliability issue and some extra devices are utilized to

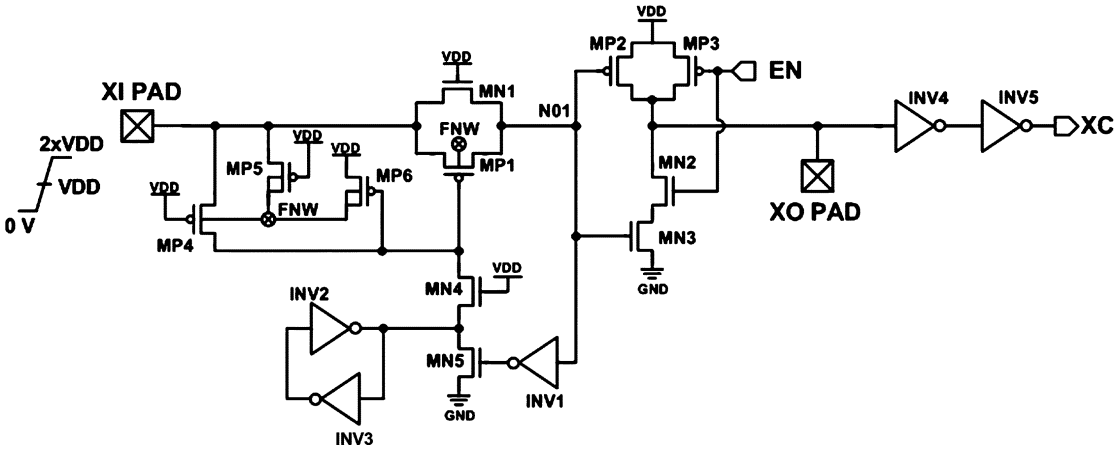

Fig. 14. New proposed mixed-voltage-tolerant crystal oscillator circuit II.

make N01 and FNW biased at proper voltage levels. The detail operation is described in the following.

A. Oscillation Mode

It is operated to generate the sinusoidal-wave signal, when the proposed circuit II is connected with crystal and two load capacitances (C_1 and C_2) at XI and XO pads. MP4 and MP5 are turned off while MN4 is turned on with the gate terminal connected to power supply (VDD). The sinusoidal-wave signal with voltage level less than VDD-Vt at XI pad can pass through the transistor MN1 to the input (N01) of the NAND gate, when oscillation starts up. When the input node (N01) of the inverter INV1 is with a low voltage level ($\sim$0V), MN5 is turned on to bias the gate terminal of MP1 at GND, and the inverters INV2 and INV3 hold this voltage level by a latch configuration. The sinusoidal-wave signal, even if the voltage level is over VDD-Vt, can pass through the transistor MP1 to N01. Therefore, the sinusoidal-wave signal can completely pass through the MN1 and MP1 to the input terminal of the NAND gate without distortion. Moreover, MP6 is turned on to bias the floating N-well (FNW) at VDD.

B. Receiving Mode

For the mixed-voltage interface applications, the proposed circuit II may receive an external input clock signal with voltage level of $1 \times$ VDD or $2 \times$ VDD. In order to limit the voltage level of input clock signal reaching to the gate oxide of the NAND gate, MP4 is utilized to trace the signal at the XI pad and control the gate voltage of transistor MP1. When the voltage level at the XI pad exceeds $\mathrm{VDD} + |\mathrm{Vtp}|$, MP4 is turned on to charge the gate terminal of MP1 up to $2 \times$ VDD. MP1 is completely turned off to prevent the voltage level at the input node (N01) of the NAND gate from rising up to $2 \times$ VDD.

With the input voltage of $2 \times$ VDD at XI pad, MP5 is turned on and MP6 is turned off to bias the floating N-well (FNW) at $2 \times$ VDD. Besides, when the voltage level of XI pad is at GND, MN5 will be turned on by the inverter INV1, and further to turn on the MP1. With the input signal of 0 V at XI pad, MP5 is turned off and MP6 is turned on to bias the floating N-well (FNW) at VDD.

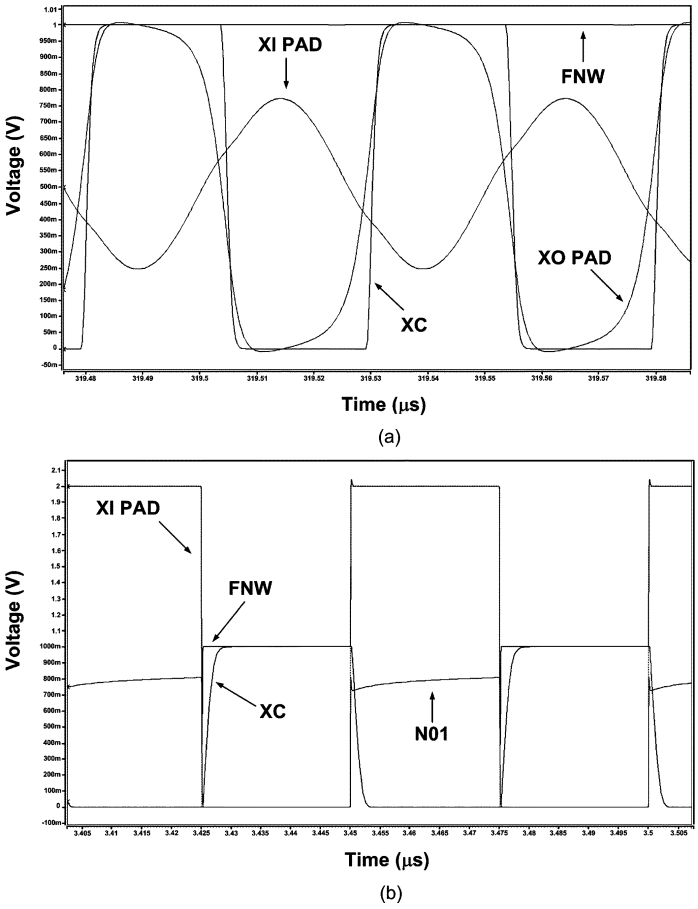

Fig. 15. Simulated waveforms of the new proposed mixed-voltage-tolerant crystal oscillator circuit II with (a) a crystal of 20-MHz fundamental frequency and load capacitance of 20 pF at the XI and XO pads and (b) 20-MHz external input clock signal with voltage level of $2 \times$ VDD into XI pad.

C. Simulations

Fig. 15 show the simulated waveform of the proposed mixed-voltage-tolerant crystal oscillator circuit II in a 90-nm 1-V CMOS process to serve 1/2-V mixed-voltage interface. In Fig. 15(a), the proposed circuit II with the crystal of 20-MHz fundamental frequency and 20-pF load capacitance at the XI and XO pads can successfully generate the clock signal of 20 MHz at the XC node under the power supply of $1 \times$ VDD.

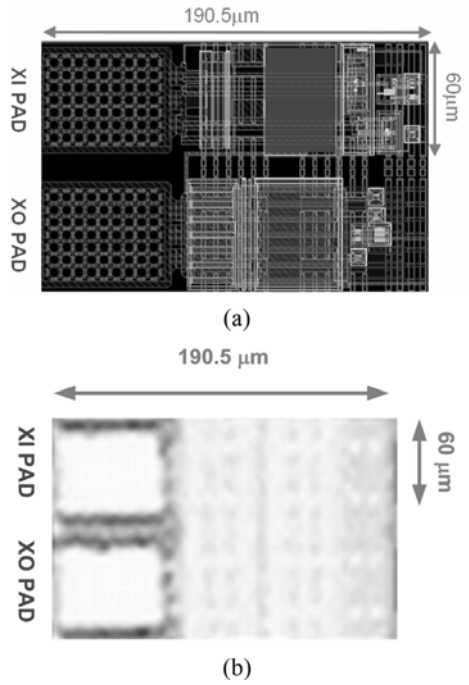

Fig. 16. (a) Layout view and (b) die photograph of the proposed mixed-voltage-tolerant crystal oscillator circuit II realized in a 90-nm CMOS process.

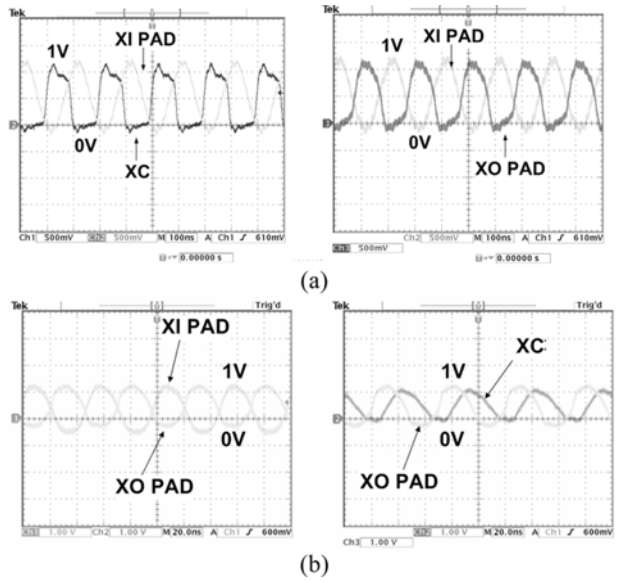

Fig. 17. Measured voltage waveforms of the new proposed mixed-voltage-tolerant crystal oscillator circuit II with crystal fundamental frequency at (a) 4 MHz and (b) 20 MHz.

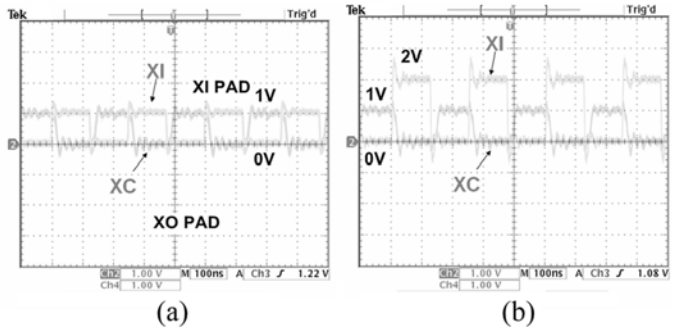

Fig. 18. Measured voltage waveforms of the new proposed mixed-voltage-tolerant crystal oscillator circuit II with a 4-MHz external input clock signal under the voltage levels of (a) 0-to-1 V and (b) 0-to-2 V.

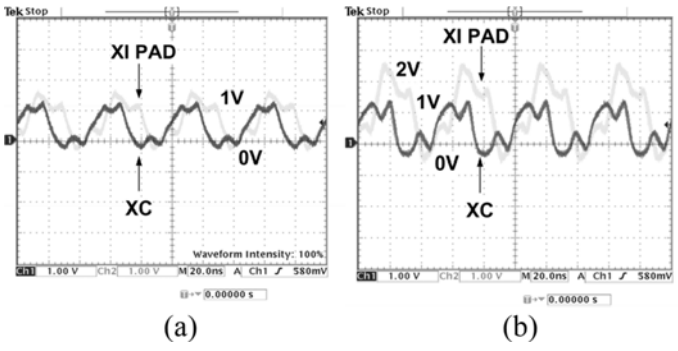

Fig. 19. Measured voltage waveforms of the new proposed mixed-voltage-tolerant crystal oscillator circuit II with a 20-MHz external input clock signal under the voltage levels of (a) 0-to-1 V and (b) 0-to-2 V.

As shown in Fig. 15(b), with the 20-MHz external clock signal of $2 \times$ VDD at XI pad, the input node (N01) of the NAND gate can be limited to the voltage level of $\sim$0.8 V. The final signal voltage level reaching to the XC node is successfully shifted down to $1 \times$ VDD. In addition, FNW is biased at $1 \times$ VDD in oscillation mode, at $2 \times$ VDD in receiving mode when the XI pad is $2 \times$ VDD, and at $1 \times$ VDD in receiving mode when the XI pad is 0 V. By simulation, the power consumption in the oscillation mode with 20-MHz fundamental frequency is 1.1 mW. The power consumption is 0.26 mW in the receiving mode with 20-MHz external input clock signal of $2 \times$ VDD. From the simulated results, the desired functions of the proposed mixed-voltage-tolerant crystal oscillator circuit II have been verified.

D. Experimental Results

The layout view and die photograph of the mixed-voltage-tolerant crystal oscillator circuit II implemented in a 90-nm 1-V CMOS process are shown in Fig. 16(a) and (b), respectively. The cell size is only 190.5 μm $\times$ 60 μm (including the bond pad), which is the same as that of digital and analog I/O cells in a standard I/O cell library. The feedback resistance R_f, implemented by the poly resistance, is also included in the layout. ESD protection is also provided by following the foundry ESD design rules to draw the nMOS and pMOS devices which are directly connected to the pads.

The measured results of the new proposed mixed-voltage- tolerant crystal oscillator circuit II in oscillation mode are shown in Fig. 17. In Fig. 17(a) and (b), the new proposed circuit II can successfully transmit the 0-/1-V sinusoidal-wave signal with frequency of 4 MHz and 20 MHz to the XC node, respectively. The measured results of the new proposed circuit II in the receiving mode are shown in Figs. 18 and 19 under the operating frequency of 4 MHz and 20 MHz, respectively. The new proposed circuit II can successfully transmit the 0-/1-V external input clock signal to the XC node with the input voltage levels of 0–1 V or 0–2 V.

Fig. 20 shows the measured jitter performance of the proposed circuit II in oscillation mode with the crystal fundamental frequency at 20 MHz. The standard deviation and peak-to-peak

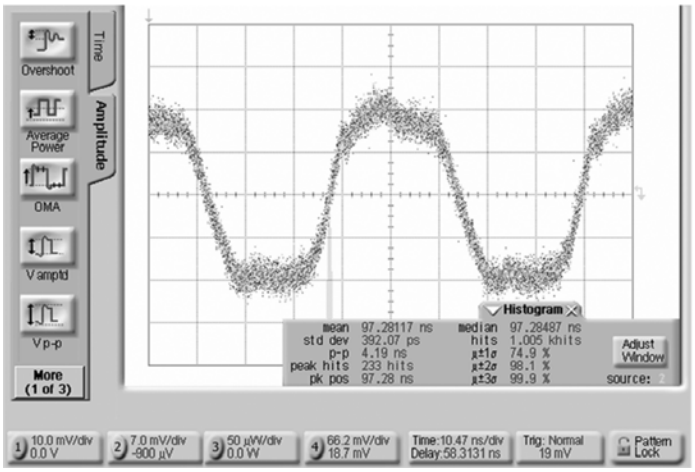

Fig. 20. Measured jitter of the new proposed mixed-voltage-tolerant crystal oscillator circuit II with the crystal fundamental frequency at 20 MHz.

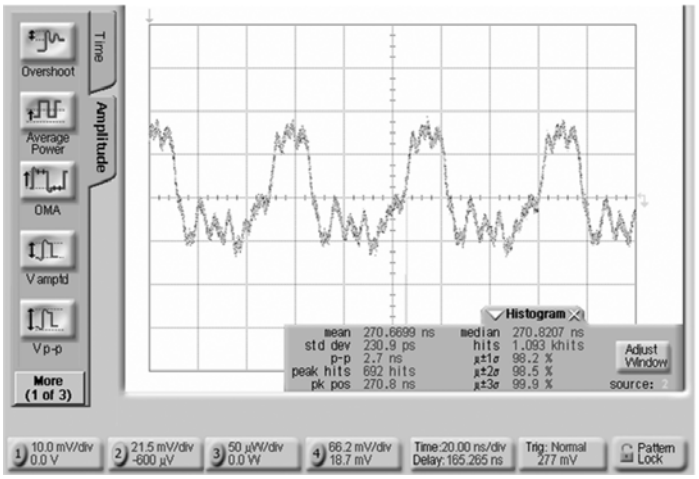

Fig. 21. Measured jitter of the new proposed mixed-voltage-tolerant crystal oscillator circuit II, when a 20-MHz external input clock signal is applied with the voltage level of 0-to-2 V.

jitter are 392 ps and 4.19 ns, respectively. Fig. 21 shows the measured jitter performance of the proposed circuit II in receiving mode with the 20-MHz external input clock signal of $2 \times$ VDD. The standard deviation and peak-to-peak jitter are 231 ps and 2.7 ns in Fig. 21. The degraded voltage waveforms measured at XI, XO, and XC nodes are due to the large parasitic capacitive loading at the bond pads with on-chip ESD protection devices and the limited driving capability of the output transistors in the test chip. To improve the circuit performance in the high-frequency measurement, additional buffers should be added between the XC node and the bond pad.

VI. Comparison and Discussion

Table I shows the comparison between the two proposed circuits. The proposed circuit I has 27 transistors with additional signal PA. The proposed circuit II has 21 transistors with FNW technique. In the oscillation (Osc.) mode, the sinusoidal-wave at the N01 node of circuit II has higher power consumption due to the short circuit current of the NAND gate. These two proposed circuits in the receiving (Rec.) mode have better jitter performance than those in oscillation mode, because the external

TABLE I
Comparison Between the Two Proposed Circuits

		Proposed Circuit I		Proposed Circuit II	
		Osc. mode	Rec. mode	Osc. mode	Rec. mode
Power (mW) @ 20 MHz		0.46	0.42	1.1	0.26
Jitter @ 20 MHz	STD.	358 ps	265 ps	396 ps	231 ps
	Peak-to-Peak	3.83 ns	2.2 ns	4.19 ns	2.7 ns

clock signal is generated by pulse generator during the measurement. Compared with some earlier works [16], [17], the jitter performance of those earlier circuits is better than that of this work. However, the main contribution of the proposed circuits in this work is to solve the gate-oxide reliability issue in the mixed-voltage I/O applications with low-voltage devices. Further optimization on this work to get a better jitter performance should be involved when such a design is applied for high-precision applications.

In an SoC chip, there are often many building blocks working with different VDD voltage levels, such as the digital part is typically supplied with 1-V VDD and the analog part is supplied with 2.5-V VDD in a given 90-nm CMOS process. Moreover, the I/O circuits are often requested to be tolerant to signal voltage level of 3.3 V (or even up to 5 V). To support such SoC applications with different signal voltage levels, the semiconductor foundry has provided the transistors with multiple gate-oxide thickness by adding the corresponding additional mask layers into the CMOS process flow. However, the increase of mask layers also causes the increase on the fabrication cost of a chip. The more process steps corresponding to the increased mask layers also cause some yield loss due to the increased opportunity to defect or particle pollution during wafer fabrication, which will in turn increase the fabrication cost of a chip. Therefore, some circuit solutions have been strongly requested by IC design houses to use the low-VDD devices for high-VDD-tolerant circuit applications. Typically, the mixed-voltage I/O circuits realized with only low-VDD devices have been widely used in IC industry [5]. Moreover, the analog circuits were also designed with only low-VDD devices for high-voltage-tolerant applications to save chip fabrication cost [18].

In this study, two $2 \times$ VDD-tolerant crystal oscillator circuits have been realized with only $1 \times$ VDD devices in a 90-nm CMOS process. With the circuit design skill of NMOS-blocking technique [7], even a $3 \times$ VDD-tolerant crystal oscillator circuit can be further developed and realized with only $1 \times$ VDD devices.

VII. Conclusion

Two new mixed-voltage-tolerant crystal oscillator circuits realized with low-voltage CMOS devices have been proposed and successfully verified in a 90-nm CMOS process, which can be operated correctly without suffering gate-oxide reliability issue in the mixed-voltage interface applications. This circuit design solution can be extended to other different mixed-voltage interfaces for chip fabrication in the advanced nanoscale CMOS processes.

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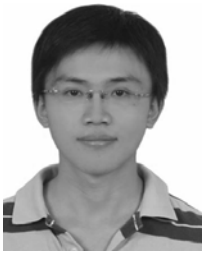

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