Design of High-Voltage-Tolerant ESD Protection Circuit in Low-Voltage CMOS Processes

Ming-Dou Ker, *Fellow, IEEE*, and Chang-Tzu Wang, *Student Member, IEEE*

***Abstract*—Two new electrostatic discharge (ESD) protection design by using only 1 × VDD low-voltage devices for mixed-voltage I/O buffer with 3 × VDD input tolerance are proposed. Two different special high-voltage-tolerant ESD detection circuits are designed with substrate-triggered technique to improve ESD protection efficiency of ESD clamp device. These two ESD detection circuits with different design concepts both have effective driving capability to trigger the ESD clamp device on. These ESD protection designs have been successfully verified in two different 0.13-μm 1.2-V CMOS processes to provide excellent on-chip ESD protection for 1.2-V/3.3-V mixed-voltage I/O buffers.**

***Index Terms*—Electrostatic discharge (ESD), low-voltage CMOS, mixed-voltage I/O, substrate-triggered technique.**

I. Introduction

With the decrease of the power supply voltage for low-power applications, the thickness of gate oxide in advanced CMOS technologies has been scaled down to improve circuit performance and to meet the gate-oxide reliability. For whole system integration, the I/O buffers may drive or receive high-voltage signals to communicate with other ICs in the microelectronic system. However, the traditional I/O buffers will suffer from gate-oxide reliability and leakage current path when the I/O buffers receive high-voltage signals. Therefore, the I/O buffers should be designed with consideration on high-voltage tolerance to prevent overstress voltage on the thinner gate oxide of the devices in I/O buffers [1]–[3]. To avoid gate-oxide reliability issue without using additional thick gate oxide process, the stacked NMOS configuration has been widely used in the mixed-voltage I/O buffers. However, the stacked NMOS configuration usually has a lower electrostatic discharge (ESD) level and slow turn-on speed of the parasitic lateral n-p-n device, as compared with the single NMOS [4], [5]. The disadvantages result from the longer base width of the lateral n-p-n BJT in the stacked NMOS devices. Therefore, additional ESD protection design must be provided to protect the stacked NMOS in the mixed-voltage I/O buffer without additional leakage current path [6].

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The mixed-voltage I/O buffer to receive 3 × VDD input signals by using only 1 × VDD low-voltage devices without suffering gate-oxide reliability issue has been proposed [7]. Nevertheless, the ESD protection design for such a 3 × VDD-tolerant mixed-voltage I/O buffer was not considered. To achieve a good whole-chip ESD protection scheme for the mixed-voltage I/O applications, it is required to design the low leakage power-rail ESD clamp circuit with only low-voltage devices that can sustain the high power-supply voltage without suffering gate-oxide reliability [8]–[11]. Recently, the ESD protection scheme for the 3.3-V mixed-voltage I/O buffers with 1-V/2.5-V dual gate low-voltage devices has been successfully verified in 0.13-μm CMOS process [10]. However, this prior design still needs extra mask-set to implement the thick gate-oxide devices (2.5-V devices). Therefore, how to design an effective ESD protection circuit with only low-voltage devices without suffering gate-oxide reliability for mixed-voltage I/O buffer with 3 × VDD input tolerance is a significant challenge.

In this paper, two new high-voltage-tolerant ESD protection designs realized with only 1 × VDD low-voltage devices to protect the mixed-voltage I/O buffer with 3 × VDD input tolerance are proposed [12], [13]. These new ESD protection designs have different efficient ESD detection circuit to trigger on the ESD clamp device, so that the turn-on efficiency of ESD clamp device can be significantly improved. The proposed ESD protection design has been successfully verified in two different 0.13-μm 1.2-V CMOS processes.

II. ESD Protection Scheme for 3 × VDD-Tolerant Mixed-Voltage I/O Buffer

To improve ESD robustness of the mixed-voltage I/O interfaces, an ESD protection concept by using the on-chip ESD bus had been reported [14]. However, in this prior art, the gate-oxide reliability was not considered in its circuit implementation. With consideration on the gate-oxide reliability, the new ESD protection scheme for mixed-voltage I/O buffer with 3 × VDD input tolerance is shown in Fig. 1. The circuit design for 3 × VDD-tolerant I/O buffer realized with only 1 × VDD devices has been reported in [7]. In the 3 × VDD I/O buffer, the dynamic gate-bias circuit controls the gate voltages of the stacked NMOS, as shown in Fig. 1. When the I/O buffer receives a logic high (3 × VDD), the gate voltages of the stacked NMOS are biased at VDD and 2 × VDD from left to right, respectively. When operating at other receiving or transmitting modes, the stacked NMOS can also be well biased by the dynamic gate-bias circuit. Therefore, the 3 × VDD I/O buffer can tolerate 3 × VDD input signals without

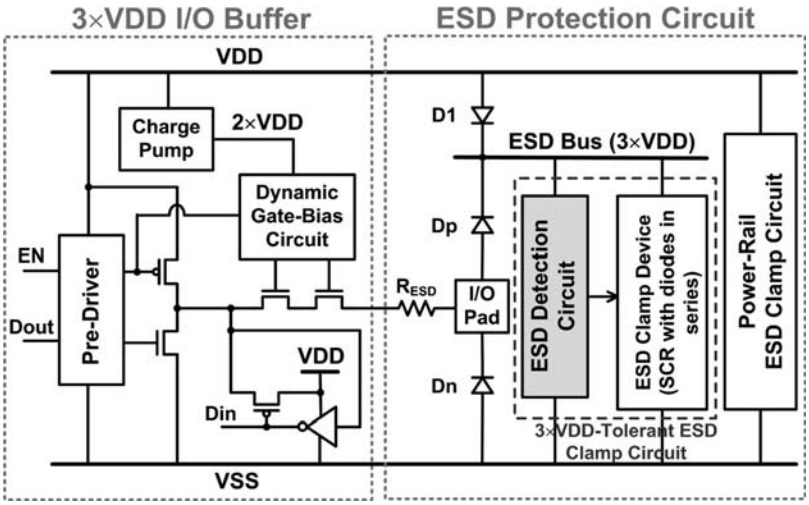

Fig. 1. Proposed ESD protection scheme for mixed-voltage I/O buffer with 3 × VDD input tolerance realized with only 1 × VDD devices.

gate-oxide reliability issue. The detailed circuit implantation to realize such dynamic gate-bias circuit, which can trace the voltage level at the I/O pad, can be found in [7].

To receive the input signals with 3.3-V voltage level, the traditional ESD protection with direct diode connection from I/O pad to VDD of 1.2 V is forbidden. Therefore, the ESD protection circuit is realized with diodes Dp, Dn, D1, ESD bus, ESD detection circuit, ESD clamp device, and the power-rail ESD clamp circuit between VDD and VSS, as shown in Fig. 1.

Under positive-to-VSS (PS-mode) ESD stress on I/O pad, the ESD current can be discharged through the diode Dp to the ESD bus and then through the ESD clamp device [silicon control rectifier (SCR)] to the grounded VSS, instead of through stacked NMOS in the I/O buffer to ground. Under positive-to-VDD (PD-mode) ESD stress on I/O pad, the ESD current can be discharged through Dp, ESD bus, and the ESD clamp device to VSS power line, and then through the power-rail ESD clamp circuit between VDD and VSS to the grounded VDD. Under negative-to-VSS (NS-mode) ESD stress on I/O pad, the negative ESD current can be discharged through the diode Dn in forward-biased condition to the grounded VSS. Under negative-to-VDD (ND-mode) ESD stress on I/O pad, the negative ESD current can be discharged through Dn to the floating VSS power line, and then through the power-rail ESD clamp circuit between VDD and VSS to the grounded VDD. The four modes of ESD stresses on the mixed-voltage I/O pad to VDD or VSS have the corresponding well-designed ESD discharging paths in the proposed ESD protection scheme.

When an ESD stress is applied to the I/O pad, the transient voltage-limiting criteria of the 3 × VDD tolerant I/O buffer can be expressed as

$$V_{\max} = I_{\mathrm{ESD}} \times R_{\mathrm{ESD}} + V_{\mathrm{BD\_NMOS}} \tag{1}$$

where $V_{\max}$ is the maximum transient voltage that the 3 × VDD I/O buffer can sustain, I_{ESD} is the ESD current, and the $V_{\mathrm{BD\_NMOS}}$ is the transient breakdown voltage of the stacked NMOS between the R_{ESD} and VSS in Fig. 1. Under the ESD stress event, all nodes in the 3 × VDD I/O buffer are floating initially. The transient breakdown voltage $V_{\mathrm{BD\_NMOS}}$ is given by the drain breakdown voltage of the stacked NMOS in the 3 × VDD I/O buffer. In order to prevent the ESD current from injecting into the 3 × VDD I/O buffer, the trigger voltage and the clamp voltage of the 3 × VDD-tolerant ESD clamp circuit should be less than $V_{\max}$. The clamp voltage of the 3 × VDD-tolerant ESD clamp circuit can be expressed as

$$V_{\mathrm{clamp}} = V_{\mathrm{D}} + V_{\mathrm{hold}} + I_{\mathrm{ESD}} \times R_{\mathrm{on}} \tag{2}$$

where V_{D} is the voltage drop across the diode Dp, V_{hold} is the holding voltage of the 3 × VDD-tolerant ESD clamp circuit, and R_{on} is the equivalent turn-on resistance of the diode Dp, parasitic routing resistance, and the 3 × VDD-tolerant ESD clamp circuit. Therefore, R_{ESD} should be designed to be slightly greater than some critical value to make sure that V_{clamp} is less than $V_{\max}$. The criterion of R_{ESD} can be found as

$$R_{\mathrm{ESD}} > R_{\mathrm{on}} + \frac{V_{\mathrm{D}} + V_{\mathrm{hold}} - V_{\mathrm{BD\_NMOS}}}{I_{\mathrm{ESD}}}. \tag{3}$$

In this paper, $V_{\mathrm{BD\_NMOS}}$ of ∼7.5 V is measured from the breakdown voltage of the stacked NMOS. For a V_{D} of 0.7 V, V_{hold} of 3.3 V, and R_{on} of 3 Ω, the resistance R_{ESD} should be greater than 0.4 and 1.7 Ω for 2 kV (I_{ESD} of 1.33 A) and 4 kV (I_{ESD} of 2.66 A) human-body-model (HBM) ESD levels, respectively. Under these criteria, the ESD current is discharged through the proposed ESD protection circuit rather than the 3 × VDD I/O buffer under ESD stress, so that the stacked NMOS in the 3 × VDD I/O buffer can be safely protected by the proposed ESD protection scheme in Fig. 1.

The power-rail ESD clamp circuit between VDD and VSS can be realized by the traditional RC-based ESD detection circuit [15]. The SCR device, which is composed of the cross-coupled n-p-n and p-n-p BJTs with regenerative feedback, with a low holding voltage can sustain a high ESD level within a small silicon area in CMOS technology [16]. However, the main concerns of SCR device as the ESD clamp device are the slow turn-on speed, high switching voltage, and latchup issue. To solve the latchup issue, several diodes are added in

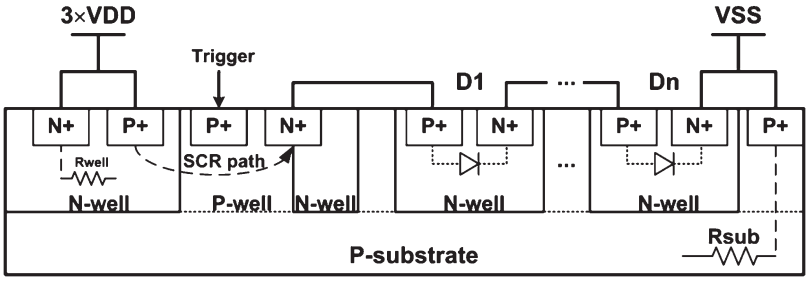

Fig. 2. Device structure of the ESD clamp device composed of substrate- triggered SCR device with diodes in series.

series with SCR as the ESD clamp device to increase its overall holding voltage for such (3.3-V) mixed-voltage I/O buffer [17]. Because these two ESD protection design were implemented in two different foundries, the electrical characteristic of SCR devices used as ESD clamp device were quite different. The holding voltage of SCR device is dominated by the doping profiles correlated with the process of each foundry, and therefore the numbers of diodes added in series with SCR for two ESD clamp circuit are different to avoid the latchup issue. In this paper, three (two) diodes are added with SCR in series to increase its overall holding voltage to approximately 4 V for such 3.3-V tolerant ESD clamp circuit A (B). The holding voltage a little higher than 3.3 V is used to overcome overshooting supply voltage. The device structure of the ESD clamp device used in these work is shown in Fig. 2. The purpose of the additional N-well region under the N+ diffusion at the cathode of the SCR device with the substrate-triggered technique is to further enhance the turn-on speed of the SCR device for better turn-on efficiency, because that can increase the equivalent substrate resistance $(R_{\rm sub})$ in this device structure.

To avoid the ESD damage on I/O buffer before ESD clamp device is turned on, the substrate-triggered technique is used to quickly trigger on the ESD clamp device. Because ESD bus line will be biased at 3.3 V through the diode Dp when 3.3-V input signals reach to the I/O pad, the ESD detection circuit connected between ESD bus and VSS must sustain the high-voltage (3.3 V) stress during normal circuit operating condition. Some ESD detection circuits proposed to increase the turn-on speed of SCR device will suffer gate-oxide reliability issue under 3.3-V bias with only 1.2-V low-voltage devices [18]. Therefore, how to design a turn-on-efficient ESD detection circuit with only 1.2-V devices to sustain 3.3-V bias becomes a quite significant challenge to this 1.2/3.3-V mixed-voltage I/O buffer.

III. 3 × VDD-Tolerant ESD Clamp Circuits

During normal circuit operating condition with 1.2-V VDD power supply and grounded VSS, when a 3 × VDD (3.3-V) input signal is applied to the I/O pad, the voltage level at the internal ESD bus will be charged up to 3.3 V through the diode Dp connected between I/O pad and ESD bus. For the convenience of easily describing the circuit operation of the 3 × VDD-tolerant ESD clamp circuit with HSPICE simulations, the ESD bus is treated as an external 3.3 V power supply in this section.

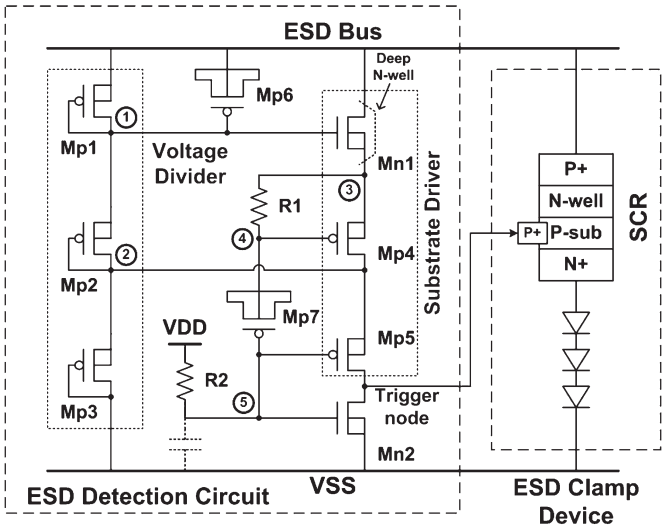

Fig. 3. Circuit implementation of the 3 × VDD-tolerant ESD clamp circuit A realized with 1 × VDD devices.

A. 3 × VDD-Tolerant ESD Clamp Circuit A

The ESD clamp circuit that can be operated under 3.3-V bias with only 1.2-V low-voltage devices is shown in Fig. 3. Under normal circuit operating condition, the diode-connected PMOS (Mp1 ∼ Mp3) are used as the voltage divider to bias the substrate driver (Mn1, Mp4, and Mp5) of the ESD detection circuit, where a deep N-well is used in Mn1 to avoid the gate-oxide overstress between gate and bulk. The NMOS (Mn2) is used to keep the voltage level of the trigger node at VSS, so the ESD clamp device is guaranteed to be kept off in the normal circuit operating condition. Here, the RC time constant of R1 and Mp7 should be designed around the order of ∼1 μs to distinguish the normal circuit operating condition from the ESD transition [11].

1) Operation Under Normal Circuit Operating Condition: During normal circuit operating condition, the node 1 and node 2 in the ESD detection circuit will be biased at 2.2 and 1.1 V, respectively. The node 5 is biased at 1.2 V through the 1-kΩ resistor of R2 to VDD, so that Mp5 is turned off. There is no trigger current generated from the ESD detection circuit into the ESD clamp device. In addition, the Mn2 in the turned-on state, whose gate is connected to VDD through the resistor of R2, can increase the noise margin of the ESD detection circuit to guarantee the ESD clamp device against false triggering during the normal circuit operating conditions. All devices in

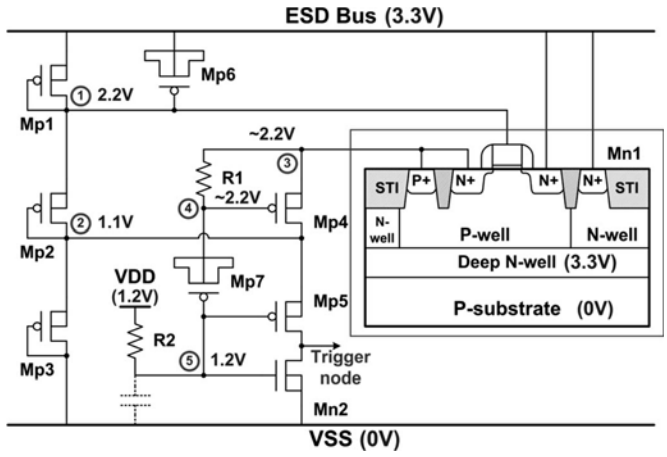

Fig. 4. Cross-sectional view of the NMOS Mn1 and the Hspice-simulated voltages at the nodes of ESD detection circuit under the normal circuit operating condition.

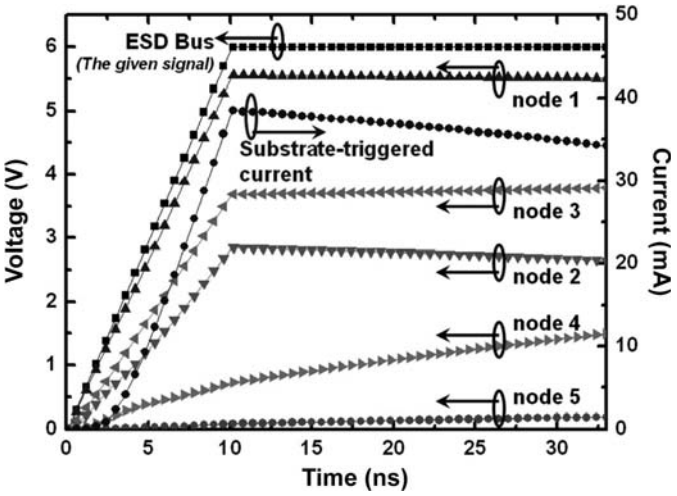

Fig. 5. Hspice-simulated voltages on the nodes of ESD detection circuit and the substrate-triggered current through Mp5 under 0-to-6 V ESD-like transition on ESD bus.

the proposed ESD detection circuit with 1.2-V gate oxide can be free from gate-oxide reliability issue under the ESD bus of 3.3 V.

In this ESD detection circuit, the drain-to-gate voltage of Mn1 is (3.3 V–2.2 V), where Mn1 is working at inversion region under the normal circuit operating conditions. However, the induced channel region of Mn1 could be insufficient to shade the strength of the electric field across the gate and bulk if its bulk region is grounded. There is somewhat gate-oxide reliability concern on Mn1 if its bulk is grounded. Therefore, to avoid this possible issue, the bulk of Mn1 is connected to its own source node. To avoid the leakage current path through the bulk (p-well) of Mn1 to the grounded p-substrate, the bulk (p-well) of Mn1 is isolated by the deep N-well with 3.3-V bias from the common p-substrate, as the diagram shown in Fig. 4. Fig. 4 also marks with the Spice-simulated voltages at the nodes of the ESD detection circuit during normal circuit operating condition. From these simulated voltages, the voltages between each two adjacent nodes of devices do not exceed their voltage limitation (1.32 V for 1.2-V devices). Therefore, the ESD detection circuit is free from the gate-oxide reliability issue.

2) Operation Under ESD Transition: When ESD voltage is applied to the I/O pad with VSS relatively grounded, such ESD transient voltage will be conducted into ESD bus through the Dp diode in forward-biased condition. Therefore, the ESD bus will have a fast rising-up ESD voltage. The capacitor (Mp6) will couple some ESD transient voltage to the node 1 to turn on Mn1 and to pull up the node 3. The RC delay from R1 and Mp7 in the ESD detection circuit will keep the gate of Mp4 (node 4) at a relatively lower voltage level (compared to the node 3) for a long time. The VDD is initially floating with an initial voltage level of 0 V during a PS-mode ESD stress at I/O pad. Some ESD transient voltage would be coupled to VDD through the parasitic capacitance during ESD zapping, but the R2 and the parasitic capacitance at the gates of Mp5 and Mn2 will hold the gate of Mp5 at a low voltage level for a long time to keep Mp5 in on state. Therefore, Mp4 and Mp5, whose initial gate voltages are at low voltage level, can be quickly turned on by ESD energy to generate the substrate-triggered current into the substrate of SCR. Then, the ESD clamp device can be quickly triggered on to discharge ESD current from ESD bus to VSS.

Fig. 5 shows the Hspice-simulated voltages and the substrate-triggered current of the ESD detection circuit under ESD transition. A 0-to-6 V ESD-like voltage pulse with a rise time of 10 ns is applied to the ESD bus to simulate the ESD transient voltage. The Spice-simulated results show that the gate voltage of Mn1 (node 1) is quickly pulled high through Mp6, whereas the gate voltage of Mp4 (node 4) is kept low due to the RC time delay from R1 and Mp7. Therefore, the ESD clamp device can be triggered on to discharge ESD current from ESD bus to VSS. The substrate driver can provide the substrate-triggered current larger than 35 mA within 10 ns when the 0-to-6 V transient voltage is applied to ESD bus, as shown in Fig. 5. By selecting the suitable device dimensions of R1, Mp7, and the substrate driver (Mn1, Mp4, and Mp5), the peak current and the period of the substrate-triggered current can be adjusted to meet different applications or specifications.

B. 3 × VDD-Tolerant ESD Clamp Circuit B

The other 3 × VDD-tolerant power-rail ESD clamp circuit, which contains ESD clamp device and ESD detection circuit with additional control, is shown in Fig. 6, where the ESD clamp device is realized by a substrate-triggered SCR with two diodes in series. The new proposed 3 × VDD-tolerant power-rail ESD clamp circuit is also realized with only 1.2-V low-voltage devices to operate at 3.3-V power supply (3 × VDD) without the risk of gate-oxide reliability.

Under normal circuit operating condition, the diode-connected PMOS (Md1~Md6) are used as the voltage divider to bias the substrate driver (Mp1, Mp2, and Mp3) and the control circuit (M1 ∼ M6, Mp4 and Mp5) of the ESD detection circuit. Here, the RC time constant of R1 and Mc1 should be designed around the order of ∼1 μs to distinguish ESD stress event from the normal circuit operating conditions. Furthermore,

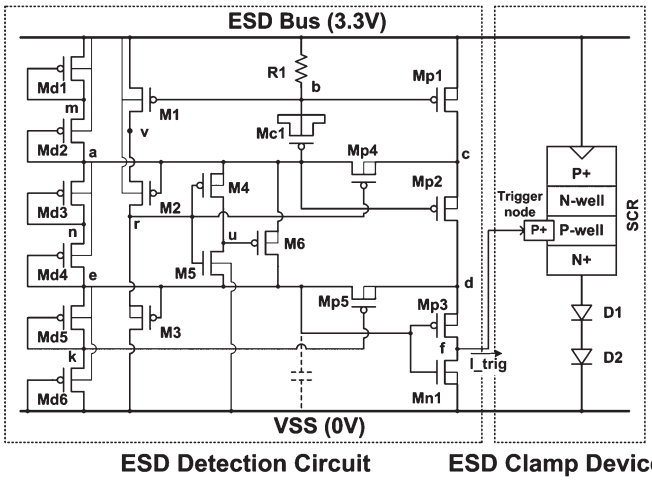

Fig. 6. Circuit implementation of the 3 × VDD-tolerant ESD clamp circuit B realized with 1 × VDD devices.

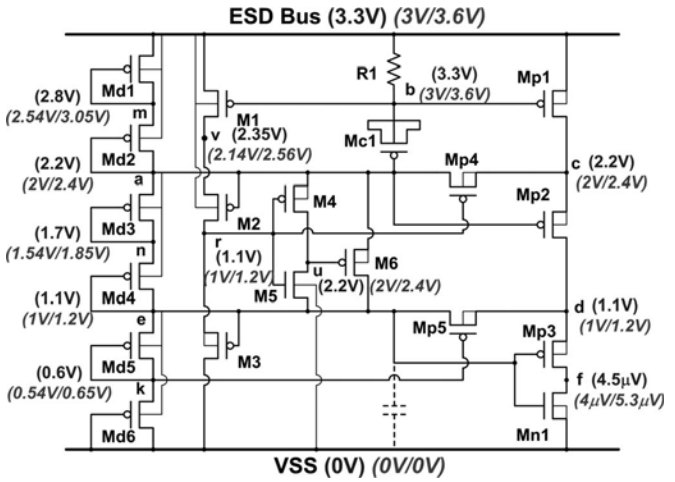

Fig. 7. Hspice-simulated voltages on nodes of the ESD detection circuit under normal circuit operating conditions with 10% voltage variation in the ESD bus line.

the special control circuit can further enhance the substrate-triggered current generated by substrate driver in ESD detection circuit.

1) Operation Under Normal Circuit Operating Condition: During the normal circuit operating condition, the node a and node e in the ESD detection circuit are biased at 2.2 and 1.1 V, respectively. The gate voltage (node k) of Mp5 will be biased at 0.6 V due to the body effect of Md6, so that Mp5 is turned on and the node d is biased at 1.1 V. The gate-to-source voltage of Mp3 is 0 V, and therefore Mp3 is turned off. There is no trigger current generated from the ESD detection circuit into the ESD clamp device. In the ESD detection circuit, the gate voltage of Mp1 and M1 is biased at 3.3 V through the resistor R1. Therefore, the Mp1 and M1 are kept in off state. Owing to the turned-off M1, there is no current path from ESD bus line through the PMOS M1, M2, and M3 to VSS, so that M2 is kept in off state. Therefore, the source-to-gate voltage of M2 is less than the threshold voltage of the 1.2-V PMOS transistor ($|$Vtp$|$), so the voltage level of node v is kept between 2.2 V (node a) and (2.2 V + $|$Vtp$|$). With the same reason, M3 is also kept in off state, and the gate voltage (node r) of M4 and Mp4 is kept between 1.1 V and (1.1 V + $|$Vtp$|$), so that M4 and Mp4 are both in on state, and therefore the voltage level of node c and node u are biased at 2.2 V. The gate-to-source voltages of M5, M6, and Mp2 are nearly 0 V, so these transistors are all in off state. In this situation, all 1.2-V devices are free from gate-oxide reliability issue under normal circuit operating condition with the ESD bus of 3.3 V.

Fig. 7 shows the Hspice-simulated voltages on the nodes of the proposed ESD detection circuit during the normal circuit operating condition with 10% variation in supply voltage of ESD bus (3 to 3.6 V). From the simulation results, the voltages across the gate-to-drain, gate-to-source, and gate-to-bulk terminals of every device in Fig. 6 do not exceed the process limitation, even if 10% voltage variation exists in ESD bus line. Therefore, the ESD detection circuit can be ensured against gate-oxide reliability issue.

2) Operation Under ESD Transition: When ESD voltage is conducted to the ESD bus line with VSS relatively grounded, the RC delay of R1 and Mc1 in the ESD detection circuit keep the gates of Mp1 and M1 (node b) at a relatively low voltage level, compared with the ESD bus line for a long time. M1 and Mp1 can be turned on, and therefore, the voltage levels at node c and node v rise rapidly. The voltage levels at node a and node e are initially floating with a voltage level of ∼0 V, so that M2 and Mp2 can be turned on, and the voltage levels at node r and node d also rise as the voltage levels at node v and node c. Mp5, whose gate voltage (node k) is relatively lower than its source voltage (node d), is in on state, and the voltage level at node e should rise with the voltage level at node d. However, the RC delay of the turn-on resistance of Mp5 and the parasitic capacitance of Mn1 keep the node e in a low voltage level to ensure that Mp3 is in the turned-on state during ESD stress event. Moreover, the gate voltage (node r) of M5 is higher than its source voltage (node e). Therefore, M5 is turned on to keep the voltage level at node u in a low voltage level as that at node e. Therefore, the gate-to-drain voltage of M6 is nearly zero to keep the voltage level at node a around the voltage level at node e plus a threshold voltage of M6, when the voltage level at node a is one threshold voltage higher than the voltage level at node u. Furthermore, the gate voltage (node r) of Mp4 is as high as its source voltage (node c), so that Mp4 is in off state to ensure that the voltage level at node a can be kept in a low voltage level compared with node c. Therefore, the substrate driver of Mp1, Mp2, and Mp3, whose gates are at relatively low voltage levels, can be quickly turned on by ESD energy to generate the substrate-triggered current into the trigger node (node f) of the SCR.

Fig. 8 shows the Hspice-simulated voltages of the ESD detection circuit under ESD stress event. A 0-to-6 V ESD-like pulse with a rise time of 10 ns is applied to the ESD bus line to simulate the ESD transient voltage. From the simulation results, such low voltage levels at node a, node b, and node e guarantee that Mp1, Mp2, and Mp3 can be turned on during ESD stress event. Therefore, the substrate-triggered current can be generated by the substrate driver into the trigger node of SCR to trigger on the ESD clamp device to discharge ESD current from the ESD bus to VSS.

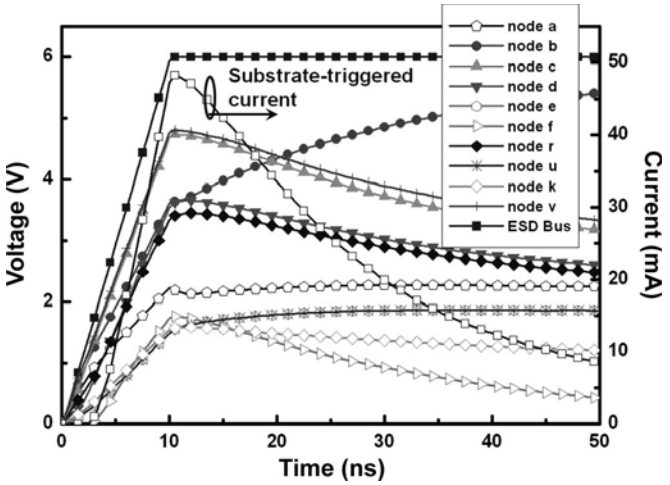

Fig. 8. Hspice-simulated voltages on the nodes of ESD detection circuit under 0-to-6 V ESD-like transition on ESD bus line (the line for node e overlaps with the line for node u).

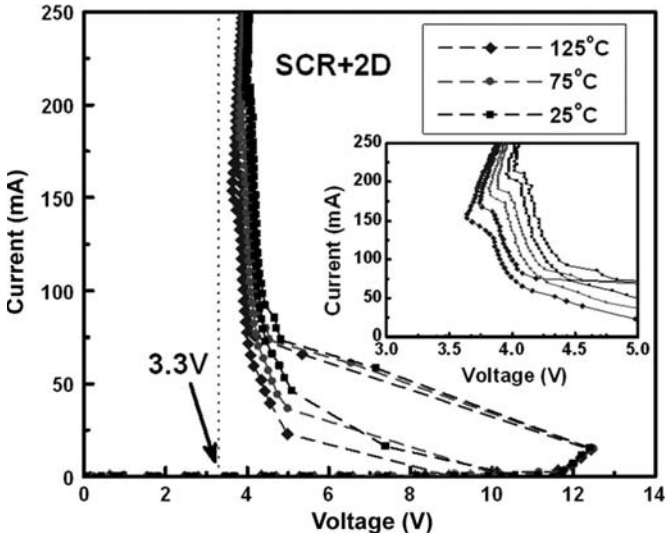

Fig. 9. Measured dc I–V characteristics of the ESD clamp device (SCR with two diodes in series) under different temperatures.

C. Discussion on 3 × VDD-Tolerant ESD Clamp Circuits

The 3 × VDD-tolerant ESD clamp circuit A seems to be easily implemented, however it needs extra mask and process steps for deep N-well formation with the additional bias connection of 1 × VDD supply. If 1 × VDD supply does not power on simultaneously with 3 × VDD supply by several microseconds or even miniseconds, the ESD detection circuit may malfunction to generate large leakage current or be damaged due to gate-oxide overstress during power-on transition. Although the 3 × VDD-tolerant ESD clamp circuit B is more complicated as compared with circuit A, it needs only conventional twin-well CMOS process to implement. Besides, it needs only 3 × VDD supply to eliminate the malfunction and gate-oxide reliability issue due to nonsimultaneous power-on transition. Furthermore, the ESD detection circuit with additional control in the 3 × VDD-tolerant ESD clamp circuit B can further enhance the detection function to ESD events rather than only using the function of RC delay.

The substrate driver in the ESD detection circuit is guaranteed to be kept in off state under the normal circuit operating condition. In this situation, the P/V/T variation could only affect the leakage current of the ESD detection circuit rather than the circuit operation. During the ESD event, any process variation might affect the triggered current generated by the substrate driver. The amount of triggered current that can trigger the SCR device on is around several milliamperes, which will be shown in the next section with measured data from silicon chip. By adjusting the device dimension in the substrate driver, the triggered current can be over designed greater than the minimum required current. Therefore, the circuit operation of ESD detection circuit can still function well under reasonable P/V/T variation in CMOS processes.

IV. Experimental Results

The proposed ESD protection circuits have been fabricated in two different 0.13-μm silicided CMOS process with only 1.2-V devices. In these proposed ESD protection circuits, the ESD detection circuits and ESD clamp devices are fully silicided. In 3 × VDD-tolerant ESD clamp circuit A, the widths of SCR in ESD clamp device are varied in 45 and 90 μm. On the other hand, the widths of SCR in ESD clamp device are varied in 30, 45, and 60 μm in 3 × VDD-tolerant ESD clamp device B.

A. DC I–V Characteristics of ESD Clamp Device

The dc I–V characteristics of the ESD clamp device (SCR with two diodes in series) in 3 × VDD-tolerant ESD clamp circuit B is measured by using Tek370 curve tracer.

To avoid the issue of false triggering and latchup, the holding voltage of the SCR-based ESD clamp device with diodes in stacked configuration must be designed to be greater than the maximum voltage level of 3 × VDD (3.3 V in 0.13-μm CMOS process) under the normal circuit operating condition. The measured dc I–V characteristics of the ESD clamp device under different temperatures are shown in Fig. 9. The inset in Fig. 9 is the enlarged view around the holding points of one SCR with two stacked diodes in series (SCR + 2-D). The holding voltages of the ESD clamp device are 3.98, 3.82, and 3.64 V under the temperatures of 25 °C, 75 °C, and 125 °C, respectively. These holding voltages are higher than the voltage level of 3 × VDD (3.3 V) under the normal circuit operating conditions. Even if the ESD clamp device was mistriggered due to noise disturbance, it can be recovered to the normal condition after the noise source is removed. Therefore, the SCR-based ESD clamp device with a suitable number of stacked diodes in series can be safely applied in 3 × VDD-tolerant ESD clamp circuit without any latchup issue.

The measured dc I–V characteristics of the ESD clamp device under different substrate-triggered currents (I_trig) into the p+ trigger node are shown in Fig. 10. The measurement setup is also shown as the inset in Fig. 10. When the SCR-based ESD clamp device has no substrate-triggered current (I_trig = 0 mA), the SCR is essentially triggered on by junction avalanche breakdown. As shown in Fig. 10, the trigger voltage of the fabricated SCR-based ESD clamp device without

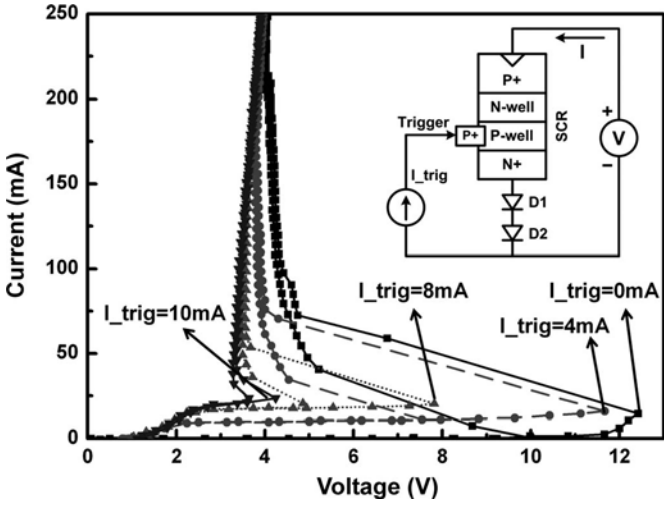

Fig. 10. Measured dc I–V characteristics of the ESD clamp device (SCR with two diodes in series) under different substrate-triggered currents (I_trig).

the substrate-triggered current is as high as ∼12.4 V, which is higher than the breakdown voltage of the stacked NMOS with $R_{\rm ESD}$ in mixed-voltage I/O buffers. However, the trigger voltage of the ESD clamp device is reduced to 8 V when the substrate-trigger current is 8 mA. Moreover, the trigger voltage of the ESD clamp device is reduced to only 4.2 V, which almost equals to the holding voltage of the ESD clamp device, when the substrate-triggered current is increased to 10 mA. The trigger voltage of the ESD clamp device is decreased while the substrate-triggered current is increased. ESD clamp device with low trigger voltage can be turned on more quickly to discharge ESD current to provide more effective protection for mixed-voltage I/O interfaces.

B. Turn-On Verification

The turn-on behavior of SCR devices is one of important factors for ESD protection, and it has been evaluated in some recent works [19]–[21]. To verify the turn-on efficiency of the proposed 3 × VDD-tolerant ESD clamp circuits, an experimental setup is shown as the inset in Fig. 11, where a voltage pulse generated from a pulse generator is used to simulate the rising edge of a PS-mode HBM ESD pulse. The voltage pulse generated from the pulse generator initially has a square-type voltage waveform with a rise time about ∼10 ns and a pulse height of 6 V, as shown in Fig. 11. When the positive voltage pulse is applied to the I/O pad of the proposed ESD protection circuit with VSS grounded, the sharp-rising edge of the ESD-like voltage pulse will start the ESD detection to generate substrate-triggered current to trigger ESD clamp device on, and provide a low-impedance path between the I/O pad and VSS. The voltage waveform on the I/O pad is therefore clamped by the turned-on ESD clamp device. The voltage waveforms, clamped by 3 × VDD-tolerant ESD clamp circuit A and B, on the I/O pad are also shown in Fig. 10. The voltage waveforms on the I/O pad are clamped by the Dp and ESD clamp device to ∼4 V, which is lower than the breakdown voltage of the stacked NMOS in the mixed-voltage I/O buffer. The time to clamp the 0-to-6 V voltage pulse to the holding voltage level (∼4 V) by the ESD clamp device is about ∼20 ns. From the measured voltage waveforms, the excellent turn-on efficiency in ESD-stress condition has been successfully verified in the proposed ESD protection circuits.

C. TLP Characteristics and ESD Robustness

To investigate the ESD level of the I/O buffer with or without ESD protection circuit during ESD stress event, transmission line pulse (TLP) generator with a pulsewidth of 100 ns, and a rise time of ∼10 ns is used to measured the second breakdown current (It2) of the ESD protection circuit. The HBM ESD levels and machine-model (MM) ESD levels are measured by KeyTek ZapMaster Mk.2, and the failure criterion is defined as the I–V characteristic curve shifting over 20% from its original curve after three continuous ESD zaps at every ESD test level.

1) ESD Protection Design With 3 × VDD-Tolerant ESD Clamp Circuit A: The TLP-measured second breakdown current and HBM ESD level of the I/O buffer with and without the proposed ESD protection design with 3 × VDD-tolerant ESD clamp circuit A under PS-mode ESD stress are compared in Table I. When the width of SCR device in ESD clamp device is 45 μm, the secondary breakdown current of the I/O buffer with the proposed ESD protection design and 3 × VDD-tolerant ESD clamp circuit A can be increased from 0.2 to 4 A, as comparing with the I/O buffer without ESD protection. In addition, the HBM ESD level of the I/O buffer with the proposed ESD protection design can be improved from 500 V to 6 kV. When the width of SCR device in ESD clamp device is increased to 90 μm, the second breakdown current and HBM ESD level of the I/O buffer with the proposed ESD protection scheme can be further increased larger than 6 A and 8 kV, respectively. The proposed ESD protection design can significantly improve the second breakdown current and HBM ESD level of the 3 × VDD-tolerant I/O buffer.

2) ESD Protection Design With 3 × VDD-Tolerant ESD Clamp Circuit B: The TLP-measured I–V characteristics of the ESD clamp device with or without ESD detection circuit of 3 × VDD-tolerant ESD clamp circuit B under PS-mode ESD stress are shown in Fig. 12, where the width of the SCR in ESD clamp device is 60 μm. From the measured results, the trigger voltage of ESD clamp device without ESD detection circuit is 12.7 V, whereas the trigger voltage of ESD clamp device can be reduced to only 4.6 V by ESD detection circuit without involving the junction avalanche breakdown. Therefore, the trigger voltage of ESD clamp device can be significantly reduced by the proposed ESD detection circuit to ensure effective ESD protection.

The second breakdown current and the turn-on resistance of the ESD protection circuit with a 60-μm-wide SCR and two diodes in series is 5.31 A and ∼1.9 Ω, respectively. The standby leakage current under 3.3-V bias of the whole ESD protection circuit is only 83 nA. By adjusting the width of the ESD clamp device and the size of the substrate driver in ESD detection circuit, the second breakdown current, turn-on resistance, and the trigger voltage of the ESD protection circuit can be modified to satisfy the specification of different mixed-voltage I/O circuits. The HBM ESD levels and MM ESD levels

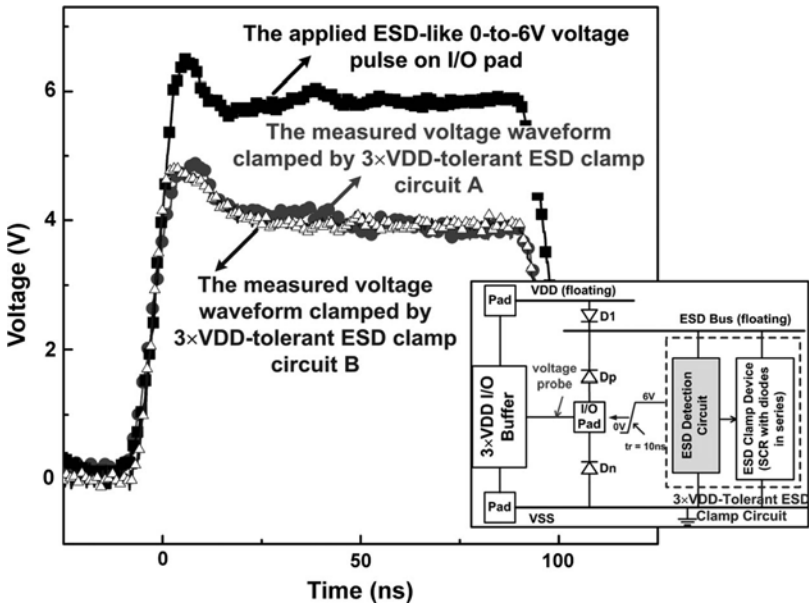

Fig. 11. Measured voltage waveforms, clamped by 3 × VDD-tolerant ESD clamp circuit A and B, on the I/O pad when a 0-to-6 V voltage pulse is applying to I/O pad under the PS-mode ESD stress (VDD floating and VSS grounded).

TABLE I
ESD ROBUSTNESS OF I/O BUFFER WITH OR WITHOUT ESD PROTECTION CIRCUIT WITH ESD CLAMP CIRCUIT A

3×VDD-Tolerant I/O Buffer	It2	HBM ESD Level
I/O Buffer without ESD Protection Circuit	0.2A	<500V
I/O Buffer with ESD Protection Circuit A (SCR Width = 45μm)	4A	6kV
I/O Buffer with ESD Protection Circuit A (SCR Width = 90μm)	>6A	>8kV

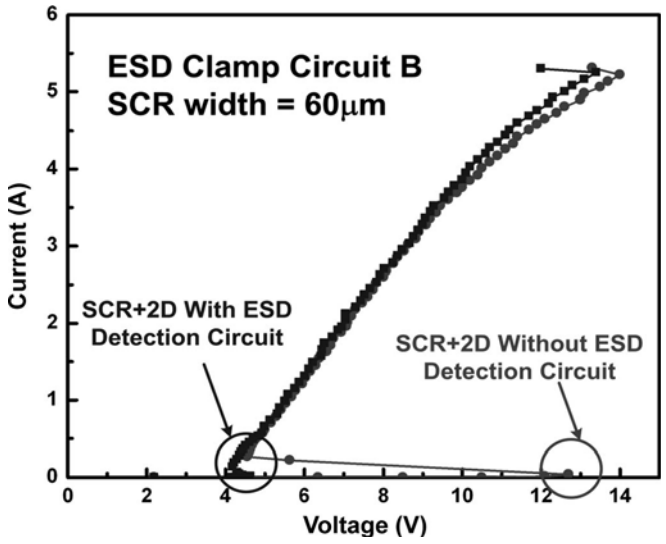

Fig. 12. Measured TLP I–V characteristics of the ESD clamp device in the 3 × VDD-tolerant ESD clamp circuit B with or without ESD detection circuit under PS-mode ESD stress.

of the proposed ESD protection circuit with 3 × VDD-tolerant ESD clamp circuit B with various widths of SCR-based ESD clamp devices under PS-mode ESD stress are listed in Table II.

TABLE II
ESD ROBUSTNESS OF THE PROPOSED ESD PROTECTION CIRCUIT WITH ESD CLAMP CIRCUIT B WITH VARIOUS WIDTHS OF ESD CLAMP DEVICES

ESD clamp device width (μm)	HBM ESD Level	MM ESD Level	It2
30	4kV	260V	2.56A
45	6.2kV	380V	3.82A
60	>8kV	440V	5.31A

The HBM ESD levels of ESD protection circuit under ESD clamp device width of 30, 45, and 60 μm are 4 kV, 6.2 kV, and larger than 8 kV, respectively. Besides, the MM ESD levels of ESD protection circuit under ESD clamp device width of 30, 45, and 60 μm are 260, 380, and 440 V, respectively. The corresponding second breakdown current measured by TLP is also listed in Table II.

The CDM ESD robustness of the proposed ESD protection circuits are also verified by KeyTek RCDM tester. The 3 × VDD-tolerant I/O buffer protected by the proposed ESD protection circuits in this paper (both 3 × VDD-tolerant ESD clamp circuits A and B) can achieve a CDM ESD level of greater than ±1 kV.

V. PIN-TO-PIN ESD PROTECTION

In the whole chip ESD protection design, the proposed 3 × VDD-tolerant ESD protection circuit can be shared with other 3 × VDD-tolerant I/O buffers by connecting ESD bus to each other to achieve pin-to-pin ESD protection, as shown in Fig. 13. During the pin-to-pin ESD test, the ESD stress is applied to one I/O pad with other I/O pad grounded, where the VDD and VSS are initially floating. The ESD current will flow from one I/O pad through the forward diode Dp, ESD bus line, and then through the proposed 3 × VDD-tolerant ESD clamp circuit to the VSS line, finally from the VSS line through the

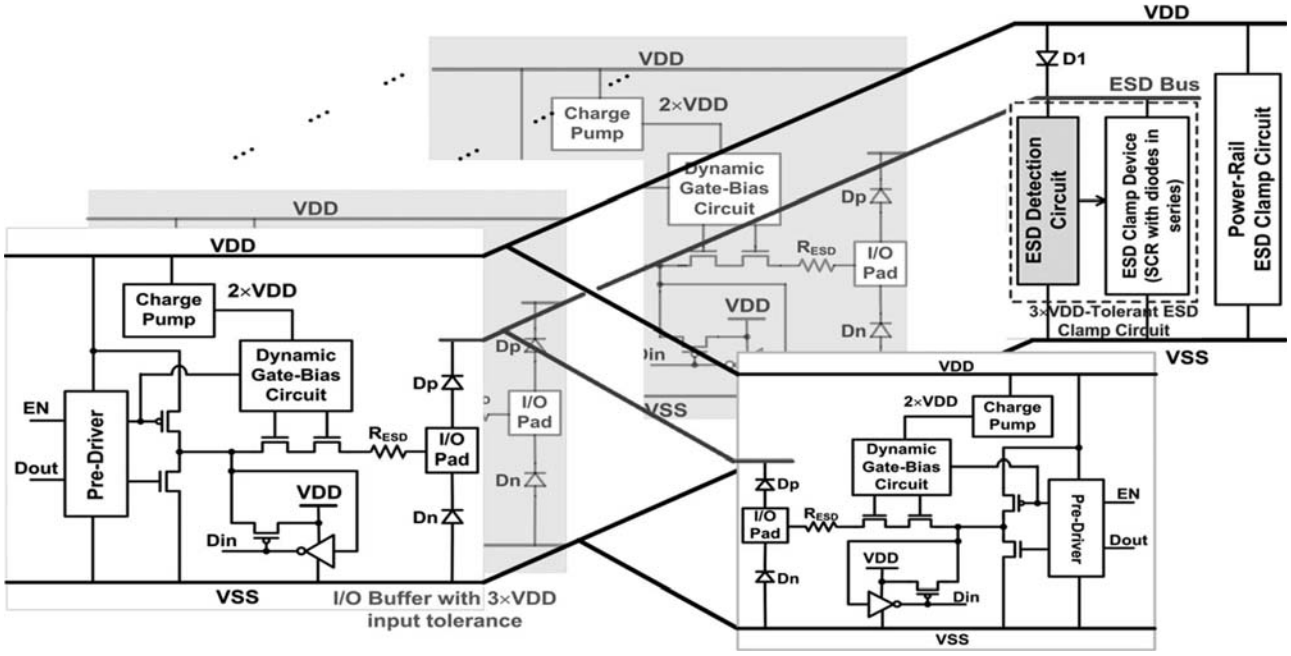

Fig. 13. Shared ESD bus and 3 × VDD-tolerant ESD clamp circuit for whole set of I/O buffers to achieve pin-to-pin ESD protection.

forward diode Dn to the other grounded I/O pad. Therefore, the pin-to-pin ESD protection can be achieved by using this ESD protection scheme with the proposed 3 × VDD-tolerant ESD clamp circuit for 3 × VDD-tolerant mixed-voltage I/O buffers.

VI. Conclusion

Two novel circuit solutions on ESD protection design, realized with 1 × VDD devices for mixed-voltage I/O buffer with 3 × VDD input tolerance, have been successfully verified in two different 0.13-μm 1.2-V CMOS process. The four-mode (PS, NS, PD, and ND) ESD stresses and pin-to-pin ESD stresses on the 1.2/3.3-V mixed-voltage I/O buffer can be effectively discharged by the ESD protection scheme, with the proposed 3 × VDD-tolerant power-rail ESD clamp circuits. The proposed 3 × VDD-tolerant power-rail ESD clamp circuits operates without gate-oxide reliability issue under the normal circuit operating conditions. By using the special control circuit in the 3 × VDD-tolerant ESD clamp circuit B, the device sizes of the resistor, capacitor, and the substrate driver can be reduced. Therefore, the active area and the standby leakage current of the ESD detection circuit in 3 × VDD-tolerant ESD clamp circuit B can be further reduced. In addition, the ESD detection circuit has also shown significant help on reducing the trigger voltage of ESD clamp device. The turn-on behaviors of the ESD clamp device have been measured to verify the effectiveness of the ESD detection circuit for both two 3 × VDD-tolerant ESD clamp circuits. The experimental results have also confirmed that the ESD robustness of the 3 × VDD mixed-voltage I/O buffer can be significantly increased up to 8 kV with the proposed ESD protection designs. These two proposed power-rail ESD clamp circuit with the advantages of low leakage current, high ESD robustness, and no gate-oxide reliability issue are the excellent ESD protection solutions to the mixed-voltage I/O interfaces with high-voltage input/output signals.

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