A 5-GHz Differential Low-Noise Amplifier With High Pin-to-Pin ESD Robustness in a 130-nm CMOS Process

Yuan-Wen Hsiao, *Member, IEEE*, and Ming-Dou Ker, *Fellow, IEEE*

***Abstract*—Two electrostatic discharge (ESD)-protected 5-GHz differential low-noise amplifiers (LNAs) are presented with consideration of pin-to-pin ESD protection. The pin-to-pin ESD issue for differential LNAs is addressed for the first time in the literature. Fabricated in a 130-nm CMOS process, both ESD-protected LNAs consume 10.3 mW under 1.2-V power supply. The first LNA with double-diode ESD protection scheme exhibits the power gain of 17.9 dB and noise figure of 2.43 dB at 5 GHz. Its human-body-model (HBM) and machine-model (MM) ESD levels are 2.5 kV and 200 V, respectively. With the same total parasitic capacitance from ESD protection devices, the second LNA with the proposed double silicon-controlled rectifier (SCR) ESD protection scheme has 6.5-kV HBM and 500-V MM ESD robustness, 17.9-dB power gain, and 2.54-dB noise figure at 5 GHz. The ESD test results have shown that the pin-to-pin ESD test is the most critical ESD-test pin combination for the conventional double-diode ESD protection scheme. With the proposed double-SCR ESD protection scheme, the pin-to-pin ESD robustness can be significantly improved without degrading RF performance. Experimental results have shown that the ESD protection circuit for LNA can be co-designed with the input matching network to simultaneously achieve excellent ESD robustness and RF performance.**

***Index Terms*—Electrostatic discharge (ESD), low-noise amplifier (LNA), power-rail ESD clamp circuit, RF integrated circuit (RF IC), silicon-controlled rectifier (SCR), substrate-triggered technique.**

I. Introduction

RF integrated circuits (RF ICs) are necessary for all portable electronics devices used for wireless communications. Early RF front-ends were implemented by using SiGe or GaAs technologies because of their superior high-frequency characteristics. Recently, the feature size of MOS transistor in CMOS technology has been continuously scaled down to improve its high-frequency characteristics, which makes CMOS processes more attractive to implement RF ICs. With the advantages of high integration capability and low cost for mass production, RF ICs operating in gigahertz frequency bands have been fabricated in CMOS technology. In an RF receiver, the low-noise amplifier (LNA) plays a very important role because it is the first stage in the RF receiver. There are several requirements on the performance of LNA. First, the noise figure of LNA should be minimized because the noise figure of the LNA dominates the overall noise figure of the RF receiver. Besides, the power gain of the LNA should be high enough to suppress the negative effects caused by the noise figures of the following stages in the RF receiver. Moreover, the power consumption of all components in the RF receiver, including the LNA, should be minimized to make the RF receiver suitable for portable use.

A differential configuration is popular for LNA design because the differential LNA has the advantages of common-mode noise rejection, less sensitivity to substrate noise, supply noise, and bond-wire inductance variation [1]–[7]. In addition, the differential output signals of the differential LNA can be directly connected to the differential inputs of the double balanced mixer.

Electrostatic discharge (ESD), which has been the most important reliability issue in integrated circuit (IC) fabrication, is getting more attention in nanoscale CMOS technology [8]. With the advances of CMOS processes, ESD robustness of CMOS ICs becomes worse and worse because of the thinner gate oxide of MOS transistors. Therefore, ESD protection should be taken into consideration during the design phase of all commercial ICs, especially in RF ICs [9]. Since the LNA is usually connected to the external of the RF receiver chip, such as the off-chip antenna, on-chip ESD protection circuits are needed for all input pads of the LNA. However, applying ESD protection circuits at the input pads introduce impacts to RF performance. As the operating frequency of RF circuits increases, degradation on RF performance due to the parasitic effects from ESD protection devices/circuits becomes serious. Therefore, the LNA and ESD protection circuit have to be co-designed to simultaneously optimize RF performance and ESD robustness.

There are several ESD protection designs reported for narrowband LNAs [10]–[15]. The typical ESD protection design with diodes at the input pad and the power-rail ESD clamp circuit had been verified [10]. To further reduce the equivalent parasitic capacitance from ESD protection devices at the input pad, the ESD protection diodes in a stacked configuration had been reported [11]. Besides diodes, inductor had been used as the ESD protection device in a 5-GHz LNA [12]. The inductance of the ESD protection inductor was designed to resonate

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with the parasitic capacitance at the selected RF operating frequency. With the parallel *LC* network resonating at the RF operating frequency, the shunt impedance of the ESD protection circuit becomes very large and the RF performance degradation can be reduced [13]. With a similar concept, an alternative design was also reported [14]. The ESD protection inductor can be connected between the ground pad VSS and the input pad, while a diode is added between the input pad and the power pad VDD. Moreover, the *LC* tanks, which resonate at the RF operating frequency, can be used between the input pad and VDD, as well as between the input pad and VSS, respectively [15].

Besides positive-to-VDD (PD mode), positive-to-VSS (PS mode), negative-to-VDD (ND mode), and negative-to-VSS (NS mode) ESD-test pin combinations, the pin-to-pin ESD test had been earlier specified in the ESD-test standards to verify ESD robustness of the differential input stages. During the pin-to-pin ESD stress, the ESD voltage is applied to one input pin with the other input pin relatively grounded, and all the other pins including all VDD and VSS pins are floating [16]. To provide efficient pin-to-pin ESD protection, the ESD protection device should be turned on quickly with low enough clamping voltage during ESD stresses to protect the thin gate oxides of the differential input transistors. As the gate oxide becomes much thinner in nanoscale CMOS processes, robust ESD protection design against all ESD-test pin combinations, including pin-to-pin ESD stresses, becomes more challenging. However, pin-to-pin ESD protection was not mentioned in those previous studies.

In this paper, three 5-GHz differential LNAs are designed and verified in a 130-nm CMOS process. The basic (as reference) LNA was designed and fabricated without ESD protection for comparison. The other two LNAs were co-designed with the double diode and the proposed double silicon-controlled rectifier (SCR) ESD protection schemes, respectively. Moreover, the pin-to-pin ESD issue for differential LNAs is specially studied clearly in this paper with failure analysis pictures after ESD stresses. Section II is focused on the LNA design. On-chip ESD protection designs for the differential LNA are presented in Section III. The experimental results are reported in Section IV. Moreover, the measured results of three differential LNAs in this work are compared with those of the prior CMOS differential LNAs.

II. LNA

The circuit schematic of the reference LNA without ESD protection is shown in Fig. 1. The architecture of common-source inductive degeneration is applied to match the source impedance ($R_S = 50\,\Omega$) at resonance. The operating frequency of the LNA was targeted at 5 GHz. Good isolation between the input and output is achieved by using the cascode configuration. Moreover, cascode configuration provides good stability and reduces the Miller effect [17]. The dimensions of the input NMOS transistors M_1 and M_3 were designed according to the compromise between noise figure and power consumption. For the ESD-protected LNAs, the ESD protection device was placed at each input pad. With the equivalent input network of the half circuit of the ESD-protected differential LNA, the RF metrics such as input impedance, power gain, and noise figure of the ESD-protected LNA can be analyzed [18].

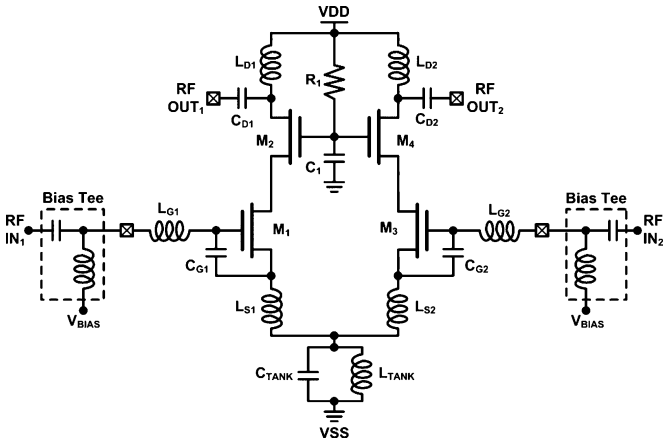

Fig. 1. Reference differential LNA without ESD protection.

The *LC* tank consisting of $L_{\rm TANK}$ and $C_{\rm TANK}$ is used to enhance the common-mode rejection. All of the active and passive devices are fully integrated in the experimental test chip fabricated in a 130-nm CMOS process. In order to verify the intrinsic ESD protection capability of the on-chip ESD protection circuits at the input pads, the ac coupling capacitor between the input pad and the gate inductor is not realized in the test chip because the ac coupling capacitor connected to the input pad can block some ESD energy when the input pad is stressed by ESD. Thus, the off-chip bias tee is needed to combine the RF input signal and the dc bias at the input node during RF performance measurement.

III. ESD Protection Design for LNA

A. Substrate-Triggered SCR

SCR had been demonstrated to be suitable for ESD protection design for RF ICs because it has both high ESD robustness and low parasitic capacitance under a small layout area [7], [19], [20]. The P-type substrate-triggered SCR (P-STSCR) and N-type substrate-triggered SCR (N-STSCR) are utilized in this work to protect LNA against ESD stresses. The cross-sectional view of the P-STSCR is shown in Fig. 2(a). The SCR path exists among the $\rm P+$ diffusion (anode), N-well, P-well, and $\rm N+$ diffusion (cathode). The equivalent circuit of the P-STSCR is shown in Fig. 2(b), which consists of a parasitic vertical PNP bipolar junction transistor (BJT) and a parasitic lateral NPN BJT. The PNP BJT $Q_{\rm PNP}$ is formed by the $\rm P+$ diffusion (anode), N-well, and P-well. The NPN BJT $Q_{\rm NPN}$ is formed by the N-well, P-well, and $\rm N+$ diffusion (cathode). When the P-STSCR is used as the ESD protection device at the input pad, the cathode and P-well are connected to VSS, while the anode and N-well are connected to the input pad and VDD, respectively. In this configuration, the P+N-well junction can be used to protect the input pad against PD-mode ESD stresses, and its parasitic capacitance is added at the input pad. To quickly turn on the P-STSCR during ESD stresses, the $\rm P+$ trigger diffusion (in the P-well region) was added between the anode and cathode. An extra ESD detection circuit is designed to inject trigger current to the P-trigger node during ESD stresses.

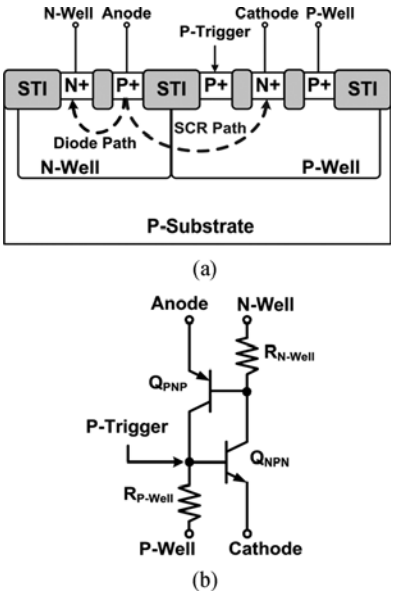

Fig. 2. (a) Cross-sectional view of P-STSCR. (b) Equivalent circuit of P-STSCR.

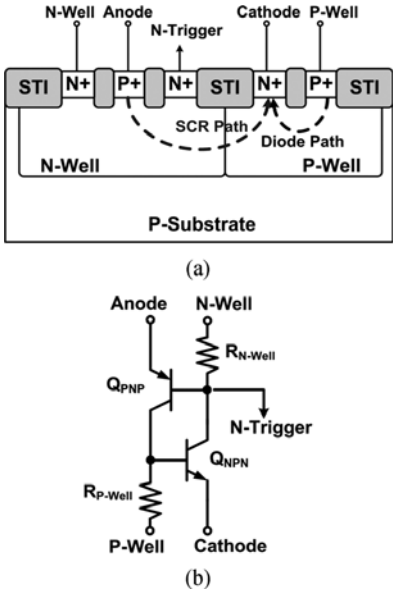

Fig. 3. (a) Cross-sectional view of N-STSCR. (b) Equivalent circuit of N-STSCR.

During PS-mode ESD stress, the trigger current is designed to be injected to the P-trigger node from the ESD detection circuit. After the voltage drop across the P-well resistance $(R_{\mathrm{P-Well}})$ is larger than the cut-in voltage of the base-emitter junction of Q_{NPN}, Q_{NPN} is turned on to conduct the ESD current, which leads to voltage drop across the N-well resistance $(R_{\mathrm{N\text{-}Well}})$. When the voltage drop across $R_{\mathrm{N\text{-}Well}}$ is larger than the cut-in voltage of the base–emitter junction of Q_{PNP}, Q_{PNP} is turned on to conduct ESD current, which causes more collector current of Q_{NPN} due to the current gain of BJT. The regenerative positive-feedback mechanism results in the great current handing capability of the SCR, and makes the SCR very robust against ESD stresses. With the low clamping voltage of the SCR, the ESD current path between the input pad and VSS is provided to protect the gate oxide of MOS transistors.

The cross-sectional view and equivalent circuit of the N-STSCR are shown in Fig. 3(a) and (b), respectively. The SCR path exists among the $\mathrm{P}+$ diffusion (anode), N-well, P-well, and $\mathrm{N}+$ diffusion (cathode). When the N-STSCR is used to protect the input pad, the anode and N-well are connected to the VDD, while the cathode and P-well are connected to the input pad and VSS, respectively. In this configuration, the $\mathrm{N}+\mathrm{P}$-well junction can be used to protect the input pad against NS-mode ESD stresses, and its parasitic capacitance is added at the input pad. To quickly turn on the N-STSCR during ESD stresses, the $\mathrm{N}+$ trigger diffusion (in the N-well region) was added between the anode and cathode. During ND-mode ESD stress, the trigger current is design to be drawn from the N-trigger node by an extra ESD detection circuit to turn on the N-STSCR. Similarly, the turned-on N-STSCR is quite robust against ESD stresses. Hence, the input pad is protected by the N-STSCR under ND-mode ESD stresses.

B. Power-Rail ESD Clamp Circuit

As shown in Fig. 4, the power-rail ESD clamp circuit includes the P-STSCR and ESD detection circuit. The anode and N-well of the P-STSCR are connected to VDD, while the cathode and P-well of the P-STSCR are connected to the VSS. The ESD detection circuit consists of an *RC* timer and an inverter. The resistor R_2 and capacitor C_2 form the *RC* timer with the time constant of 0.3 μs, which can distinguish the ESD transients from the normal circuit operating conditions [21]. During normal circuit operating conditions, the node between R_2 and C_2 is charged to high potential (VDD). Since NMOS M_{N} is turned on and PMOS M_{P} is turned off, the P-trigger node is tied to the VSS and no trigger current is injected. During ESD stresses, the ESD energy is coupled to the VDD quickly. With the *RC* delay provided by R_2 and C_2, the gate voltages of M_{P} and M_{N} are initially at low potential $(\sim 0\ \mathrm{V})$. Therefore, M_{P} is turned on to inject trigger current into the P-trigger node. As a result, the P-STSCR is turned on to provide ESD current path between the VDD and VSS.

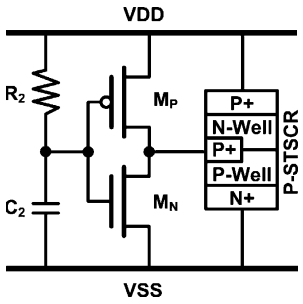

Fig. 4. Power-rail ESD clamp circuit realized with P-STSCR.

The power-rail ESD clamp circuit is placed between the VDD and VSS, which does not contribute parasitic capacitance to the input or output pads of RF ICs. Thus, the size of the P-STSCR in the power-rail ESD clamp circuit is not limited by the specification of parasitic capacitance.

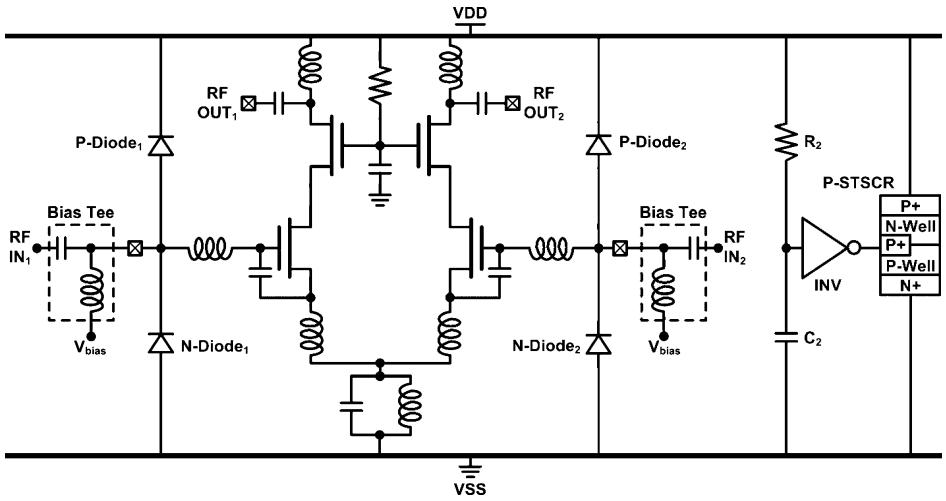

Fig. 5. Differential LNA with the double-diode ESD protection scheme.

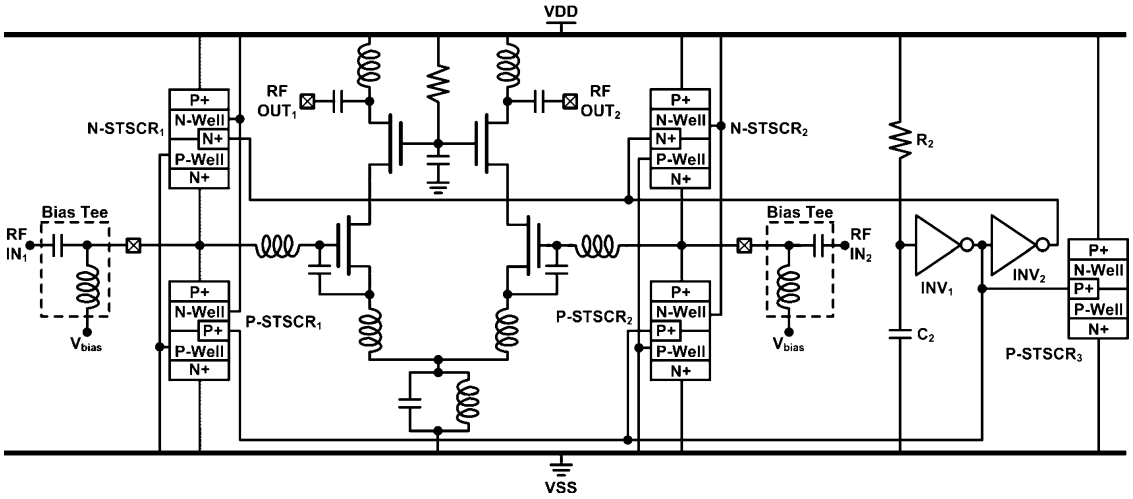

Fig. 6. Differential LNA with the proposed double-SCR ESD protection scheme.

C. ESD-Protected LNAs

In this work, two ESD protection schemes, which are the double-diode ESD protection scheme and the proposed double-SCR ESD protection scheme, were designed and applied to protect LNAs. The total parasitic capacitances of these two ESD protection schemes at each input pad are chosen to be the same amount, which is 300 fF, to investigate their ESD robustness. With the same total parasitic capacitance from ESD protection devices at the input pad, the RF performance and ESD robustness of these two LNAs with different ESD protection schemes can be compared. Both ESD-protected LNAs have the same power-rail ESD clamp circuit implemented with P-STSCR.

The circuit schematic of the LNA with a double-diode ESD protection scheme is shown in Fig. 5. The double-diode ESD protection scheme includes a $\mathrm{P}+\mathrm{N}$-well diode (P-diode) between each differential input pad and VDD, and an $\mathrm{N}+\mathrm{P}$-well diode (N-diode) between the VSS and each differential input pad. To achieve the total parasitic capacitance of 300 fF contributed by these two ESD protection diodes at each input pad, two parallel $\mathrm{P}+\mathrm{N}$-well diodes with the dimensions of 16 μm $\times$ 5 μm and two parallel $\mathrm{N}+\mathrm{P}$-well diodes with the dimensions of 19.2 μm $\times$ 5 μm were used. To co-design the LNA and ESD protection circuit, the source inductors (L_{S1} and L_{S2}) and gate inductors (L_{G1} and L_{G2}) need to be adjusted to achieve input matching at RF operating frequency after the addition of ESD protection diodes.

The circuit schematic of the LNA with the proposed double-SCR ESD protection scheme is shown in Fig. 6. The P- and N-diodes in the LNA with double-diode ESD protection scheme are replaced with the N-STSCRs and P-STSCRs, respectively. To meet the requirement of 300-fF total parasitic capacitance at each input pad, the anode diffusion size of the P-STSCR and the cathode diffusion size of the N-STSCR are 60 μm $\times$ 2.4 μm and 60 μm $\times$ 2.7 μm, respectively. Similarly, the input matching network was co-designed with the SCRs to accomplish satisfaction on RF performance after ESD protection circuit was inserted. Since $\mathrm{P}-\mathrm{STSCR}_1$ and $\mathrm{P}-\mathrm{STSCR}_2$ are the same type of device as that used in the power-rail ESD clamp circuit, the ESD detection circuit in the power-rail ESD clamp circuit can also serve as the ESD detection circuit for the P-STSCR at each input pad. To realize the ESD detection circuit for the N-STSCR, the inverter INV_2 was cascaded to the inverter INV_1, which is a

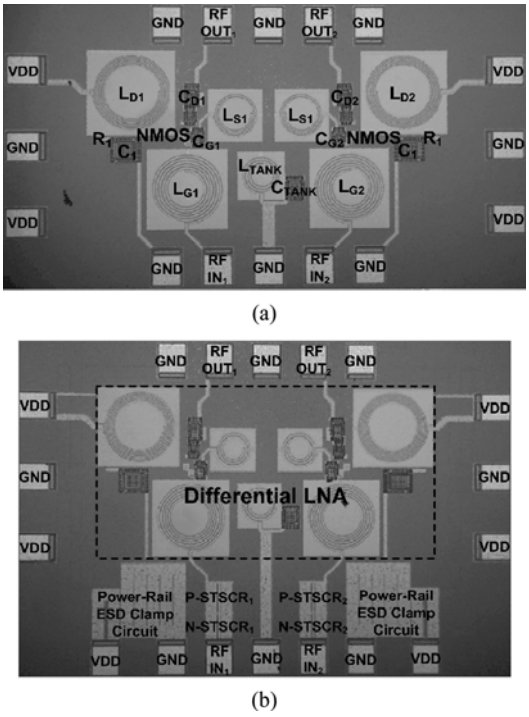

Fig. 7. Chip micrographs of: (a) reference LNA without ESD protection and (b) LNA with the proposed double-SCR ESD protection scheme.

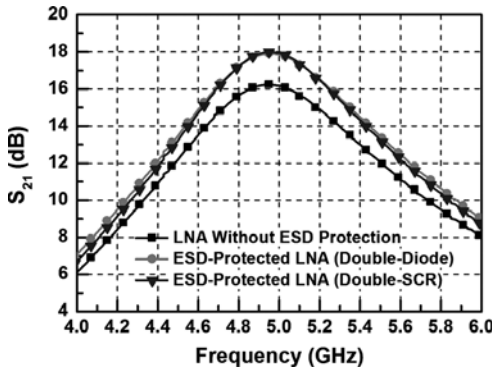

Fig. 8. Measured S_{21}-parameters (power gain) among the reference LNA and two ESD-protected LNAs.

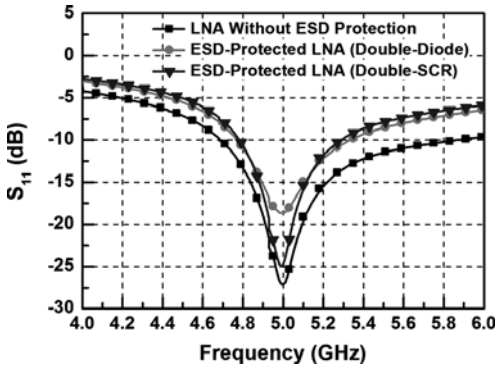

Fig. 9. Measured S_{11}-parameters (input reflection) among the reference LNA and two ESD-protected LNAs.

part of the ESD detection circuit for the P-STSCR. With the *RC* delay provided by the *RC* timer at the input node of INV_1, the input of INV_1 is initially at low potential ($\sim$ 0 V), which leads to the high potential (VDD) at the input of INV_2 during ESD stresses. Thus, the NMOS in INV_2 is turned on to draw the trigger current to turn on the N-STSCR during ESD stresses.

After the ESD protection circuit is applied to LNA, the passive impedance matching network is re-designed to match the input and output of the LNA to the source impedance with the matching structure unchanged. The dimensions of the cascoded NMOS transistors in three LNAs are identical, and only the dimensions of the passive devices are different. For the LNA, the S-parameters and noise figure are the main factors to determine RF performance. With the LNA and ESD protection co-design, the simulated results show that good S-parameters can be achieved after the ESD protection circuit is inserted. However, applying the ESD protection circuits at the input pads inevitably degrades the noise figure of the ESD-protected LNA.

IV. Experimental Results

The reference LNA without ESD protection and the other two LNAs with double-diode and double-SCR ESD protection schemes had been fabricated in the same experimental test chip in a 130-nm CMOS process. The chip micrographs of the reference LNA and the LNA with a double-SCR ESD protection scheme are shown in Fig. 7(a) and (b), respectively. The reference LNA occupies the area of 1070 μm $\times$ 630 μm, and the circuit area of each ESD-protected LNA is 1090 μm $\times$ 750 μm. On-wafer measurements were performed to characterize the RF performance and ESD robustness. Each LNA consumes 10.3 mW under 1.2-V power supply. In Sections IV-A–C, the measured RF performances, including the S-parameters, noise figures, and third-order intercept points (IP3s) of the three fabricated LNAs are reported and compared. The human-body-model (HBM) and machine-model (MM) ESD levels of the LNAs are evaluated and discussed. Moreover, the failure mechanism under ESD stresses is also investigated with failure analysis.

A. Measured Results on RF Performance

To measure the S-parameters of differential LNAs, on-wafer four-port S-parameter measurement with an Agilent E8361A network analyzer was performed. The measurement system converted the measured four-port S-parameters to the differential two-port S-parameters. Fig. 8 shows the measured S_{21}-parameters of the three fabricated LNAs. The measured results show that these three LNAs have their best S-parameters at about 5 GHz. The power gain of the reference LNA is 16.2 dB at 5 GHz, while these two ESD-protected LNAs exhibit the power gain of 17.9 dB. The measured S_{11}-parameters are compared in Fig. 9. All of the fabricated LNAs have the S_{11}-parameter of less than -18 dB at 5 GHz. The reference LNA and the ESD-protected LNAs achieve the best input matching at the same frequency. The same operating frequency can be achieved after adding the ESD protection circuits as long as the parasitic effects caused by ESD protection circuits can be well characterized. As shown in Fig. 10, the measured S_{22}-parameters deviate from the simulated results. Since the designed drain capacitance is quite small, it is sensitive to the parasitic effects at the output node and drain inductor. Therefore, the parasitic effects degrade output matching. The reference LNA

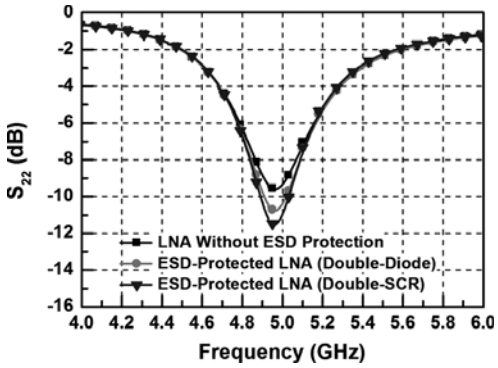

Fig. 10. Measured S_{22}-parameters (output reflection) among the reference LNA and two ESD-protected LNAs.

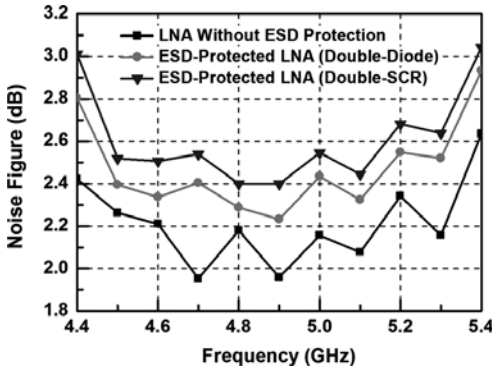

Fig. 11. Measured noise figures among the reference LNA and two ESD-protected LNAs.

exhibits the S_{22}-parameter of -9.3 dB at 5 GHz, whereas these two ESD-protected LNAs have the S_{22}-parameters of less than -10 dB. The measured S_{12}-parameters of these three LNAs are better than -28 dB because good reverse isolation is one of the attributes in the cascode configuration.

The noise figures were measured by using an Agilent N8975A noise figure analyzer with an Agilent 346C noise source. The measured noise figures are shown in Fig. 11. The reference LNA has the best noise figure, which is 2.16 dB at 5 GHz. With the ESD protection circuits, the LNA with double-diode and double-SCR ESD protection schemes have the noise figures of 2.43 and 2.54 dB, respectively. The increase in the noise figures of the ESD-protected LNAs is caused by the addition of ESD protection devices. The IP3 was measured by the two-tone test with 5- and 5.005-GHz signals. An Agilent E8247C signal generator and Agilent E4407B spectrum analyzer were used in the two-tone test. The input-referred third-order intercept point (IIP3) value is -12.5 dBm for these three LNAs. There is no significant difference on RF performances, except noise figure among these three fabricated LNAs, which demonstrates the effectiveness of the co-design with LNA and ESD protection.

B. ESD Robustness

With different ESD protection schemes, the ESD levels of these three LNAs are expected to be different even though the total parasitic capacitances of ESD protection devices are identical. To compare the ESD levels of these three LNAs, the HBM and MM ESD tests have been performed [22], [23]. The failure criterion is 30% voltage shift under 1-μA current bias. The measured HBM and MM ESD levels of these three LNAs under different ESD-test pin combinations are listed in Table I. When the input pin was tested, the reference LNA was very vulnerable to ESD, which failed at 50- and 10-V ESD stresses in HBM and MM ESD tests, respectively. The LNA with the double-diode ESD protection scheme has HBM and MM ESD levels of 2.5 kV and 200 V, respectively. The ESD test results have shown that the pin-to-pin ESD test is the most critical ESD-test pin combination for the conventional double-diode ESD protection scheme. With the proposed double-SCR ESD protection scheme, the HBM and MM ESD levels of the LNA are significantly improved to 6.5 kV and 500 V, respectively. Moreover, the pin-to-pin ESD test is no longer the most critical ESD-test pin combination for the LNA with the proposed double-SCR ESD protection scheme. The VDD-to-VSS ESD test was also used to verify the power-rail ESD clamp circuit. Both of the ESD-protected LNAs can sustain the VDD-to-VSS ESD stress of over 8 kV and over 1 kV in HBM and MM ESD tests, respectively.

TABLE I
HBM AND MM ESD ROBUSTNESS UNDER DIFFERENT TEST PIN COMBINATIONS

ESD Robustness	LNA Without ESD Protection		ESD-Protected LNA (Double-Diode)		ESD-Protected LNA (Double-SCR)	
	HBM	MM	HBM	MM	HBM	MM
Positive to VSS	< 50 V	< 10 V	3 kV	250 V	6.5 kV	500 V
Positive to VDD	< 50 V	< 10 V	7 kV	550 V	> 8 kV	950 V
Negative to VSS	< 50 V	< 10 V	7 kV	550 V	> 8 kV	900 V
Negative to VDD	< 50 V	< 10 V	7 kV	400 V	7.5 kV	700 V
Pin to Pin	< 50 V	< 10 V	2.5 kV	200 V	> 8 kV	550 V
VDD to VSS	0.5 kV	< 10 V	> 8 kV	> 1000 V	> 8 kV	> 1000 V

In the double-diode ESD protection scheme, the positive (negative) ESD voltage is coupled from the input pad to VDD (VSS) through the P-diode (N-diode) to turn on the power-rail ESD clamp circuit during PS-mode (ND-mode) ESD stresses. In the proposed double-SCR ESD protection scheme, the positive (negative) ESD voltage is coupled from the input pad to VDD (VSS) through the parasitic $\mathrm{P}+\mathrm{N}$-well diode in the P-STSCR (parasitic $\mathrm{N}+\mathrm{P}$-well diode in the N-STSCR) to enable the ESD detection circuit to turn on the P-STSCR (N-STSCR) during PS-mode (ND-mode) ESD stresses. During PS- and ND-mode ESD stresses, the ESD current path consists of a diode and an SCR in the double-diode ESD protection scheme, whereas only an SCR is needed to bypass ESD current in the proposed double-SCR ESD protection scheme. Fewer ESD protection devices along the ESD current path indicates lower ESD clamping voltage and higher ESD robustness. Under PD- and NS-mode ESD tests, the ESD current paths in the double-diode and proposed double-SCR ESD protection schemes all consist of only a forward-biased diode, so their ESD levels are higher than those under PS- and ND-mode ESD tests.

During pin-to-pin ESD stresses, the ESD pulse is applied to one differential input pad with the other differential input pad grounded. Both VDD and VSS pads are floating. The ESD current paths in these two ESD protection schemes are shown in Fig. 12. In Fig. 12(a), the ESD current is first conducted from the zapped pad to VDD through $\mathrm{P}-\mathrm{diode}_1$. Besides, VSS initially has a voltage level near to ground because it is connected to the grounded input pad through $\mathrm{N}-\mathrm{diode}_2$. Thus, the

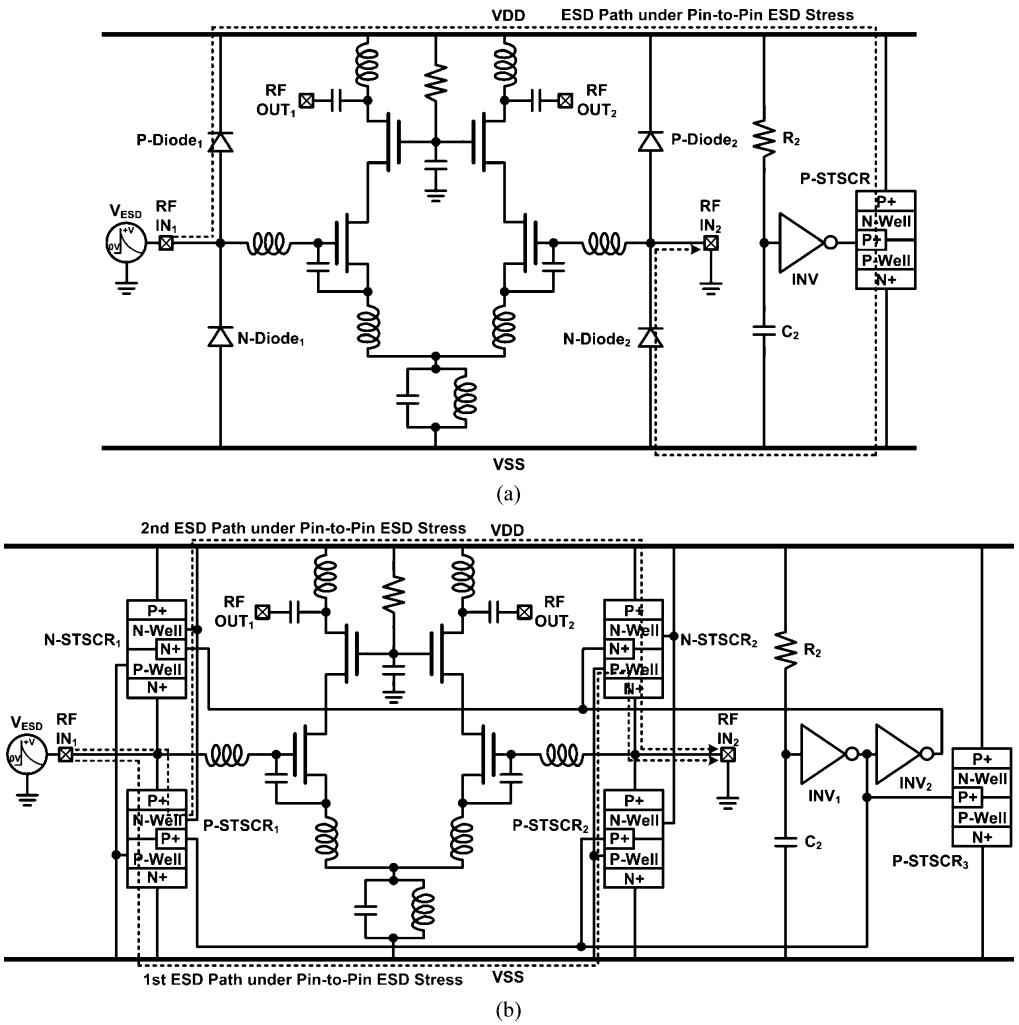

Fig. 12. ESD current paths under pin-to-pin ESD stress in: (a) LNA with the double-diode ESD protection scheme and (b) LNA with the proposed double-SCR ESD protection scheme.

pin-to-pin ESD-stress voltage across these two differential pins becomes across VDD and VSS, and the power-rail ESD clamp circuit is turned on to conduct ESD current from VDD to VSS. Consequently, the ESD current path consists of $\mathrm{P-diode_1}$, P-STSCR, and $\mathrm{N-diode_2}$ in the double-diode ESD protection scheme. In the proposed double-SCR ESD protection scheme, all of the SCR devices are turned on during pin-to-pin ESD stresses, as shown in Fig. 12(b). There are two ESD current paths with lower clamping voltage, which includes only the voltage drop across a diode and an SCR. The first ESD current path is through $\mathrm{P-STSCR_1}$ and the parasitic $\mathrm{N+P}$-well diode in $\mathrm{N-STSCR_2}$, and the second one is through the parasitic $\mathrm{P+N}$-well diode in $\mathrm{P-STSCR_1}$ and $\mathrm{N-STSCR_2}$. Except lower clamping voltage along the current path, the proposed double- SCR ESD protection scheme has more ESD current paths than the double-diode ESD protection scheme. Therefore, the LNA with the proposed double-SCR ESD protection scheme sustains much higher pin-to-pin ESD robustness ($>$ 8 kV in HBM and 550 V in MM) than that (2.5 kV in HBM and 200 V in MM) of the LNA with a double-diode ESD protection scheme.

In the differential LNA with the proposed double-SCR ESD protection scheme, $\mathrm{P-STSCR_3}$ in the power-rail ESD clamp circuit can also be turned on under pin-to-pin ESD stresses. However, since the power-rail ESD clamp circuit is far from the stressed pads, the speed and efficiency to bypass the ESD current through $\mathrm{P-STSCR_3}$ is delayed and degraded by the parasitic resistance of the power lines. Besides, the voltage drop along this ESD current path consists of the voltage drop of two forward-biased diodes (parasitic $\mathrm{P+N}$-well diode in $\mathrm{P-STSCR_1}$ and parasitic $\mathrm{N+P}$-well diode in $\mathrm{N-STSCR_2}$) and a turned-on SCR ($\mathrm{P-STSCR_3}$). However, the voltage drop along the first or second ESD paths shown in Fig. 12(b) consists of the voltage drop of only a forward-biased diode and a turned-on SCR. Due to the higher voltage drop, the ESD current path along $\mathrm{P-STSCR_3}$ in the double-SCR ESD protection scheme is negligible under the pin-to-pin ESD stress.

Table II summarizes the measured performances of the three fabricated LNAs and compares the performances with those of the prior CMOS differential LNAs. In this paper, the pin-to-pin ESD robustness of the differential LNA is first investigated. Among the previous differential LNAs, several works were not equipped with the ESD protection circuit [1]–[3], [5]. Among the ESD-protected differential LNAs, the diode is the most popular ESD protection device at the input pad of the LNA, because it is easy to implement [4], [7]. In this work, the SCR is proposed as the ESD protection device at the input pads of the differential

TABLE II
COMPARISON WITH CMOS DIFFERENTIAL LNAs

Topology	Process	f_0 (GHz)	VDD (V)	P_{DC} (mW)	NF (dB)	S_{21} (dB)	S_{11} (dB)	S_{22} (dB)	IIP3 (dBm)	HBM ESD Level (kV)	MM ESD Level (V)
LNA Without ESD Protection	130-nm CMOS	5	1.2	10.3	2.16	16.2	-27.2	-9.3	-12.5	< 0.05	< 10
ESD-Protected LNA (Double-Diode)	130-nm CMOS	5	1.2	10.3	2.43	17.9	-18.7	-10.4	-12.5	2.5	200
ESD-Protected LNA (Double-SCR)	130-nm CMOS	5	1.2	10.3	2.54	17.9	-24.8	-10.9	-12.5	6.5	500
Transformer-Feedback LNA [1]	180-nm CMOS	5.75	1	16	0.9	14.2	N/A	-8	0.9	N/A	N/A
Gain-Controlled LNA With Current Reuse [2]	180-nm CMOS	5.8	1.8	14.4	3.7	12.5	-15	-9	-0.45	N/A	N/A
Capacitor Cross-Coupled Common-Gate LNA [3]	180-nm CMOS	6	1.8	6.48	3	7.1	-10	-7.3	11.4	N/A	N/A
Two-Stage Feedback LNA+PGA [4]	130-nm CMOS	3 - 5	1.5	45	4	25.8	-11	N/A	-13	1.5	N/A
LNA With LC-Ladder Input Network [5]	130-nm CMOS	2 - 4.6	1.5	16.5	3.5	9.5	-10	N/A	-0.8	N/A	N/A
Packaged and Inductorless Wideband LNA [6]	90-nm CMOS	0.1 - 8	1.4	16	3.4	17	-10	N/A	-9	2.25	N/A
2-Stage AC-Coupled Pseudo-Differential LNA [7]	130-nm CMOS	18	1.5	36	4.1	22.4	-7	-17	-5.6	2	N/A

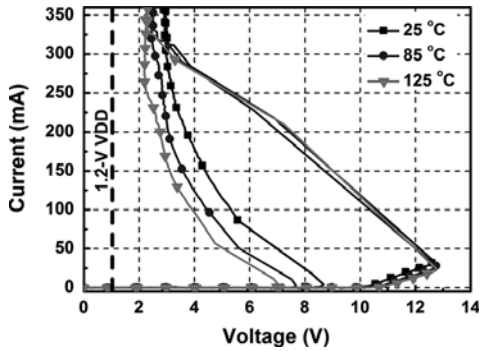

Fig. 13. Measured dc *I–V* curves of the standalone SCR device under different temperatures.

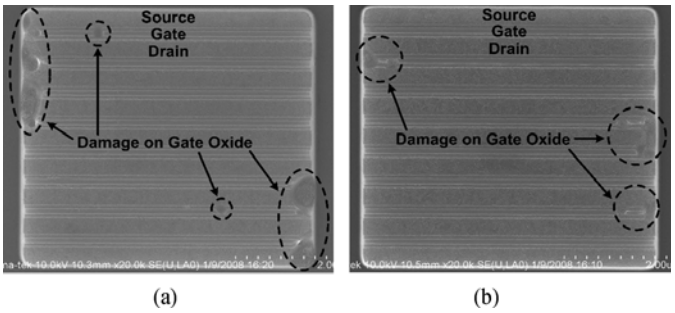

Fig. 14. SEM photograph at the failure points of: (a) LNA with double-diode ESD protection scheme after 3-kV HBM pin-to-pin ESD test and (b) LNA with double-SCR ESD protection scheme after 7-kV HBM PS-mode ESD test. The failure locations are all located at the gate oxide of input NMOS M_1 of the LNA circuit.

LNA because the SCR is expected to be capable of sustaining higher ESD robustness than the diode under the same parasitic capacitance. Experimental results have shown that the ESD robustness of the differential LNA with the proposed double-SCR ESD protection scheme is significantly higher than that of the differential LNA with the double-diode ESD protection scheme. Besides, the RF performance is not degraded when the SCR is used as the input ESD protection device. Thus, the proposed double-SCR ESD protection scheme is very suitable for ESD protection design for RF front-end circuits.

The dc *I–V* curves of the standalone SCR device were measured using Tektronics 370B curve tracer. As shown in Fig. 13, the holding voltages of the SCR device under 25 °C, 85 °C, and 125 °C are 2.84, 2.58, and 2.38 V, respectively. Since the holding voltage of the SCR device is higher than the power-supply voltage of 1.2 V, the SCR device can be used for ESD protection without a latchup issue. Fig. 13 shows that the standalone SCR device has the trigger voltage of more than 10 V, which is too high to protect the LNA. Thus, the trigger voltage needs to be reduced by injecting trigger current into the P-STSCR or drawing trigger current from the N-STSCR. With the ESD detection circuit in this work, the trigger voltage of SCR devices can be substantially reduced to efficiently protect the LNA.

C. Failure Analysis

Compared with the standalone ESD protection device, the ESD-protected LNAs still have lower ESD levels. Therefore, it is expected that the failure could be located on the gate oxide of the input NMOS, which is connected to the input pad. The scanning electron microscope (SEM) pictures in Fig. 14 have confirmed the ESD failure location of the ESD-protected LNAs after ESD stresses. The failure locations of ESD damage during

all ESD-test modes are at the gate oxide of the input NMOS whose gate is connected to the zapped pad. This failure mechanism indicates that even if the ESD protection device does not fail, the overshooting voltage across the gate oxide is so large to cause damage at the gate oxide. The ESD clamping voltage should be further lowered to prevent such internal ESD damages because the gate–oxide breakdown voltage is decreasing as the CMOS technology is scaled down.

V. Conclusion

Two ESD protection schemes for a 5-GHz differential LNA have been verified in a 130-nm CMOS process. Both ESD protection schemes have the same parasitic capacitance of 300 fF at each input pad. With the LNA and ESD protection co-design, the RF performances of the ESD-protected LNAs have only little degradation as compared with the reference LNA. However, the ESD robustness of the LNA is substantially improved by the proposed on-chip ESD protection circuit. Moreover, the pin-to-pin ESD robustness of the gigahertz differential LNA is investigated in this paper for the first time. The 5-GHz differential LNA with a double-diode ESD protection scheme exhibits the power consumption of 10.3 mW, power gain of 17.9 dB, input matching of -18.7 dB, noise figure of 2.43 dB, as well as 2.5-kV HBM and 200-V MM ESD robustness The ESD robustness of the double-diode ESD-protected LNA is dominated by the most critical ESD-test combination, which is the pin-to-pin ESD test. With the same power consumption and power gain, the 5-GHz differential LNA with the proposed double-SCR ESD protection scheme features the input matching of -24.8 dB, noise figure of 2.54 dB, as well as 6.5-kV HBM and 500-V MM ESD robustness. The LNA with the proposed double-SCR ESD protection scheme can especially sustain the HBM and MM pin-to-pin ESD stress of over 8 kV and 550 V, respectively. Hence, the ESD protection schemes proposed in this paper can be successfully co-designed with the LNA to achieve good RF performance and high ESD robustness simultaneously.

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