Implementation of delta–sigma analog-to-digital converter in LTPS process

Chia-Chi Tsai
Tzu-Ming Wang (SID Student Member)
Ming-Dou Ker

Abstract — An on-panel delta–sigma analog-to-digital converter (ADC) has been implemented and verified for 3-μm low-temperature polysilicon (LTPS) technology with two basic blocks: a delta–sigma modulator and a decimation filter. From the experimental results, the digital output from the delta–sigma modulator is correctly matched with the analog input voltage ratio such that the digital output can be converted into 8-bit digital code successfully under a supply voltage of 10 V from the decimation filter. The implemented on-panel delta–sigma ADC can be used for the application of temperature-to-digital converter on glass substrate.

Keywords — *Delta–sigma, analog-to-digital converter (ADC), low-temperature polysilicon (LTPS), system-on-panel (SOP).*

DOI # 10.1889/JSID18.11.904

1 Introduction

Recently, low-temperature polycrystalline-silicon (LTPS) thin-film transistors (TFTs) have been studied extensively for active-matrix liquid-crystal-display (AMLCD) applications. The pioneering TFT circuit work had been reported in Ref. 1. Compared with amorphous-silicon TFTs (a-Si TFTs), LTPS TFTs have several orders of magnitude higher electron mobility.[2] Consequently, liquid-crystal-display (LCD) panels utilizing LTPS technology are expected to become a dominant display technology in the small-to-medium-sized display market.[3] Furthermore, LTPS technology can achieve a slim, compact, and high-resolution display by integrating the driving circuits onto the peripheral area of the display. Such a technology will also be more suitable for the realization of system-on-panel (SOP) applications.

To gain the advantages of SOP applications, some researchers had reported the integration of all control and driving circuits into the display panel.[4–6] An 8-bit CPU containing 13,000 TFTs on glass substrate was reported to demonstrate the feasibility of SOP.[7] In Ref. 8, the touch-panel function fully integrated in a 2.45-in. a-Si QVGA TFT-LCD was reported to detect the capacitance change of the liquid crystal in LCDs. In Ref. 9, the temperature coefficient of polysilicon TFTs and their application on a voltage reference circuit with temperature compensation in the LTPS process had been proposed. Moreover, ADCs have been widely used in the interface of the analog sensing circuits and digital-processing circuits, such as the touch-panel system or the thermal compensation system, to convert the analog signals into digital signals.[10–12] Thus, integration of ADC on glass substrate is a value-added approach to SOP applications.

For silicon CMOS technology, the delta-sigma ADC has been widely used in the IC industry. With a small amount of analog circuitry, in the frequency range from the kilohertz scale to the hundreds of kilohertz scale, the delta-sigma ADC is very economically competitive with other types of data converters, such as the pipeline ADC or the flash ADC, for high-resolution applications.[13–15] Although the delta–sigma ADC had been reported and realized for silicon CMOS technology, the delta–sigma ADC realized on glass substrate with LTPS technology was never reported in the literature.

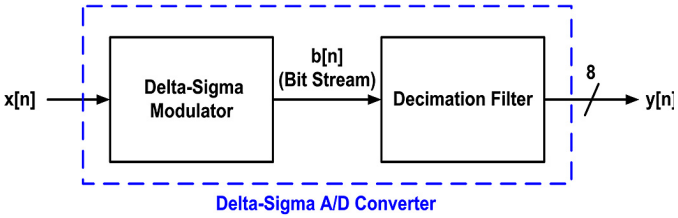

FIGURE 1 — Basic block diagram of delta–sigma ADC.

In this work, a delta–sigma ADC designed with TFTs on glass substrate has been proposed and successfully verified for a 3-μm LTPS process,[16] and the proposed delta–sigma ADC is designed for temperature-to-digital converter application on glass substrate in combination with an on-panel bandgap reference circuit.[9] Compared with Ref. 16, more detailed explanations of design and circuit theory in this work has been added in Secs. 2 and 3. Furthermore, the measured results of the whole delta–sigma ADC (delta–sigma modulator and decimation filter) and among 10 different panels have also been appended in Sec. 4.

2 Design and realization of delta–sigma modulator

The proposed delta-sigma ADC is composed of two basic blocks: a delta–sigma modulator and a decimation filter, as shown in Fig. 1.[17] One analog input $x[n]$ enters the modula-

Received 04/27/10; accepted 08/02/10.
C-C. Tsai and T-M. Wang are with the Nanoelectronics and Gigascale Systems Laboratory, Institute of Electronics, National Chiao Tung University, 1001 Ta-Hsueh Rd., Hsinchu, Taiwan 200, ROC.
M-D. Ker is with the Nanoelectronics and Gigascale Systems Laboratory, Institute of Electronics, National Chiao Tung University, and the Department of Electronic Engineering, I-Shou University, Kaohsuing, Taiwan, ROC; e-mail: mdker@ieee.org.

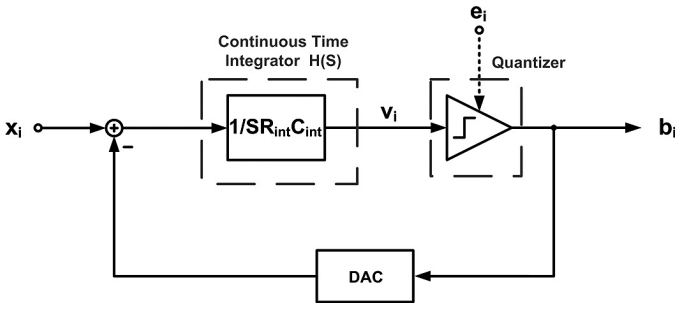

FIGURE 2 — Block diagram of delta–sigma modulator.

tor with a sampling rate 8–512 times higher than the Nyquist rate (2 MHz/256).

2.1 Theoretical operation

Figure 2 shows a block diagram of the delta–sigma modulator which consists of an integrator, a comparator, and a digital-to-analog converter (DAC). b_i is

$$b_i = x_{i-1} + (e_i - e_{i-1}). \tag{1}$$

In addition, the transfer function of the continuous time integrator can be derived as

$$H(S) = \frac{1}{s \cdot R_{\text{int}} \cdot C_{\text{int}}}. \tag{2}$$

where $R_{\text{int}} = R_{\text{int1}} = R_{\text{int2}}$ and $C_{\text{int}} = C_{\text{int1}} = C_{\text{int2}}$ as shown in Fig. 3.

The quantization noise e generated by the comparator, which is approximated as a white-noise source, is shaped by the high-pass function $\{1/[1 + H(s)]\}$. In this case, the input/output characteristic of the DAC consists of only two levels to ensure the inherent linear operation of DAC.

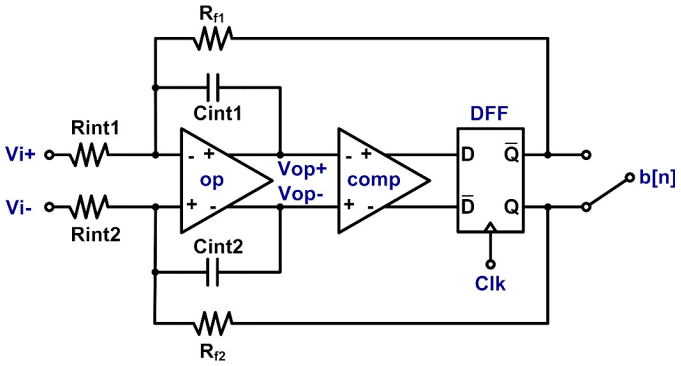

FIGURE 3 — Circuit implementation of the delta–sigma modulator on glass substrate for 3-μm LTPS technology.

In addition, the relationship between x, output bit stream b, and the output of the integrator v in Fig. 2 can be expressed as

$$v_{i+1} = x_i - b_i + v_i. \tag{3}$$

Equation (3) can be used to generate the sequences v and b from a given input x with the initial condition of v_0. For example, in Table 1, x_i is 4 V and v_0 is 1 V, the probability of "Logic-1" in the bit stream is 0.4 (2/5), which is exactly equal to the ratio of input voltage (4 V) to the supply voltage (10 V).

TABLE 1 — Operation of delta–sigma modulation with an input signal x_i of 4 V.

i	0	1	2	3	4	5	6
x_i	4	4	4	4	4	4	4
v_i	1	–5	–1	3	–3	1	–5
b_i	10	0	0	10	0	10	0

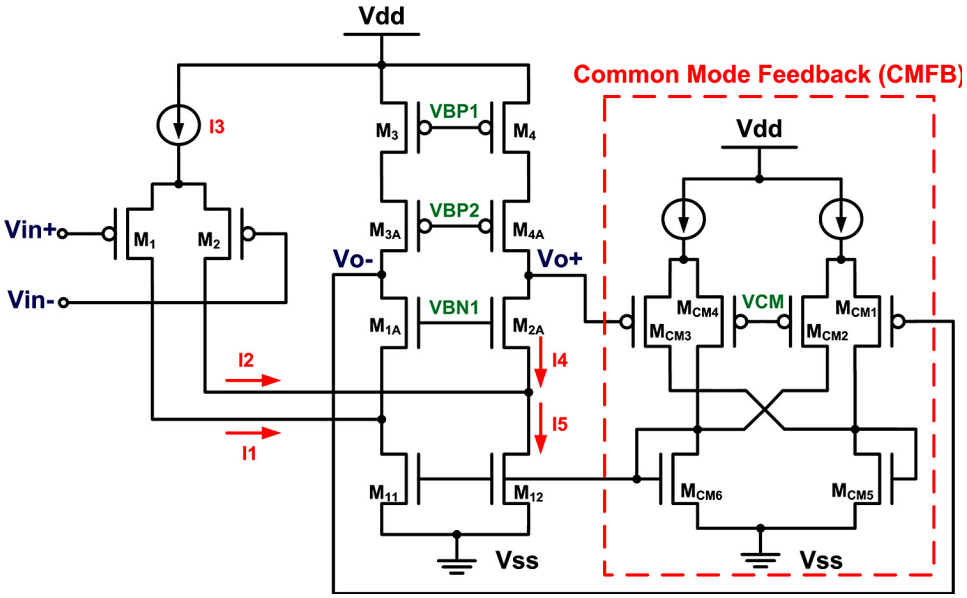

FIGURE 4 — Schematic diagram of the fully differential operational amplifier on glass substrate for 3-μm LTPS technology.

2.2 Circuit implementation and simulation results

Figure 3 shows a circuit implementation of a delta–sigma modulator using a fully differential architecture to overcome the common-mode noise with $R_{int} = R_{int1} = R_{int2} = 400\ k\Omega$, $R_{f1} = R_{f2} = 400\ k\Omega$, and $C_{int} = C_{int1} = C_{int2} = 4$ pF. The DAC function is performed by R_{f1} and R_{f2}. When positive input $Vi+$ is equal to x_i in Fig. 2, $Vi-$ is equal to $10-Vi+$, under a supply voltage (V_{dd}) of 10 V.

Because the output voltage of DFF, $b[n]$, is high ("Logic-1"), it feeds back a positive (negative) charge through R_{f2} (R_{f1}) to drive the output of the integrator $Vop-$ ($Vop+$) down (up). Therefore, $b[n]$ becomes low ("Logic-0") to form a negative feedback loop. Therefore, when the positive input voltage $Vi+$ is larger than that of $Vi-$, it will produce a high probability of "Logic-1" in the bit steam $b[n]$.

The schematic diagram of the fully differential folded-cascode operational amplifier used in this work is shown in Fig. 4. Compared with a conventional two-stage operational amplifier, this architecture exhibits a better input common-mode range, power supply rejection ratio, larger gain, and easier frequency compensation. The amplifier is simulated by an eldo simulator[18] with a supply voltage of 10 V for 3-μm LTPS technology. The simulated frequency response of the fully differential operational amplifier in the open-loop condition is shown in Fig. 5, where the VCM is given at 5 V. The DC gain and the phase margin are 61.55 dB and 79°, respectively. The simulated gain bandwidth is 4.3 MHz, and the

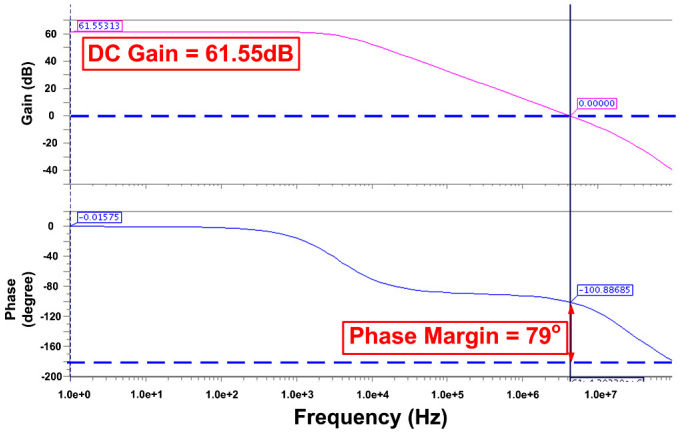

FIGURE 5 — The simulated frequency response of the fully differential operational amplifier in open-loop condition.

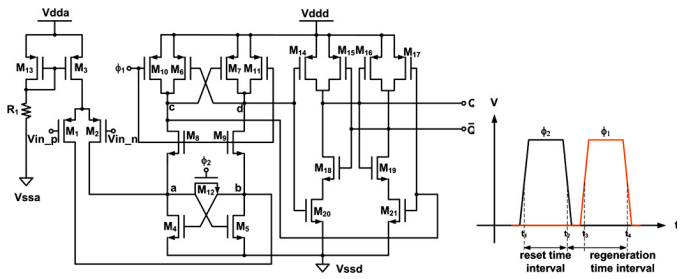

FIGURE 6 — Circuit schematic and timing diagram of the fully differential comparator on glass substrate for 3-μm LTPS technology.

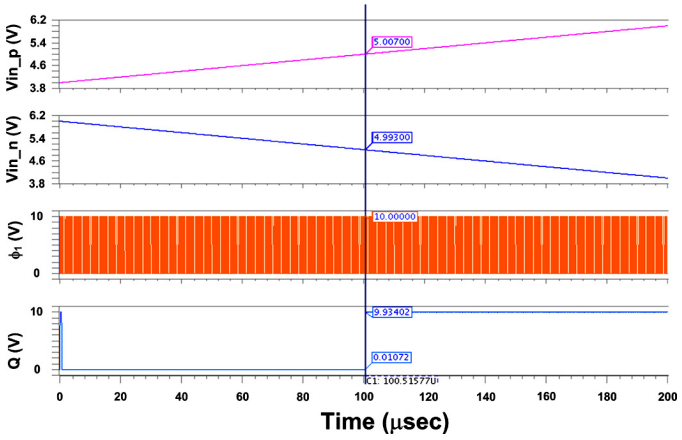

FIGURE 7 — The simulated result of the fully differential comparator.

average power dissipation is 2.3 mW. The simulated average power consumption of the entire ADC is 5.4 mW, which will depend on the fabrication technology used to implement this circuit, and the detail circuit description of the decimation filer is shown in Sec. 3.

Figure 6 shows the circuit schematic and timing diagram of the fully differential comparator realized on glass substrate for 3-μm LTPS technology. The circuit dynamic operation can be divided into two intervals: the reset time interval and the regeneration time interval, respectively. During ϕ2, the comparator is in the reset mode and transistors M_8 and M_9 isolate the p-type flip-flop from the n-type flip-flop. After the input stage settles on its decision, the output Q is forced to keep the previous state and any change in the input stage will not affect the output when the circuit is in the reset time interval. The regeneration mode initialized as M_{12} is open. The n-type flip-flop and the p-type flip-flop regenerate the voltage differences between nodes a and b, and between nodes c and d, respectively. Then, the voltage difference between nodes c and d is amplified up to the supply voltage. The following latch is driven to full complementary digital output levels at the end of the regeneration mode. The simulated result of the fully differential compa-

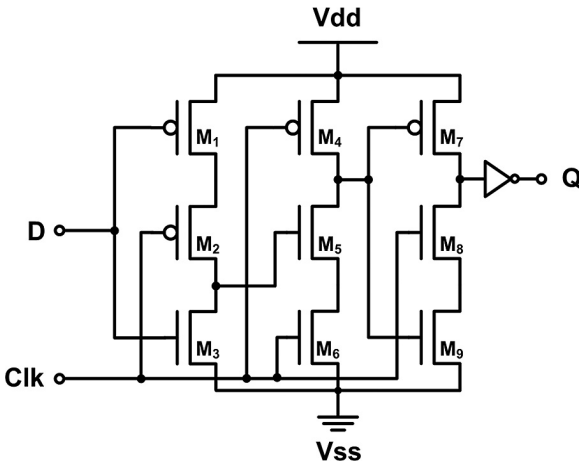

FIGURE 8 — Schematic diagram of the D flip-flop on glass substrate for 3-μm LTPS technology.

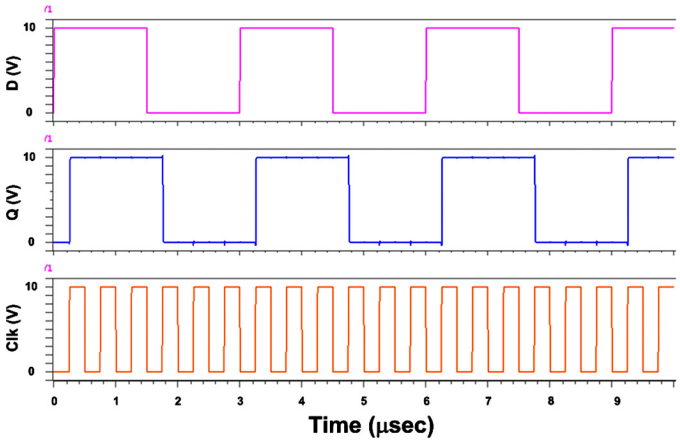

FIGURE 9 — The simulated result of the D flip-flop.

rator is shown in Fig. 7. It can successfully determined which of the two input nodes is higher with the result shown in the output.

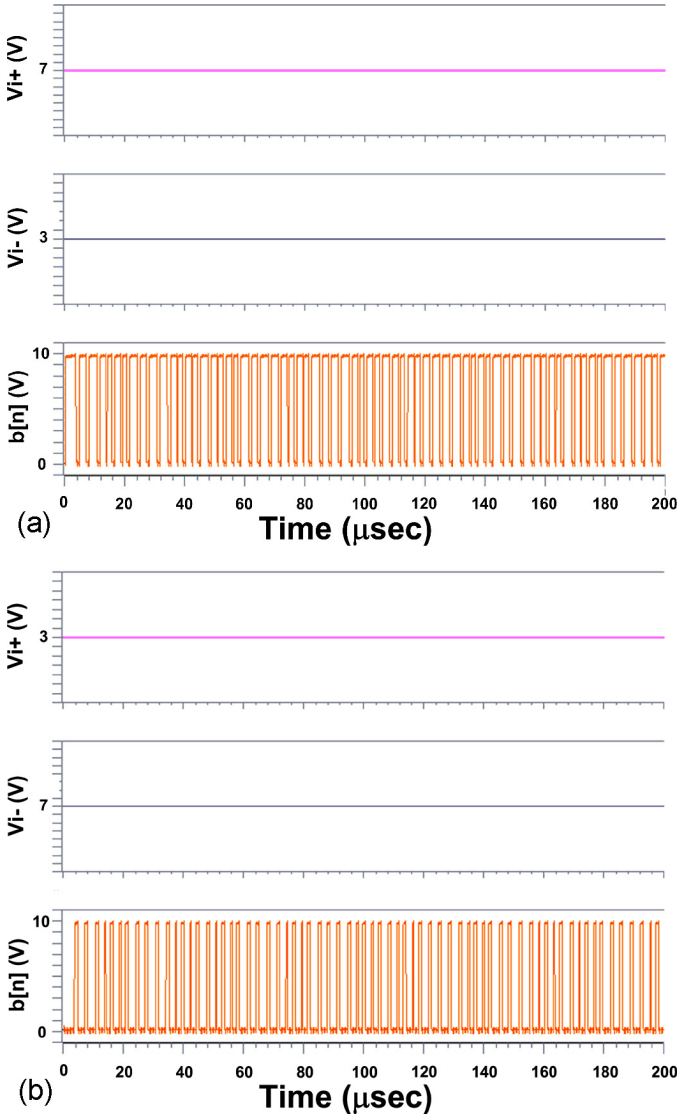

FIGURE 10 — The simulated results of the delta-sigma modulator with the input *Vi*+ of (a) 7 V and (b) 3 V for 3-μm LTPS technology.

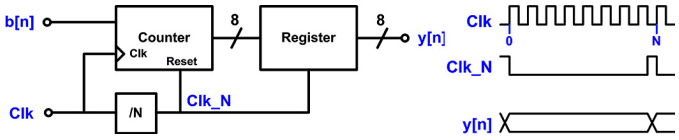

FIGURE 11 — Block diagram and timing chart of decimation filter.

The schematic diagram of the D flip-flop is shown in Fig. 8. This flip-flop requires only one clock, called a true single-phase-clock (TSPC) flip-flop.[19] The output signal Q will be high as long as the input signal D is high when the Clk signal is rising. The simulated result of the D flip-flop is shown in Fig. 9.

The delta–sigma modulator is implemented by combining the aforementioned operational amplifier, comparator, and the D flip-flop. The simulated results with different input data by the eldo simulator are shown in Figs. 10(a) and 10(b). The probability of "logic-1" in one period is also calculated. When the input signals Vi+ are 7 and 3 V, the calculated probability results are 0.703 and 0.293, respectively.

3 Design and realization of decimation filter

3.1 Theoretical operation

Figure 11 shows the block diagram of the decimation filter and its timing chart. A counter is incremented for each "Logic-1" of $b[n]$ from the modulator. The counter produces k-bit output if $N = 2^k$, which may be interpreted as a binary fraction between 0 and 1. In this work, N is chosen as 256 for an 8-bit digital output. Therefore, the output $y[n]$ of the decimation filter expressed as a function of output bit stream $b[n]$ of the delta–sigma modulator can be written as

$$y[n] = \frac{1}{N}\sum_{i=0}^{N-1} b[n-i]. \tag{4}$$

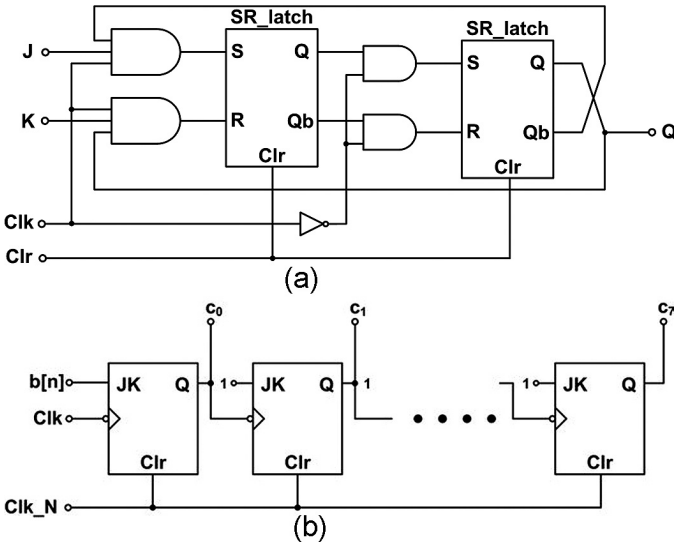

FIGURE 12 — (a) The schematic diagram of the JK flip-flop and (b) the block diagram of the counter on glass substrate for 3-μm LTPS technology.

Then, Eq. (4) can be translated into its z-domain transfer function, which is derived as

$$H_1(z) = \frac{1}{N}\frac{1-z^{-N}}{1-z^{-1}}. \quad (5)$$

The important advantage of such a decimation filter is the economical realization for a single-bit modulator.

3.2 Circuit implementation

Figure 12(a) shows the JK flip-flop and Fig. 12(b) shows the block diagram of the counter. The counter contains eight JK flip-flops whose input signals J and K are combined together. As shown in Fig. 12(b), the input of the least-significant-bit (LSB) JK flip-flop is $b[n]$, produced by the delta–sigma modulator, and it is negative edge triggered by the Clk signal. The inputs of the other 7 JK flip-flops are all "1" driven by the supply voltage. Then, the output of the counter, c0–c7, is produced.

The register is used to hold the value calculated by the counter, and the counter is designed to calculate the next 256 data in the next time frame. Figure 13 shows the block diagram of the register which consists of eight D flip-flops, and the register is positive edge triggered by the Clk_N signal produced by the divider shown in Fig. 14. The counter here is a down counter and the output $q_0 - q_7$ is counted down from 255 to 0, respectively.

The timing chart of the decimation filter is summarized and shown in Fig. 15. The operation can be divided into five steps. The first step occurs as Clk goes to "1" in one new period, then the output of the divider $q_0 - q_7$ produced by the eight D flip-flops will count down once to represent that the first data coming from the delta-sigma modulator will be processed by the counter. The second step occurs when the Clk first goes to low in one new period. At this moment, the output of the counter, which is represented as c_0 in Fig. 15, will be incremented when $b[n]$ is "1", but kept at the value of the previous state when $b[n]$ is "0". The third step occurs at the last cycle of a period. The last data will be processed in the counter and c_0 goes to "1". Then, the divider produces a pulse in the output Clk_N with some logic delay when 256 cycles are passed. The rising edge in Clk_N is the forth step and the 8-bit register is positive edge triggered to

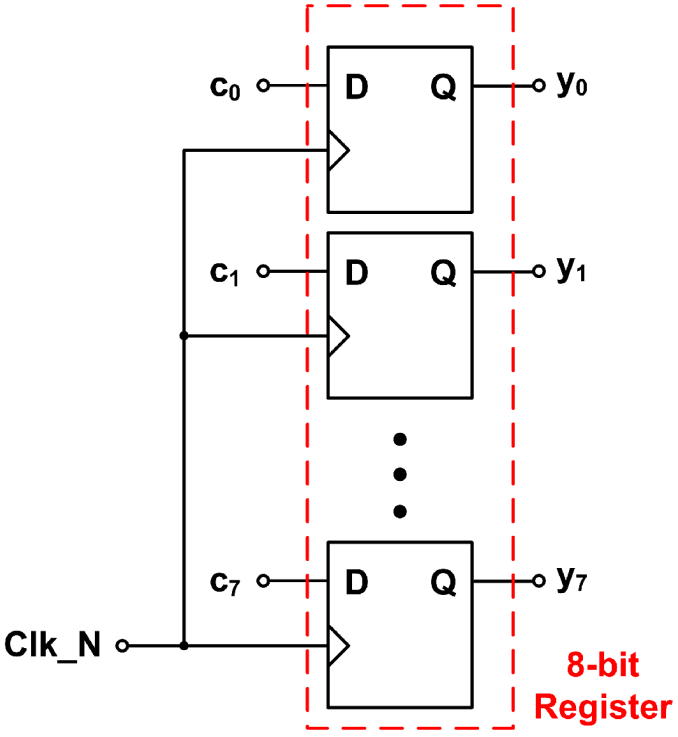

FIGURE 13 — The block diagram of the register which consists of eight D flip-flops which is positive edge triggered by the Clk signal.

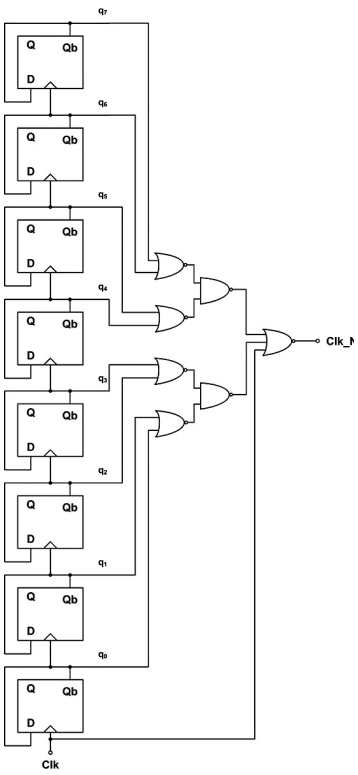

FIGURE 14 — The block diagram of the divider which consists of eight D flip-flops.

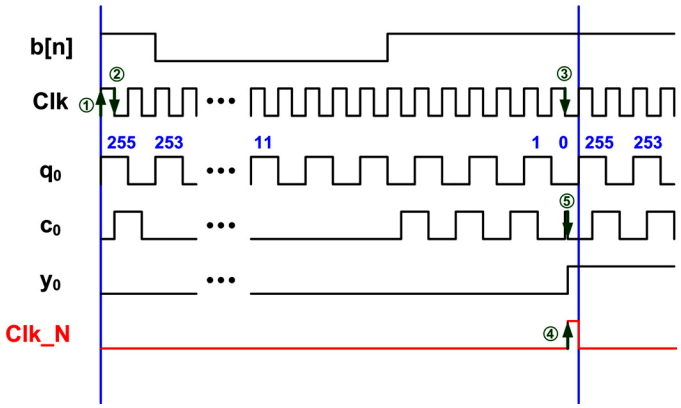

FIGURE 15 — Timing chart of the decimation filter where its operation is divided into five steps.

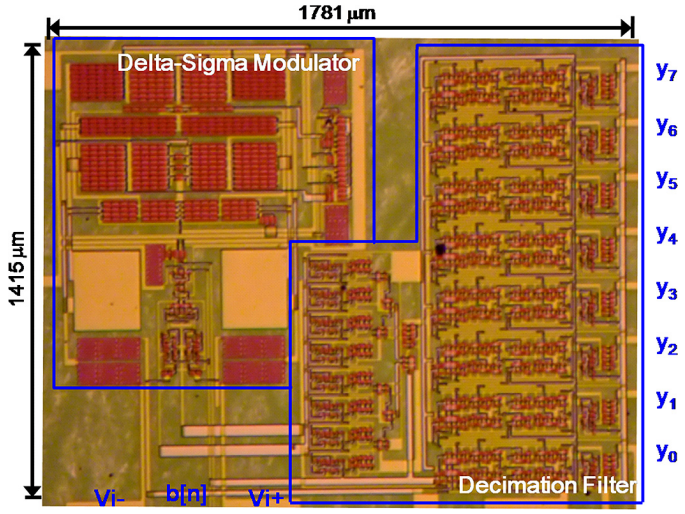

FIGURE 16 — Die photo of the fabricated delta–sigma ADC for 3-µm LTPS technology.

keep the data produced by the counter. Therefore, y_0 reflects the value of c_0 and the counter will be reset in the last step. Thus, the decimation filter processes the input data in every 256 cycles and the output represents the normalized average of $b[n]$.

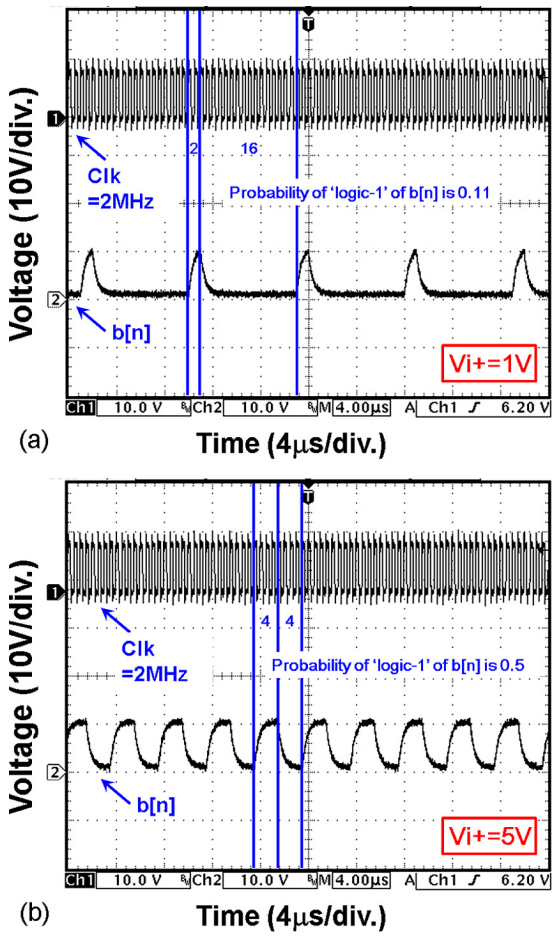

FIGURE 17 — Measured result of the delta–sigma modulator between the relation of output bit stream $b[n]$ and clock signal Clk as the input (a) $Vi+$ = 1 V and $Vi-$ = 9 V and (b) Vi+ and $Vi-$ = 5 V.

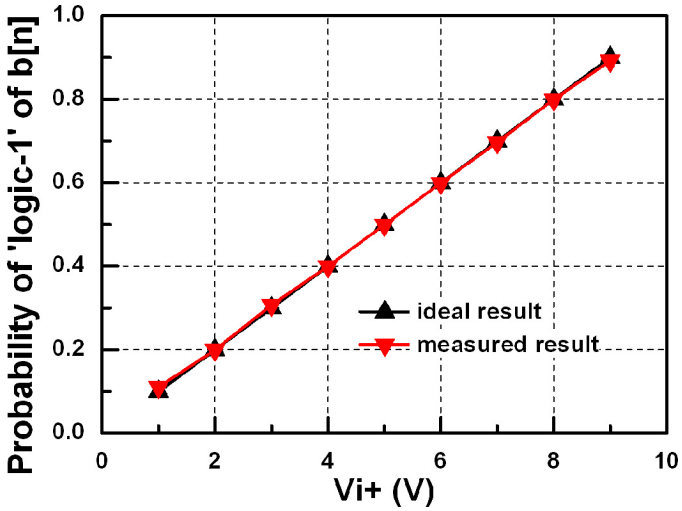

FIGURE 18 — Measured results of the fabricated delta–sigma modulator, compared with the ideal calculation.

4 Experimental results and discussion

The proposed delta–sigma ADC has been fabricated on glass substrate for 3-µm LTPS technology. The die photo of a fabricated delta–sigma ADC is shown in Fig. 16 with a test-chip size of 1415 × 1781 µm. In Fig. 16, the left-hand side is the delta-sigma modulator and the right-hand side is the decimation filter. The measured results of the delta–sigma modulator, shown in Fig. 17, represent the relationship between Clk and the output bit stream $b[n]$. In Fig. 17(a), as the input voltage $Vi+$ is equal to 1 V and $Vi-$ is equal to 9 V at a 2-MHz clock, 16 cycles of "Logic-0" accompany two cycles of "Logic-1" which can be found in the bit stream $b[n]$. With such an input signal, the probability of $b[n]$ is 0.11, which is close to the input voltage ratio (1/10). Figure 17(b) shows that input voltages $Vi+$ and $Vi-$ are both 5 V. Then, four cycles of "Logic-0" accompany four cycles of "Logic-1" which can be found in the bit stream $b[n]$, which determines the probability of $b[n]$ is 0.5 to fit the input voltage ratio (5/10). Figure 18 shows the comparison between

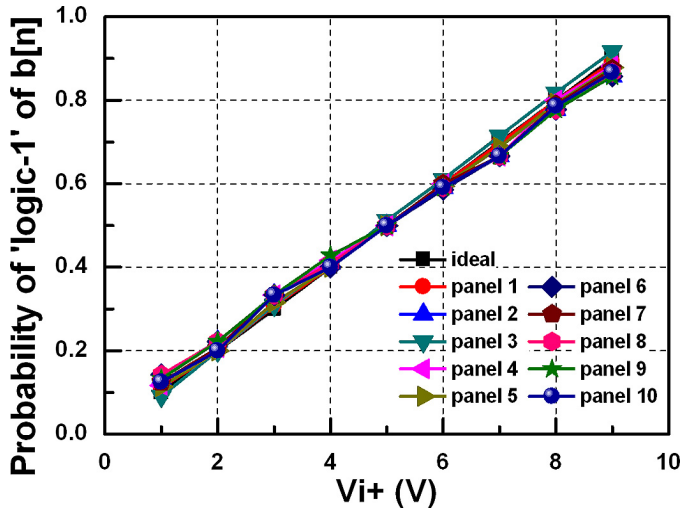

FIGURE 19 — Comparison between ideal and measurement results of a probability of "logic-1" in the bit stream $b[n]$ among 10 different panels.

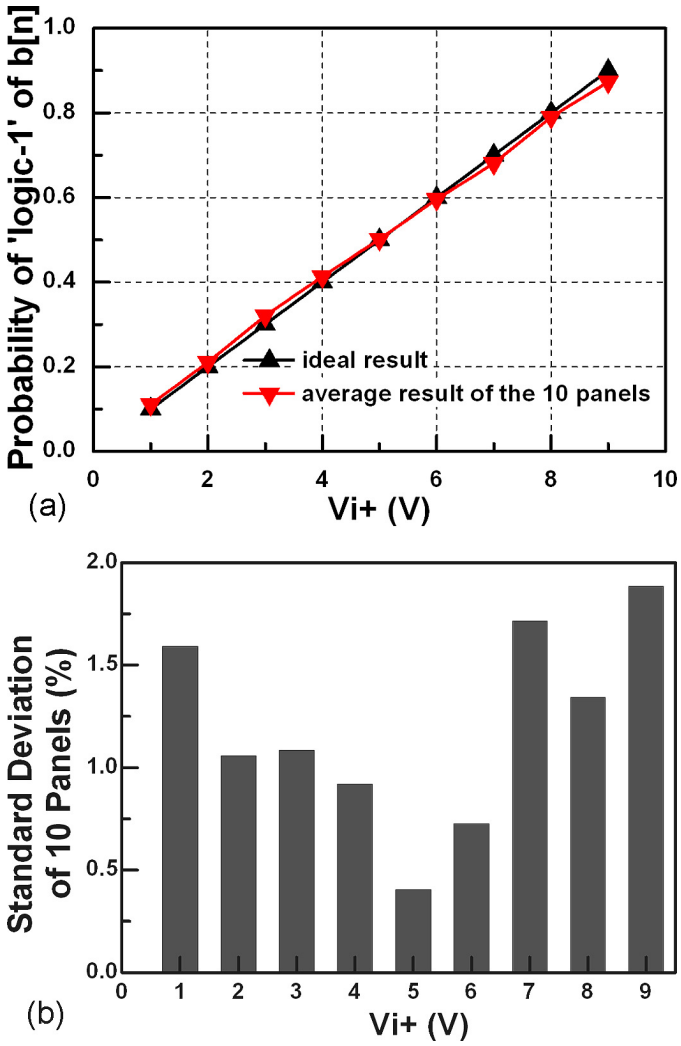

FIGURE 20 — Measured results of (a) the averaged and (b) standard deviation probability of "Logic 1" of $b[n]$ among 10 different panels.

the ideal and the measured results of a probability of "logic-1" in the bit stream $b[n]$. Good agreement between the ideal calculation and the measured results can be obtained from the fabricated delta–sigma modulator.

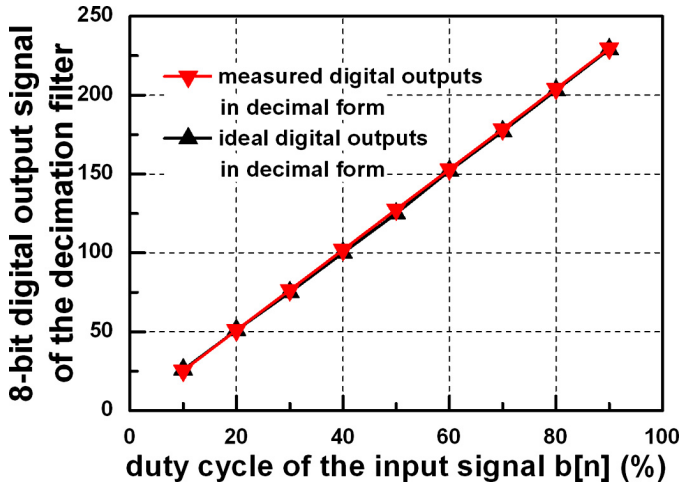

FIGURE 21 — Measured results of the decimation filter with its input signal produced by the pulse generator.

Figure 19 shows the measured results of 10 panels. According to Fig. 19, Fig. 20(a) shows the average result of the 10 panels and Fig. 20(b) shows the standard deviation among 10 different panels with different input voltages. The minimum standard deviation occurs at $Vi+ = 5$ V and the maximum of that which is less than 2% occurs as $Vi+ = 9$ V. Summing up the above-measured results, the delta–sigma modulator is successfully implemented and verified on glass substrate for 3-μm LTPS technology.

Figure 21 shows the measured results of the decimation filter with its input provided by changing the duty cycle in the waveform of the pulse generator. Because such a decimation filter will sum up the number of "logic-1" in every 256 cycles, changing the duty cycle of the input pulse also changes the probability of "logic-1" counted by the decimation filter. The measured results are compared with the ideal one in decimal form. Good agreement between the ideal and measured results can be obtained from the fabricated decimation filter.

The measured results of the whole delta–sigma ADC are shown in Fig. 22 for one measured typical panel. The probability of "logic-1" in $b[n]$ is obtained in the same manner mentioned in Fig. 17. The normalized output of the ADC is found by dividing the 8-bit digital output signal of the decimation filter by a factor of 256 and then calculate its corresponding probability of "logic-1" in $b[n]$. However, the output of the whole delta–sigma ADC shows a small variation in the unchanged input because the period of the bit stream $b[n]$ is not always a factor of 256 (the 256 is the conversion cycle number of the decimation filter). For example, the period of $b[n]$ is 18 cycles with two numbers of "logic-1" and 16 numbers of "logic-0" as shown in Fig. 17(a). When the number 256 is divided by 18, the remainder is 4. Thus, that will cause a 4-cycle error. Therefore, the measured results of the decimation filter in every 256 cycles deliver some errors when the input signal is unchanged. For that reason, Fig. 22 also shows the minimum and maximum nor-

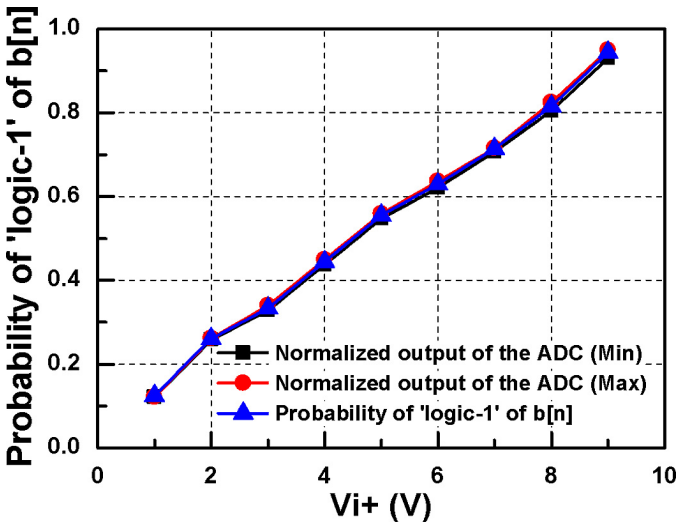

FIGURE 22 — Measured results of the ADC where its digital output is normalized to compare with the probability of $b[n]$.

malized output of the ADC with an unchanged input signal, and the probability of "logic-1" in $b[n]$ is located between the other two lines.

The flicker noise is most significant at low frequency, and it theoretically may incur a function error of ADC with DC-like input. However, the power of DC-like input signals in this ADC is much larger than that of the flicker noise, so the flicker noise did not show an obvious influence on the performance of this ADC in the experimental results.

Finally, since the carrier mobility depends on the grain size of the active poly-Si layer, the deviation of the TFT characteristic is dependent on the quality of the poly-Si layer. The device showed much larger variation for LTPS technology than that for CMOS technology.[20] In Ref. 21, some well-known architectures of ADC, such as flash, pipeline, successive approximation (SAR), and delta-sigma, have different requirements to obtain higher performance. For flash and SAR ADCs, the accuracy is highly dependent on the offset of the comparator. For a pipeline ADC, the gain of OP is usually required to be higher for accuracy. Since the LTPS process exhibits larger variation and worse device characteristics (such as mobility), it is difficult to reduce the offset of the comparator utilized in flash and SAR ADCs and to achieve a high gain for the OP used in a pipeline ADC. In this work, the delta–sigma ADC selected due to its accuracy, does not highly depend on component matching, precise sample-and-hold, or trimming, and only a small amount of analog circuitry is required. Larger variation and worse device characteristics for the LTPS process can therefore have a much smaller influence on the delta–sigma ADC. In addition, the proposed delta–sigma ADC is designed for the application of a temperature-to-digital converter on glass substrate in combination with an on-panel bandgap reference circuit.[9] Since the input signal of a delta–sigma ADC is mostly a dc-like value, only a sinc filter is implemented after the delta–sigma modulator to simplify the circuit complexity.

5 Conclusion

By reality consideration and comparisons of the open literatures, a delta–sigma ADC on glass substrate for panel integration has been successfully designed and fabricated for 3-μm LTPS technology. The input signal of delta–sigma ADC can be reconstructed by calculating the running probability of $b[n]$. By the application of a temperature-to-digital converter on glass substrate, only a sinc filter is implemented after the delta–sigma modulator to simplify the circuit complexity. Good agreement between ideal and measured results has been obtained from the fabricated delta–sigma ADC. The proposed delta–sigma ADC, the first implemented on glass substrate, enables the analog circuits to be integrated in AMLCD panels for SOP applications.

Acknowledgment

This work was supported by AU Optronics Corp., and partially supported by the "Aim for the Top University Plan" of National Chiao Tung University and Ministry of Education Taiwan, R.O.C. This work was also supported in part by the National Science Council (NSC), Taiwan, and under contract NSC 98-2221-E-009-113-MY2.

References

1 F. Gan and I. Shih, "Preparation of thin-film transistors with chemical bath deposited CdSe and CdS thin films," *IEEE Trans. Electron. Dev.* **49**, No. 1, 15–18 (Jan. 2002).
2 J.-C. Liao *et al.,* "Dynamic negative bias temperature instability (NBTI) of low-temperature polycrystalline silicon (LTPS) thin-film transistors," *IEEE Electron. Dev. Lett.* **29**, No. 5, 477–479 (May 2008).
3 H.-J. Chung and Y.-W. Sin, "Low power level shifter for system-on-panel applications," *SID Symposium Digest* **39**, 1231–1234 (2008).
4 S.-H. Yeh *et al.,* "A 2.2-in. QVGA system-on-glass LCD using P-type low temperature poly-silicon thin film transistors," *SID Symposium Digest* **36**, 352–355 (2005).
5 M. Murase *et al.,* "A 2.2-inch narrow frame liquid crystal system display with low voltage interface circuitry," *SID Symposium Digest* **37**, 1654–1657 (2006).
6 Y.-S. Park *et al.,* "An 8b source driver for 2.0 inch full-color active-matrix OLEDs made with LTPS TFTs," in *IEEE Intl. Solid-State Circuits Conf. Dig. Tech. Papers,* 130–132 (2007).
7 B. Lee *et al.,* "A CPU on a glass substrate using CG-silicon TFTs," *IEEE Intl. Solid-State Circuits Conf. Dig. Tech. Papers,* 164–165 (Feb. 2003).
8 J. Lee *et al.,* "Hybrid touch screen panel integrated in TFT-LCD," *SID Symposium Digest* **38**, 1101–1104 (2007).
9 T.-C. Lu *et al.,* "Temperature coefficient of poly-silicon TFT and its application on voltage reference circuit with temperature compensation in LTPS process," *IEEE Trans. Electron. Dev.* **55**, No. 10, 2583–2589 (Oct. 2008).
10 J.-H. Yu *et al.,* "4 inch a-Si TFT-LCD with an embedded color image scanner," *SID Symposium Digest* **38**, 196–198 (2007).
11 K.-C. Lee *et al.,* "A thermally adaptive response time compensation system for LCD panels," *SID Symposium Digest* **38**, 484–487 (2007).
12 M. Pertijs *et al.,* "A CMOS smart temperature sensor with a 3σ inaccuracy of 0.1°C from –55°C to 125°C," *IEEE J. Solid-State Circuits* **40**, No. 12, 2805–2815 (Dec. 2005).
13 M. Keramat, "Functionality of quantization noise in sigma-delta modulators," *IEEE Midwest Symp. Circuits and Systems,* 912–915 (2000).
14 N. Amin *et al.,* "An efficient first order sigma delta modulator design," *IEEE J. Solid-State Circuits* **23**, No. 6, 1298–1308 (Aug. 2002).
15 L. Cao and Z. Yang, "The error analysis of sigma delta modulator," *IEEE Intl. Symp. Commun. Info. Technol.,* 255–258 (2005).
16 C.-C. Tsai *et al.,* "Design and realization of delta-sigma analog-to-digital converter in LTPS technology," *SID Symposium Digest* **40**, 1283–1286 (2009).
17 R. Schreier and G. C. Temes, *Understanding Delta-Sigma Data Converters* (John Wiley & Sons, Inc., 2005).
18 Mentor Graphics, *Eldo simulation*, Mentor Graphics Corporation (2007).
19 N. H. E. Weste and D. Harris, *CMOS VLSI Design: A Circuits and Systems Perspective* (Addison Wesley, Inc., 2005).
20 Y.-H. Tai *et al.,* "A statistical model for simulating the effect of LTPS TFT device variation for SOP applications," *IEEE J. Display Technol.* **3**, No. 4, 426–433 (Dec. 2007).
21 R. J. Baker, *CMOS: Circuit Design, Layout, and Simulation* (John Wiley & Sons, Inc., 2008).

Chia-Chi Tsai received her M.S. degree from the Department of Electronics Engineering, National Chiao-Tung University, Hsinchu, Taiwan, R.O.C., in 2009. In 2009, she joined the Realtek Semiconductor Corporation. Her main research interest is the design of analog circuits.

Tzu-Ming Wang received his B.S. degree from the Department of Electronics Engineering, National Chiao-Tung University, Hsinchu, Taiwan, R.O.C., in 2005. He is currently working toward his Ph.D. degree at the Institute of Electronics, National Chiao-Tung University. His current research interests include analog circuit design on glass substrate and mixed-voltage I/O circuit design in low-voltage CMOS technology.

Ming-Dou Ker received his Ph.D. degree from the Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan, in 1993. During 1994–1999, he worked in the VLSI Design Division, Computer and Communication Research Laboratories, Industrial Technology Research Institute (ITRI), Hsinchu, Taiwan. Since 2004, he has been a Full Professor in the Department of Electronics Engineering and Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan. From 2008, he was rotated to be Chair Professor and Vice-President of I-Shou University, Kaoshiung, Taiwan. In 2010, he has been a Distinguished Professor in the Department of Electronics Engineering, National Chiao-Tung University, and he also served as the Executive Director of the National Science and Technology Program on System-on-Chip (NSoC) in Taiwan. In the field of reliability and quality design for circuits and systems in CMOS technology, he has published over 400 technical papers in international journals and conferences. He has proposed many inventions to improve the reliability and quality of integrated circuits, which have been granted with 166 U.S. patents and 148 R.O.C. (Taiwan) patents. His current research interests include reliability and quality design for nanoelectronics and gigascale systems, high-speed and mixed-voltage I/O interface circuits, on-glass circuits for system-on-panel applications, and biomimetic circuits and systems for intelligent prosthesis. Prof. Ker had been invited to teach or to consult reliability and quality design for integrated circuits by hundreds of design houses and semiconductor companies in the worldwide IC Industry. Prof. Ker has served as the member of Technical Program Committees and the Session Chair of numerous international conferences. He served as the Associate Editor for the *IEEE Transactions on VLSI Systems*. He has been selected as the *Distinguished Lecturer* by the IEEE Circuits and Systems Society (2006–2007) and by the IEEE Electron Devices Society (2008–2010). He was the President of Foundation in Taiwan ESD Association. In 2009, he was selected as one of the top-ten *Distinguished Inventors* in Taiwan; and one of the top-hundred *Distinguished Inventors* in China. In 2008, Prof. Ker was elevated as an IEEE Fellow with the citation of *"for contributions to electrostatic protection in integrated circuits, and performance optimization of VLSI micro-systems."*