High-Voltage-Tolerant ESD Clamp Circuit With Low Standby Leakage in Nanoscale CMOS Process

Ming-Dou Ker, *Fellow, IEEE*, and Chun-Yu Lin, *Member, IEEE*

***Abstract*—For system-on-chip applications with mixed-voltage I/O interfaces, I/O circuits with low-voltage devices must drive or receive high-voltage signals to communicate with other circuit blocks. With the consideration of low standby leakage in nanoscale CMOS processes, a new $2 \times V_{\rm DD}$-tolerant electrostatic discharge (ESD) clamp circuit by using only $1 \times V_{\rm DD}$ devices was presented in this paper. The new ESD clamp circuit had a high-voltage-tolerant ESD detection circuit to improve the turn-on efficiency of an ESD clamp device, which consisted of a silicon-controlled rectifier (SCR) with a diode in series. This design had successfully been verified in a 65-nm CMOS process. The leakage current of this ESD clamp circuit under normal circuit operating condition was only on the order of 100 nA. The test patterns with 25- and 50-μm SCR-based ESD clamp devices can achieve 2.6- and 4.8-kV human-body-model ESD robustness, respectively. Such high-voltage-tolerant ESD clamp circuits, by using only low-voltage devices with very low standby leakage current and high ESD robustness, were very suitable for mixed-voltage I/O interfaces in nanoscale CMOS processes.**

***Index Terms*—Electrostatic discharge (ESD), low-voltage CMOS, mixed-voltage I/O, power-rail ESD clamp circuit, silicon-controlled rectifier (SCR).**

I. Introduction

In ADVANCED CMOS technologies, the thickness of gate oxide has been scaled down to improve circuit performances with the decreased power supply voltage for low-power applications. However, for system-on-chip (SoC) applications, I/O buffers with low-voltage devices will drive or receive high-voltage signals to communicate with other integrated circuits in the microelectronic systems or subsystems. Therefore, the I/O buffers must be designed with consideration of high-voltage tolerance to prevent overstress voltage on the thinner gate oxide of the devices in I/O buffers. To avoid this gate-oxide reliability issue without using additional thick gate-oxide devices, the stacked NMOS configuration has widely been used in the mixed-voltage I/O buffers [1]–[3]. Without the thick gate-oxide devices in low-voltage processes, the process steps can be reduced, the fabrication yield can be increased, and the chip cost can be lowered. However, the stacked NMOS configuration usually has lower electrostatic discharge (ESD) robustness and slow turn-on speed of the parasitic lateral n-p-n bipolar junction transistor (BJT), compared to the single NMOS [4]–[6]. Therefore, additional ESD protection design must be provided to protect the stacked NMOS in the mixed-voltage I/O buffer.

The ESD protection scheme with ESD bus and high-voltage-tolerant ESD clamp circuit for a SoC with mixed-voltage I/O interfaces has been presented [7], [8]. The high-voltage-tolerant ESD clamp circuits realized with only $1 \times V_{\rm DD}$ devices have been reported [9]–[12]. However, in nanoscale CMOS technologies, the leakage current must be considered during the circuit design [13]–[15]. Therefore, the high-voltage-tolerant power-rail ESD clamp circuit must be designed with consideration of low standby leakage current in nanoscale CMOS processes.

II. ESD Protection Scheme With on-Chip ESD Bus for High-Voltage-Tolerant Mixed-Voltage I/O Buffer

To receive the input signals with $n \times V_{\rm DD}$ voltage level, the traditional ESD protection design with direct diode connection from the I/O pad to the $1 \times V_{\rm DD}$ line is forbidden. To improve the ESD robustness of the mixed-voltage I/O interfaces, the ESD protection circuit with on-chip ESD bus is used. The ESD protection scheme with ESD bus and high-voltage-tolerant ESD clamp circuit for a SoC with mixed-voltage I/O interfaces has been presented [7], [8]. With consideration of gate-oxide reliability, the ESD protection scheme with on-chip ESD bus for high-voltage-tolerant mixed-voltage I/O buffer is shown in Fig. 1. The ESD protection scheme is realized with ESD diodes (D_P, D_N, and D_1), ESD bus, $1 \times V_{\rm DD}$ ESD clamp circuit, and high-voltage-tolerant ESD clamp circuit.

While positive ESD charges stress to the I/O pad with grounded ESD bus, the ESD currents can be discharged through diode D_P in forward-biased condition. As positive ESD charges stress to the I/O pad with grounded $V_{\rm SS}$, the ESD currents can be discharged through diode D_P to the ESD bus and then through the high-voltage-tolerant ESD clamp circuit to $V_{\rm SS}$. Once positive ESD charges stress to the I/O pad with grounded $V_{\rm DD}$, the ESD currents can be discharged through D_P, ESD bus, high-voltage-tolerant ESD clamp circuit, $V_{\rm SS}$ line, and $1 \times V_{\rm DD}$ ESD clamp circuit.

Manuscript received September 29, 2009; revised April 13, 2010; accepted April 13, 2010. Date of publication May 20, 2010; date of current version June 23, 2010. This work was supported in part by the National Science Council, Taiwan, under Contract NSC 98-2221-E-009-113-MY2, by the Ministry of Economic Affairs, Taiwan, under Grant 98-EC-17-A-01-S1-104, by the "Aim for the Top University Plan" of National Chiao-Tung University and Ministry of Education, Taiwan, and by Faraday Technology Corporation, Taiwan. The review of this paper was arranged by Editor R. Huang.

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Digital Object Identifier 10.1109/TED.2010.2049072

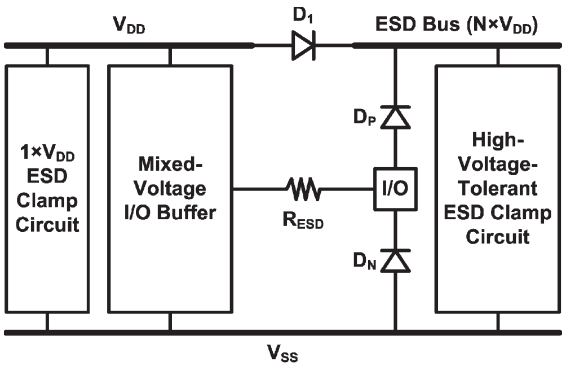

Fig. 1. ESD protection scheme with on-chip ESD bus for high-voltage-tolerant mixed-voltage I/O buffer.

While negative ESD charges stress to the I/O pad with grounded $V_{\rm SS}$, the ESD currents can be discharged through the diode D_N in forward-biased condition. As negative ESD charges stress to the I/O pad with grounded ESD bus, the ESD currents can be discharged through D_N to the floating $V_{\rm SS}$ line and then through the high-voltage-tolerant ESD clamp circuit to the ESD bus. Once negative ESD charges stress to the I/O pad with grounded $V_{\rm DD}$, the ESD currents can be discharged through D_N to the floating $V_{\rm SS}$ line and then through the $1 \times V_{\rm DD}$ ESD clamp circuit to $V_{\rm DD}$. Each mode of ESD stresses has the corresponding well-designed ESD discharging path in this ESD protection scheme.

III. New Design of High-Voltage-Tolerant ESD Clamp Circuit

In nanoscale CMOS technologies, a new design of high-voltage-tolerant ESD clamp circuit is proposed to reduce standby leakage current. The details of the proposed design will be discussed in this section.

A. Circuit Topology

The new ESD clamp circuit has an $n \times V_{\rm DD}$-tolerant ESD detection circuit to improve the turn-on efficiency of the $n \times V_{\rm DD}$-tolerant ESD clamp device, as shown in Fig. 2. The $n \times V_{\rm DD}$-tolerant ESD detection circuit is composed of n low-leakage ESD detection circuits to divide $n \times V_{\rm DD}$ voltage into $1 \times V_{\rm DD}$ voltage by their self. Even if there is process variation, each low-leakage ESD detection circuit is expected to have almost the same variation due to the symmetry between these low-leakage ESD diction circuits. Thus, each low-leakage ESD diction circuit still sustains $\sim 1 \times V_{\rm DD}$ voltage. In other words, this design prevents from gate-oxide overstress issue as all low-voltage devices sustain only $1 \times V_{\rm DD}$ voltage. In addition, the initial-on p-channel MOS (PMOS) devices (Mt1, . . ., Mtn) [16] exist in each low-leakage ESD detection circuits to effectively trigger the ESD clamp device under ESD stress conditions. The main ESD current discharging path is an $n \times V_{\rm DD}$-tolerant ESD clamp device, which consists of the silicon-controlled rectifier (SCR) with diodes in series. The SCR device, which is composed of cross-coupled p-n-p and n-p-n BJTs with regenerative feedback loop, can sustain high ESD level within a small silicon area in the CMOS process. To improve the turn-on speed of

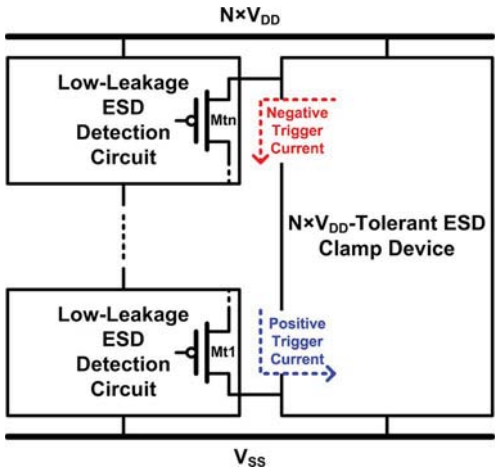

Fig. 2. New ESD clamp circuit with $n \times V_{\rm DD}$-tolerant ESD detection circuit to trigger $n \times V_{\rm DD}$-tolerant ESD clamp device.

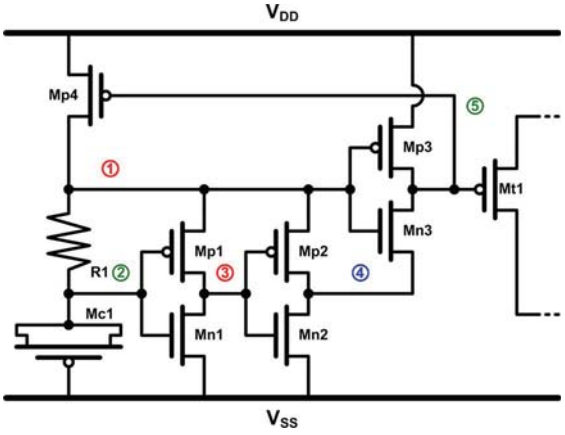

Fig. 3. Implementation of $1 \times V_{\rm DD}$-tolerant ESD detection circuit.

SCR device under ESD stress conditions, the trigger currents can be absorbed from the base terminal of p-n-p BJT and be injected to the base terminal of n-p-n BJT in SCR device. In addition, the ESD clamp device of SCR with diodes in series has been verified to have low leakage current, high ESD robustness, and good latchup immunity [18]. Moreover, the SCR device without polygate layer has good immunity against the gate-oxide overstress problem.

B. $1 \times V_{\rm DD}$-Tolerant ESD Detection Circuit

Fig. 3 shows a $1 \times V_{\rm DD}$-tolerant ESD detection circuit of the $n \times V_{\rm DD}$-tolerant ESD detection circuit. The $1 \times V_{\rm DD}$-tolerant ESD detection circuit consists of the RC timer, inverters, feedback PMOS Mp4, and trigger PMOS Mt1. The RC timer is typically used to enable the clamp during fast-edge ESD event and to isolate it from the power supply during normal power-on condition. Under normal circuit operating condition, the voltage of node 5 is biased at logic high, and no trigger current is generated in the trigger PMOS Mt1. In the mean time, the feedback PMOS Mp4 can lower the voltage drop across the RC timer, because the voltage of node 1 can be decreased as the voltage of node 5 is biased at logic high. Therefore, the voltage drop and gate-leakage current of the MOS capacitor under the normal circuit operating condition can be reduced. Fig. 4 shows

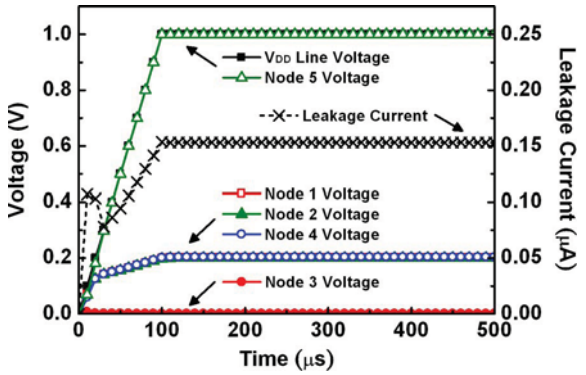

Fig. 4. HSPICE-simulated results of $1 \times V_{\rm DD}$-tolerant ESD detection circuit under normal power-on condition.

the HSPICE-simulated results of the $1 \times V_{\rm DD}$-tolerant ESD detection circuit under normal circuit operating conditions. The node-2 voltage is only ~0.2 V. In other words, the voltage across the MOS capacitor is only $\sim 0.2 \times V_{\rm DD}$, which is much lower than that in the traditional RC-based ESD detection circuits. Therefore, the gate-leakage current through the MOS capacitor can be significantly reduced, and the total leakage current can be reduced to ~ 0.15 μA at room temperature.

When a positive fast-transient ESD voltage is applied to the $V_{\rm DD}$ line with $V_{\rm SS}$ grounded, the trigger currents will pass through the initial-on PMOS Mt1 to trigger the ESD clamp device. In the mean time, the voltage of node 5 is still floating, so the voltage of node 1 can be charged through the PMOS Mp4 to logic high to turn on the NMOS Mn3. The RC delay keeps the voltage of node 2 at logic low, the voltage of node 3 at logic high, and the voltage of node 4 at logic low. Therefore, the voltage of node 5 can be kept at logic low through the turned-on NMOS Mn3, and the trigger PMOS Mt1 can continuously generate the trigger currents. Finally, the ESD clamp device can be fully turned on into the holding state to discharge ESD currents from $V_{\rm DD}$ to $V_{\rm SS}$.

C. High-Voltage-Tolerant ESD Clamp Circuit

Fig. 5 shows the test circuit of the $2 \times V_{\rm DD}$-tolerant ESD clamp circuit. The main ESD current discharging path consists of the double-triggered SCR (DTSCR) with a diode in series (DTSCR + diode). The DTSCR + diode structure has high-enough holding voltage to prevent from the latchup issue. In addition, the SCR device and the forward-biased diode can sustain a high ESD level within a small silicon area in CMOS process. Under HSPICE simulations, the SCR compact model can be introduced for the DTSCR device [19], [20]. Since the simulations dealt with the conditions before the SCR turned on, the SCR can be regarded as an open circuit between its anode and cathode. Only the parasitic well resistances between the negative (positive) trigger port of DTSCR and $V_{\rm DD}$ ($V_{\rm SS}$), which are labeled as Rn (Rp) in Fig. 5, need to be considered. To simplify the simulation in this study, the ESD clamp device in Fig. 5 is represented by resistances Rn and Rp. These resistances are estimated from the design kit of the given process to be 100 Ω. Fig. 6(a) shows the HSPICE-simulated results of the $2 \times V_{\rm DD}$-tolerant ESD clamp circuit under normal circuit

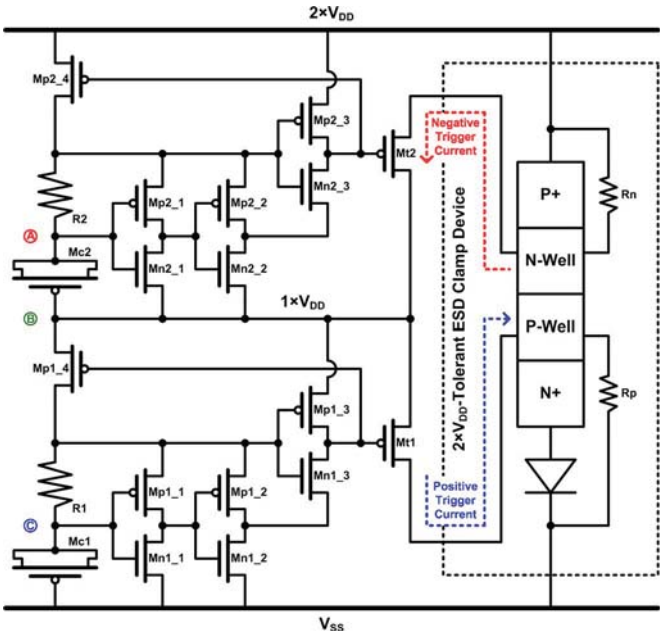

Fig. 5. Implementation of $2 \times V_{\rm DD}$-tolerant ESD clamp circuit with $2 \times V_{\rm DD}$-tolerant ESD detection circuit and SCR-based ESD clamp device.

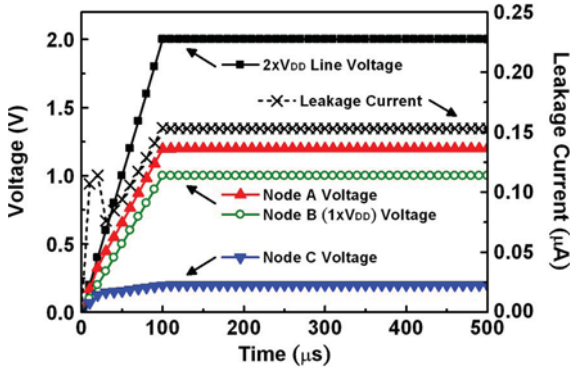

Fig. 6. HSPICE-simulated results of $2 \times V_{\rm DD}$-tolerant ESD clamp circuit under normal power-on condition (a) at 25 °C and (b) within 25 °C and 100 °C.

operating conditions. With 2-V $2 \times V_{\rm DD}$ and grounded $V_{\rm SS}$, node B ($1 \times V_{\rm DD}$) of the circuit in Fig. 5 is 1 V. In other words, all low-voltage devices sustain only 1 V. Therefore, all low-voltage devices prevent from the gate-oxide overstress issue.

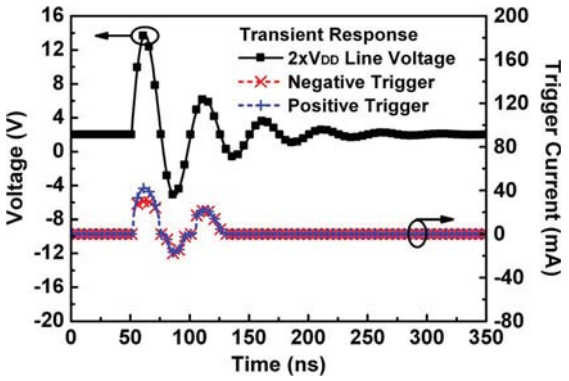

Fig. 7. HSPICE-simulated transient responses of $2 \times V_{\rm DD}$-tolerant ESD clamp circuit.

The total leakage current is only ~ 0.15 μA at 25 °C. As the temperature varies from 25 °C to 100 °C, Fig. 6(b) summarizes the simulated results under normal circuit operating conditions. The node B $(1 \times V_{\rm DD})$ voltage is exactly at 1 V, even if the temperature varies from 25 °C to 100 °C.

Fig. 7 shows the simulated transient responses of the $2 \times V_{\rm DD}$-tolerant ESD clamp circuit. With the voltage disturbance on $2 \times V_{\rm DD}$ line, the ESD detection circuit is accidentally turned on under normal circuit operating condition. However, the MOS capacitors can be restored to logic high to turn off the trigger currents.

When a positive fast-transient ESD voltage is applied to $2 \times V_{\rm DD}$ line with $V_{\rm SS}$ grounded, the trigger currents will pass through the initial-on PMOS (Mt1 and Mt2) to trigger the DTSCR device. The RC delay keeps the trigger PMOS (Mt1 and Mt2) turned on to continuously generate the trigger currents. Finally, the DTSCR device can be fully turned on into holding state to discharge ESD currents from the $2 \times V_{\rm DD}$ line to $V_{\rm SS}$. Fig. 8(a) shows the simulation results of the ESD detection circuit under 5-V ESD-like pulse stress to simulate the fast transient voltage of human-body-model (HBM) ESD events, and Fig. 8(b) summarizes that under different voltage pulse stresses. The trigger currents can be successfully generated.

The $2 \times V_{\rm DD}$-tolerant ESD clamp devices with and without the ESD detection circuit have been fabricated in a 1-V 65-nm CMOS process. The size of ESD clamp devices is designed to pass the general requirement of 2-kV (4-kV) HBM ESD level, so the sizes of the DTSCR and diode are all selected to be 25 μm (50 μm). In addition, Mt1 and Mt2 of the ESD detection circuit are also selected to be 25 μm (50 μm). The layout area of the test circuits is summarized in Table I.

D. Experimental Results

The I–V characteristics of the circuits are measured by using a transmission line pulsing (TLP) system with 10-ns rise time and 100-ns pulsewidth. Fig. 9 shows the TLP-measured I–V curves of the ESD clamp circuits. The trigger voltages V_{t1} of each stand-alone ESD clamp devices without the ESD detection circuit are 11.8 V. The trigger voltage of the ESD clamp circuit with 25-μm trigger PMOS and 25-μm (50-μm) DTSCR is reduced to 6.7 V (7.3 V), while that with 50-μm

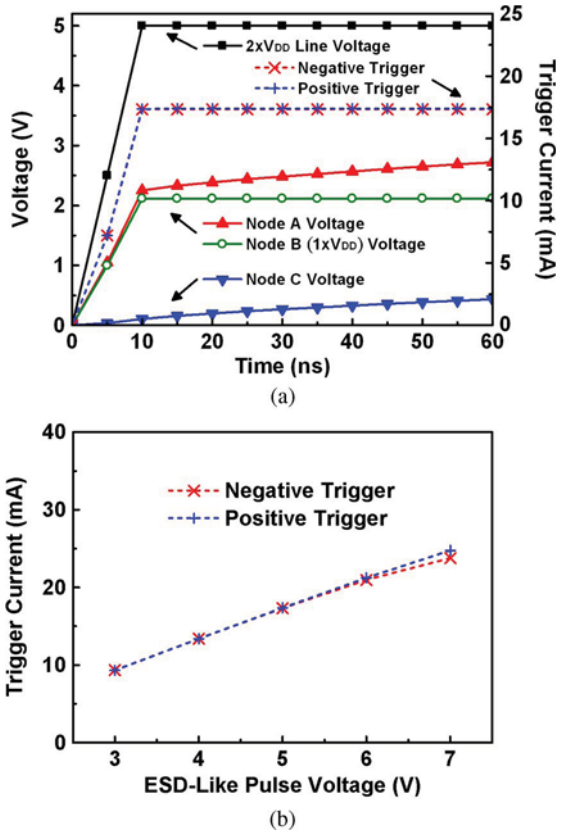

Fig. 8. HSPICE-simulated results of $2 \times V_{\rm DD}$-tolerant ESD detection circuit under ESD-like pulse stress. (a) 5-V pulse. (b) Summary of different voltage pulses.

trigger PMOS and 25-μm (50-μm) DTSCR is reduced to 6 V (6.5 V). The secondary breakdown currents I_{t2} of ESD clamp circuits with 25- and 50-μm DTSCR are kept at $\sim$1.6 and $\sim$2.9 A, respectively. These data are summarized in Table I.

The HBM ESD robustness of the fabricated ESD clamp circuits are evaluated by the ESD simulator. All ESD clamp devices with 25-μm (50-μm) size can achieve 2.6-kV (4.8-kV) HBM ESD robustness. These data are also summarized in Table I.

The dc I–V characteristics of ESD clamp circuits are shown in Fig. 10. Although the holding voltages $V_{\rm hold}$ of ESD clamp circuits under dc measurement are somewhat lower than those under TLP measurement due to the self-heating effects [17], all the dc holding voltages exceed $2 \times V_{\rm DD}$ (2 V) with 0.8-V margin, which is very safe from latchup event.

The standby leakage current of the standalone 25-μm (50-μm) DTSCR in series with diode under 2-V bias at room temperature is only 4 nA (5 nA). Even if the 25-μm trigger PMOS is applied to the 25-μm (50-μm) DTSCR in series with diode, the standby leakage current under 2-V bias at room temperature is 148 nA (170 nA). As the 50-μm trigger PMOS is applied to the 25-μm (50-μm) DTSCR in series with diode, the standby leakage current under 2-V bias at room temperature is 264 nA (293 nA). Although the leakage current is increased with the insert of ESD detection circuit, the trigger voltage can be significantly reduced to effectively protect the core circuits. Therefore, the ESD clamp circuit of this work can provide the

TABLE I
COMPARISON AMONG ESD CLAMP CIRCUITS

ESD Detection Circuits	ESD Clamp Devices	Layout Area (μm^2)	TLP V_{t1} (V)	TLP I_{t2} (A)	HBM ESD (kV)	DC V_{hold} @ 25°C (V)	I_{Leak} @ 25°C / 2V (nA)	I_{Leak} @ 50°C / 2V (nA)	I_{Leak} @ 100°C / 2V (nA)
None	25-μm DTSCR + Diode	~500	11.8	1.6	2.6	2.8	4	4	6
	50-μm DTSCR + Diode	~1000	11.8	2.9	4.8	2.8	5	6	8
With 25-μm Trigger PMOS	25-μm DTSCR + Diode	~3000	6.7	1.6	2.6	2.8	148	349	1304
	50-μm DTSCR + Diode	~3500	7.3	2.8	4.8	2.8	170	368	1480
With 50-μm Trigger PMOS	25-μm DTSCR + Diode	~3500	6.0	1.6	2.6	2.8	264	571	2807
	50-μm DTSCR + Diode	~4000	6.5	2.9	4.8	2.9	293	871	3115

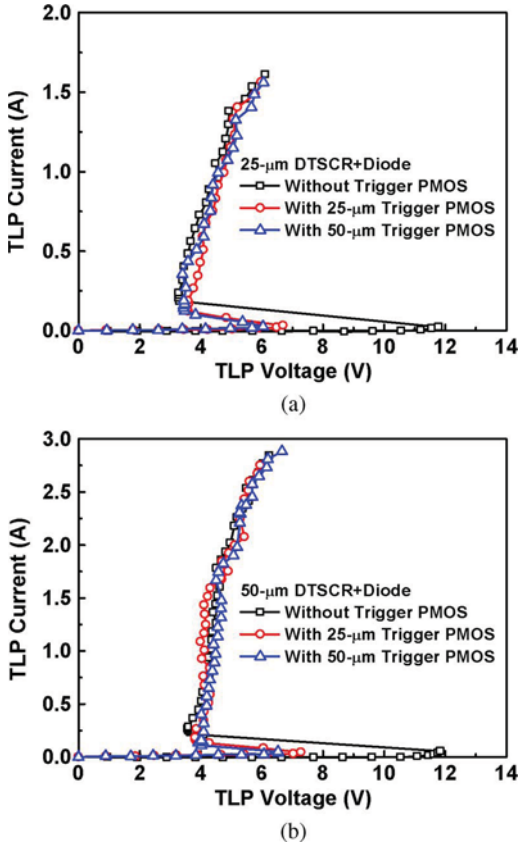

Fig. 9. TLP-measured I–V curves of $2 \times V_{DD}$-tolerant ESD clamp circuits with (a) 25-μm and (b) 50-μm ESD clamp devices.

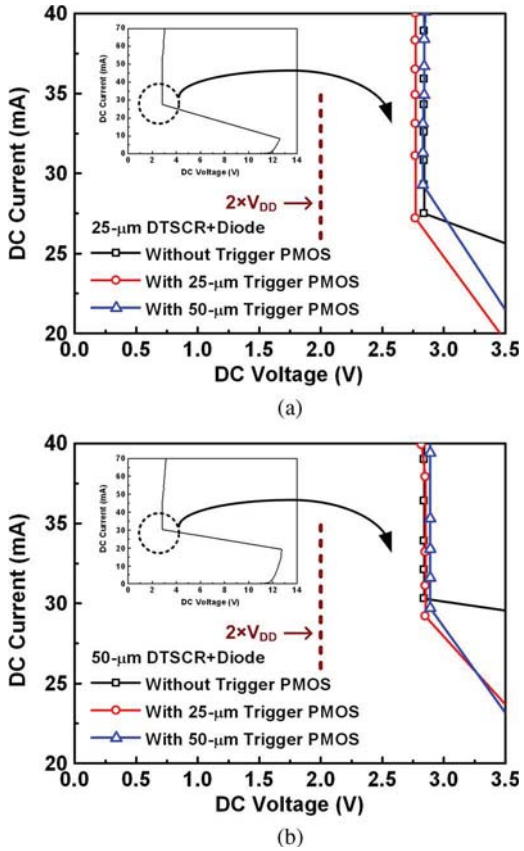

Fig. 10. Measured dc holding voltages of ESD clamp circuits with (a) 25-μm and (b) 50-μm ESD clamp devices under room temperature.

excellent ESD robustness with low standby leakage current by using only low voltage devices.

IV. CONCLUSION

The new $2 \times V_{DD}$-tolerant ESD clamp circuit by using only low-voltage devices with low standby leakage current and high ESD robustness for SoC applications with mixed-voltage I/O interfaces has been successfully designed and verified in a 65-nm CMOS process. The $2 \times V_{DD}$-tolerant ESD clamp circuit can operate without gate-oxide reliability issue, and the leakage current is only on the order of 100 nA under normal circuit operating condition. The HBM ESD robustness of the test patterns with 25- and 50-μm ESD clamp devices can achieve 2.6 and 4.8 kV, respectively. In addition, the new ESD detection circuit shows significant help on increasing the turn-on speed of the ESD clamp device. With trigger currents generated from the ESD detection circuit, the trigger voltage of the SCR-based ESD clamp device can be reduced, compared with the stand-alone SCR device. The TLP-measured trigger voltage of the ESD clamp device with the ESD detection circuit is ~6 V. In addition, the holding voltage of each ESD clamp circuits is ~2.8 V, which is much greater than $2 \times V_{DD}$ voltage (2 V). Therefore, there is no latchup concern in this design. The new ESD clamp circuit by using only low-voltage devices with very low standby leakage current and high ESD robustness is the useful circuit solution for on-chip ESD protection design with mixed-voltage I/O interfaces in SoC applications.

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