Design and implementation of readout circuit on glass substrate with digital correction for touch-panel applications

Tzu-Ming Wang (SID Student Member)
Ming-Dou Ker

Abstract — A readout circuit on glass substrate with digital correction, which contains a transconductance amplifier, counter, and digital correction circuit, has been designed for touch-panel applications for 3-μm low-temperature polysilicon (LTPS) technology. The voltage difference as a result of a change in capacitance due to a touch event is converted to current by a transconductance amplifier. By charging and discharging the capacitor in the counter, the counter displays different digital-output codes according to touch or non-touch events. Furthermore, not only can the touch or non-touch event be distinguished, but also the influence of LTPS process variation can be compensated by a digital correction circuit in the proposed readout circuit.

Keywords — *Readout circuit, low-temperature polysilicon (LTPS), system-on-panel (SOP), touch panel, digital correction.*

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1 Introduction

Low-temperature polysilicon (LTPS) technology exhibits numerous advantages over amorphous-silicon (a-Si) technology in display applications, resulting in high resolution, small size, low power, high reliability, and further reduction in cost. With such features, LTPS thin-film transistors (TFTs) can be utilized to achieve system-on-panel (SOP) applications, where some peripheral functional circuits can be integrated on the panel, such as a digital-to-analog converter, timing controller, DC–DC converter, and interface circuits. Furthermore, the operating voltage and device dimensions should decrease, resulting in low power consumption along with the integration of peripheral functional circuits on the panel.[1–4] Broadband services will be in great demand as wireless transmission speed increases. As a result, the features of using LTPS technology encourage the further spread of SOP applications.

SOP applications with LTPS TFTs have been in development for many years, and the integration of peripheral functional circuits have also been achieved.[5–7] Some works had been performed on the integration of peripheral functional circuits for SOP applications.[8–10] Recently, touch panels have gained significant interest and market penetration because of its intuitive operation and advantages of easier and faster entry of information for electronic devices such as PDAs, tabled PCs, and smart phones.[11] Capacitive-type touch panels have been widely adopted in high-end mobile applications due to the capability of multi- and soft-touch with higher durability and better light transmittance over resistive-type touch panels. Therefore, the integration of touch-screen panels, readout circuits, and other functional blocks together on a panel is highly desired in the industry for SOP applications.[12]

In this work, a new readout circuit on glass substrate for touch-panel applications has been proposed and designed for 3-μm low-temperature polysilicon (LTPS) technology.

2 On-panel readout circuit with digital correction

Figure 1 shows a block diagram of a touch-panel system. The structure of the touch-panel system is composed of an LCD, touch panel which is added to the LCD, and the readout circuit, on glass substrate. When the touch event happens, a conductive object like a finger will induce a capacitance change on the touch panel. The readout circuit is designed to distinguish such a touch event, which is directly implemented on glass substrate by placing TFT devices together on the LCD panel. There are a total of 14 and 8 capacitive sensor lines in the x and y directions, respectively, on the touch panel. When the touch panel is touched, the total capacitance of the capacitive sensor line will be changed. The voltage difference from the capacitance change due to a touch event on a panel is converted to current by a transconductance amplifier. By charging and discharging the capacitor in the counter, the counter displays different digital output codes under touch or non-

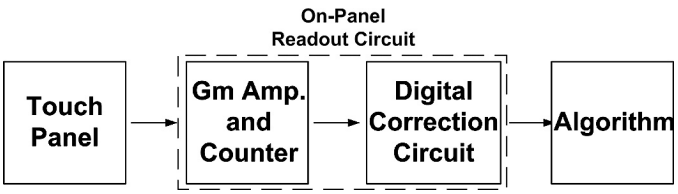

FIGURE 1 — A block diagram of a touch-panel system.

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T-M. Wang is with the Nanoelectronics and Gigascale Systems Laboratory, Institute of Electronics, National Chiao-Tung University, 1001 Ta-Hsueh Rd., Hsinchu, Taiwan 300, ROC.
M-D. Ker is with the Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan, ROC, and the Department of Electronic Engineering, I-Shou University, Kaohsuing, Taiwan, ROC; telephone +886-3-513-1573, e-mail: mdker@ieee.org.

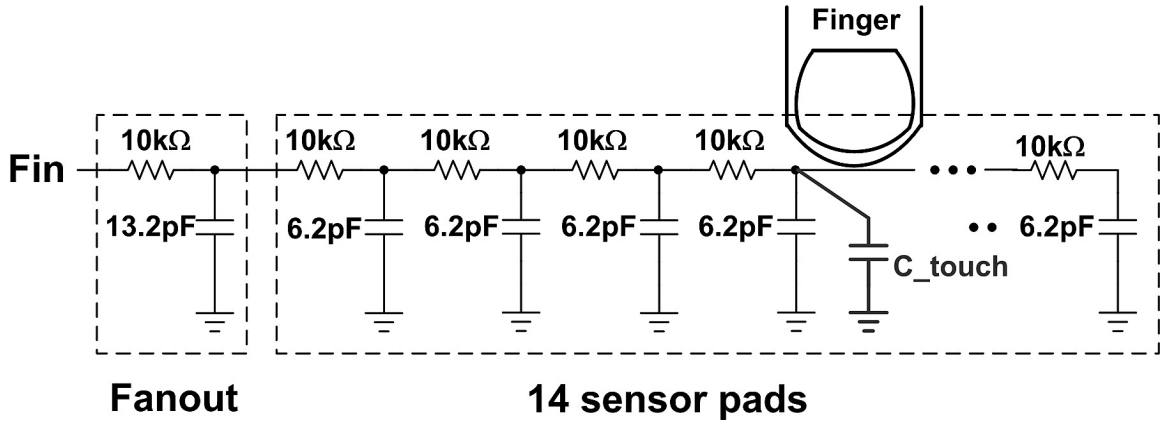

FIGURE 2 — The equivalent RC model of a one-capacitive sensor line on a 2.8-in. touch panel.

touch events. The digital output codes from the counter are periodically stored in the digital correction circuit. The touch or non-touch events can be distinguished by the digital output codes of the digital correction circuit having a compensation design against process variation. Finally, by analyzing the digital output codes, the corresponding functions, such as zoom in, zoom out, move, *etc.*, can be performed on the touch panel by the appropriate software algorithm in the microelectronic system.

2.1 Equivalent model of the capacitive sensor line

Figure 2 shows the equivalent RC model of a one capacitive sensor line on a 2.8-in. touch panel provided by the panel manufacturer with a total R of 150 kΩ and C of 100 pF. The Fanout block is the equivalent parasitic RC network of the interconnect line between the sensor line and the output node Fin. The touch capacitor (C_touch) is varied from 0.5 to 2 pF according to the different touch area. When the sensor line is touched by a finger, C_touch is added in parallel to the touched node and the total capacitance on the capacitive sensor line is also changed. In order to discriminate between the touch and non-touch events, by detecting the capacitance change from C_touch, each node on the sensor line is initially pre-charged to 10 V. When the touch event happened, the voltage at the output node Fin (V_{Fin}) will change to

$$V_{\text{Fin}} = \frac{C_{\text{total}}}{C_{\text{total}} + C\_\text{touch}} \cdot V_{\text{pre-charge}}, \qquad (1)$$

where $V_{\text{pre-charge}}$ = 10 V, C_{total} = 100 pF, and C_touch = 0.5–2 pF. Therefore, the voltage level at the output node Fin under a touch event can be derived from 9.8 to 9.95 V with a corresponding C_touch value from 2 to 0.5 pF. With such a capacitive sensor line, the capacitance change due to a touch event can be monitored by a voltage change. So, the on-panel readout circuit is designed to distinguish the voltage difference at the Fin node.

2.2 Circuit implementation and simulated results

Figure 3 shows the new proposed on-panel readout circuit with digital correction for touch-panel applications. The

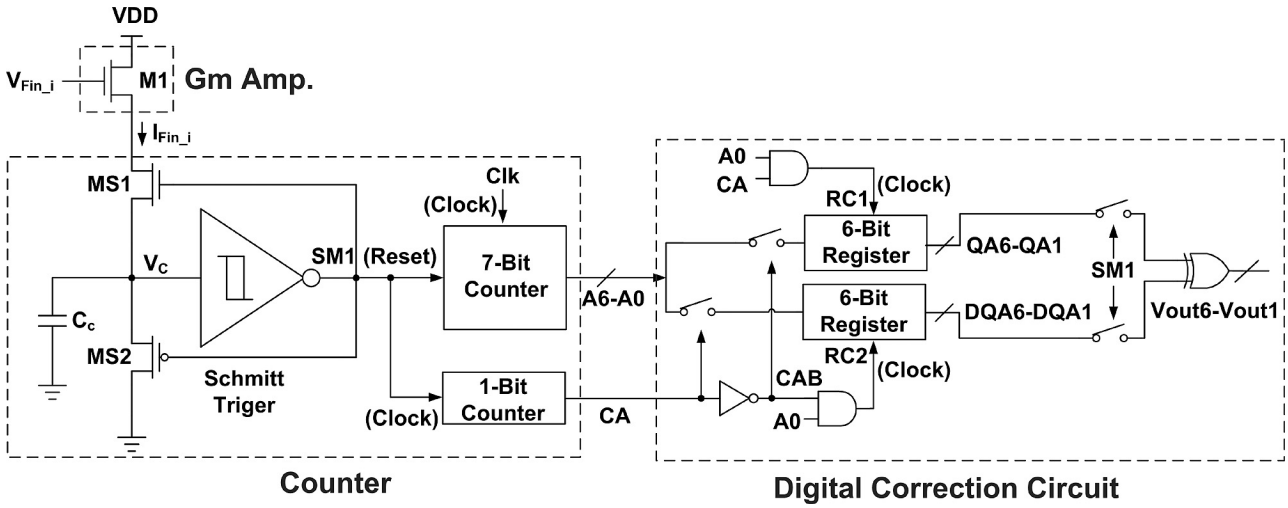

FIGURE 3 — New proposed on-panel readout circuit with digital correction to sense the voltage change due to the capacitance change caused by finger touch on a touch panel for 3-μm LTPS technology.

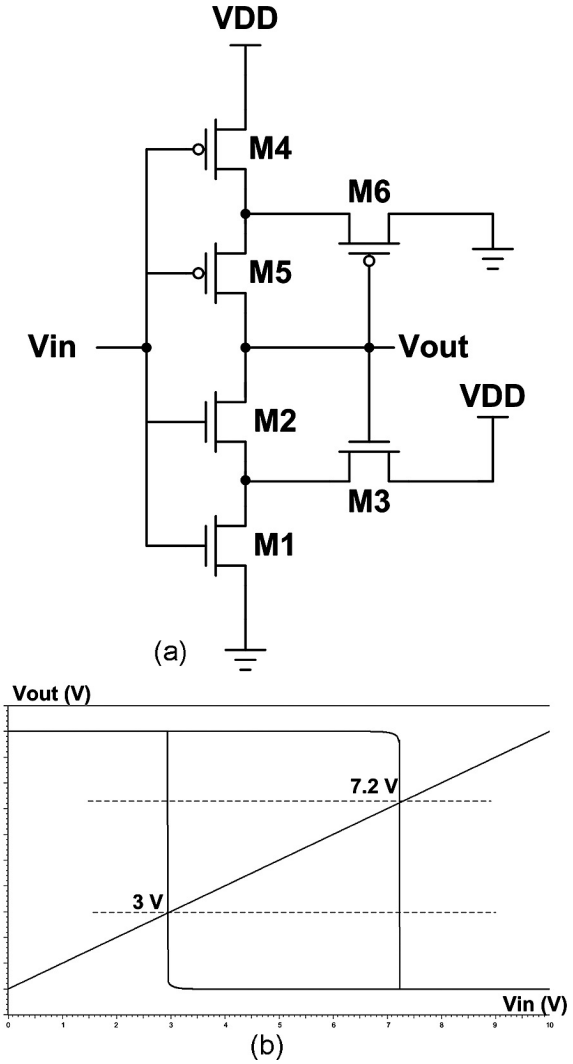

FIGURE 4 — (a) The schematic of a Schmitt trigger and (b) its simulated V_{in}–V_{out} characteristics.

proposed circuit is composed of three parts: transconductance amplifier (Gm.Amp.), counter, and digital-correction circuit. The gate of the Gm amplifier is connected to the Fin node of a one-capacitive sensor line shown in Fig. 2. In the i_{th} sensor line, the voltage variance at the Fin node is converted to different currents (I_{Fin_i}) by the Gm amplifier as the touch event happens. By charging the capacitor in counter (C_c), the voltage of capacitor (V_c) rises and the 7-bit counter begins to count. The Schmitt trigger is utilized to control the charge or discharge C_c by MS1 and MS2, and the output of the Schmitt trigger (SM1) is used as the reset signal of a 7-bit counter and the clock signal of a 1-bit counter. As V_c reaches the higher threshold voltage of the Schmitt trigger, MS2 is turned on and MS1 is turned off due to the low logic level of SM1. The 7-bit counter stops counting and V_c is decreases. When V_c reaches the lower threshold voltage of the Schmitt trigger, MS2 is turned off and MS1 is turned on due to the high logic level of SM1. The 7-bit counter starts counting again and V_c increases. Since the current of the Gm amplifier (I_{Fin_i}) is different due to a touch or non-touch event, the charging time of V_c is also

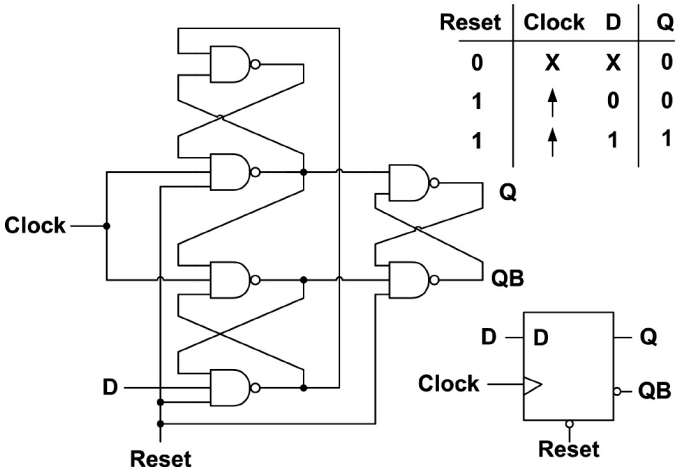

FIGURE 5 — The schematic, graphic symbol, and characteristic table of a positive-edge-trigger D-type flip-flop.[14]

different; *i.e.,* the 7-bit counter shows a different output (A6-A0) under touch or non-touch event. However, even under the same touch or non-touch events, 7-bit counters in different sensor lines show various outputs due to the process variation in LTPS technology. The digital correction circuit is necessary to overcome this issue.

In the digital correction circuit, two 6-bit registers are utilized to store the output from the 7-bit counter (A6-A1) periodically, according to the output of the 1-bit counter (CA). The least significant bit of the 7-bit counter (A0) is combined with CA by logical operation to perform the clock function of two 6-bit registers. Thus, the proposed circuit only needs one external clock signal, which is applied to the 7-bit counter. After that, the outputs of two 6-bit registers

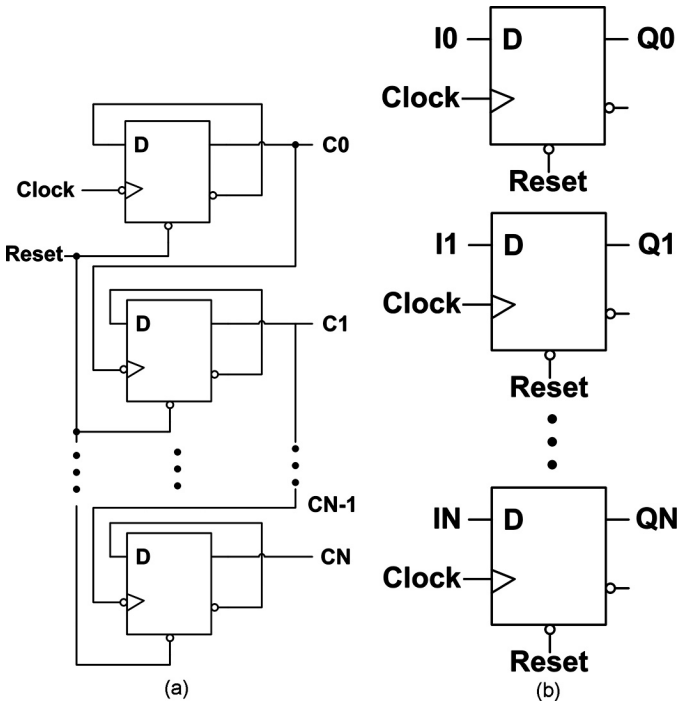

FIGURE 6 — The schematics of (a) N-bit counter and (b) N-bit register.

(QA6–QA1 and DQA6–DQA1) are compared by using the XOR gate as SM1 is at the low logic level. Some of the output of the XOR gate shows a high logic when the touch event happens and a low logic is displayed for all outputs of an XOR gate under a non-touch event. Even if 7-bit counters in a different sensor line show various outputs due to the process variation of LTPS technology, the digital correction circuit can compensate for the effect of process variation by storing output from the 7-bit counter (A6–A1) periodically and comparing the outputs of two 6-bit registers (QA6–QA1 and DQA6–DQA1) by the XOR gate.

Figure 4 shows (a) a schematic of the Schmitt trigger and (b) its simulated V_{in}–V_{out} characteristic. The hysteresis characteristic raises the switching point when the input is low and lowers the switching point when the input is high. The higher threshold voltage and lower threshold voltage of the Schmitt trigger are 7.2 and 3 V, respectively. Figure 5 shows the schematic, graphic symbol, and characteristic table of the positive-edge-trigger *D*-type flip-flop.[14] Two latches respond to the external *D* (data) and clock inputs, and the third latch provides the outputs for the flip-flop. In addition, one additional reset signal (Reset) is applied. When Reset = 0, the *D*-type positive-edge-trigger flip-flop is reset; *i.e.*, $Q = 0$ whether $D = 1$ or 0. Figure 6 shows the schematics of (a) an N-bit counter and (b) an N-bit register, which are implemented with a positive-edge-trigger D-type flip-flop shown in Fig. 5.

The proposed circuit has been designed and simulated by using Eldo software with the RPI model (Level = 62) in a 3-µm LTPS process.[15] Typical TFT properties provided by the foundry are listed in Table 1. The simulated output waveforms of (a) the top 6-bit register and (b) the bottom 6-bit register, in the proposed circuit under non-touch condition (V_{Fin_i} = 10V) is shown in Fig. 7 with V_{DD} = 10 V, MS1 = MS2 = 4 µm/20 µm, Cc = 10 pF, and Clk = 10 MHz. In Fig. 7, the output of the 7-bit counter is periodically stored separately in two 6-bit registers, and each output of the two 6-bit registers is held as the other one stores the output from the 7-bit counter. By applying the XOR gate to compare the outputs of the two 6-bit registers as SM1 = 0, each output of the XOR gate displays low logic level under the non-touch event. Therefore, the proposed circuit under non-touch conditions (V_{Fin_i} = 10 V) show all digital outputs (V_{out6}–V_{out1}) of 0. Since V_{Fin_i} is unchanged for a non-touch event, the current converted from the Gm amplifier, I_{Fin_i}, is the same to charge C_c in the counter. The period of the SM1 signal under a high logic level is identical to the output of the 7-bit counter, A6–A0, shows exactly the same digital codes. By applying the same digital codes of a 7-bit

TABLE 1 — Typical TFT properties in a 3-µm LTPS process.

	Threshold Voltage	Mobility	T_{ox}
NTFT	1 V	135 cm^2/V-sec	5.87×10^{-8} cm
PTFT	–0.8 V	115 cm^2/V-sec	5.87×10^{-8} cm

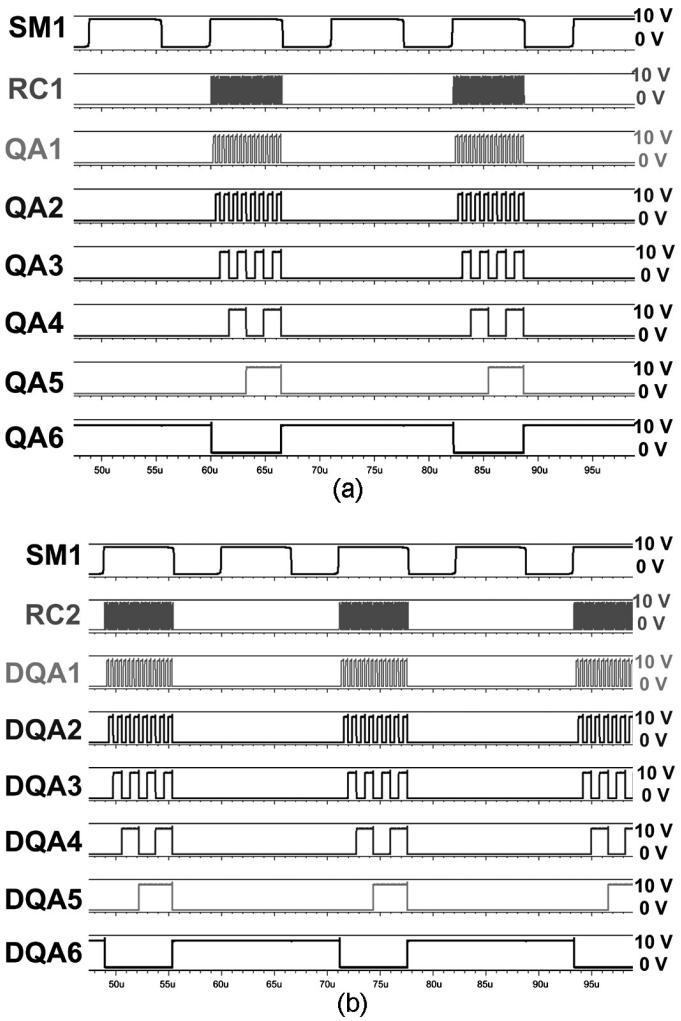

FIGURE 7 — The simulated output waveforms of (a) the top 6-bit register, and (b) the bottom 6-bit register in the proposed circuit under non-touch conditions (V_{Fin_i} = 10 V).

counter to a digital correction circuit, the output of the digital correction circuit exhibits 0 for a non-touch event. In the proposed circuit, the SM1 frequency is dependent on the current converted from the Gm amplifier, I_{Fin_i}, and the C_c in counter. A lower SM1 frequency results in higher sensitivity of the proposed readout circuit.

Figure 8 shows the simulated results of the proposed circuit for a 2-pF touch event (V_{Fin_i} = 9.8 V) to obtain digital outputs of 1 when (a) SM1 = 0 and (b) SM1 = 1. V_{Fin_i} changes from a non-touch event to a 2-pF touch event, and the current converted from the Gm amplifier, I_{Fin_i}, is different than the charge C_c in the counter before and after the touch event happens. Therefore, the period of the SM1 signal under a high logic level is different before and after the touch event happens so that the output of the 7-bit counter, A6–A0, shows some digital outputs of 1 from the non-touch event to the 2-pF touch event. Because the output of the 7-bit counter is stored separately in two 6-bit registers periodically, some outputs of the XOR gate show 1 right after the touch event happens and each output of the XOR gate displays a low logic level before the touch event happens and after some outputs of the XOR gate showing 1. Further-

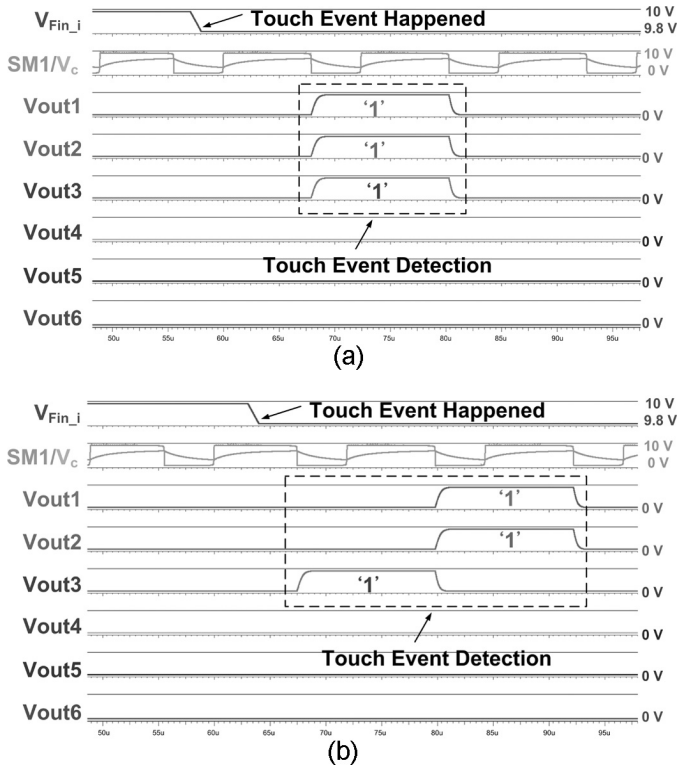

FIGURE 8 — The simulated results of the proposed circuit for a 2-pF touch event (V_{Fin_i} = 9.8 V) to obtain some digital outputs of 1 when (a) SM1 = 0 and (b) SM1 = 1.

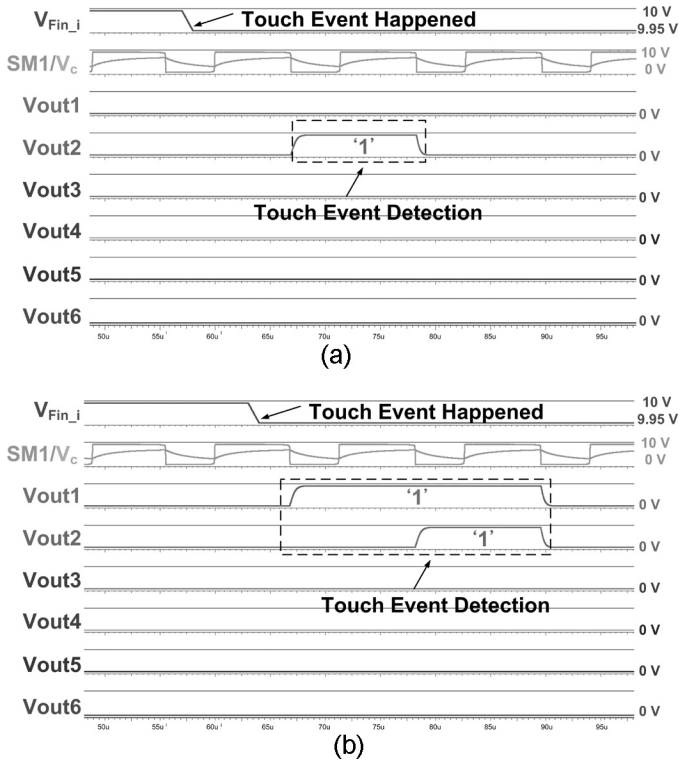

FIGURE 9 — The simulated results of the proposed circuit for a 0.5-pF touch event (V_{Fin_i} = 9.95 V) to obtain some digital outputs of 1 when (a) SM1 = 0 and (b) SM1 = 1.

more, the period for some outputs of the XOR gate showing 1 may be different under different touching times, *i.e.*, when SM1 = 0 and SM1 = 1 due to the effect of variant charging time on C_c. Figure 9 shows the simulated results of the proposed circuit under a 0.5-pF touch event (V_{Fin_i} = 9.95 V) to obtain some digital outputs of 1 when (a) SM1 = 0 and (b) SM1 = 1. Some digital outputs of the proposed circuit show 1 after the touch event happened. From Figs. 8 and 9, a larger voltage (V_{Fin_i}) variation results in higher-digital-output bit changes. Figure 10 shows the simulated waveforms of 6-bit outputs in the proposed circuit when it is changing with a successive non-touch event from a touch state under a (a) 2-pF and (b) 0.5-pF touch event. Some of the 6-bit outputs change from 0 to 1 to represent that the touch event happened, and they changed from 0 to 1 again under successive non-touch events from a touch state. By

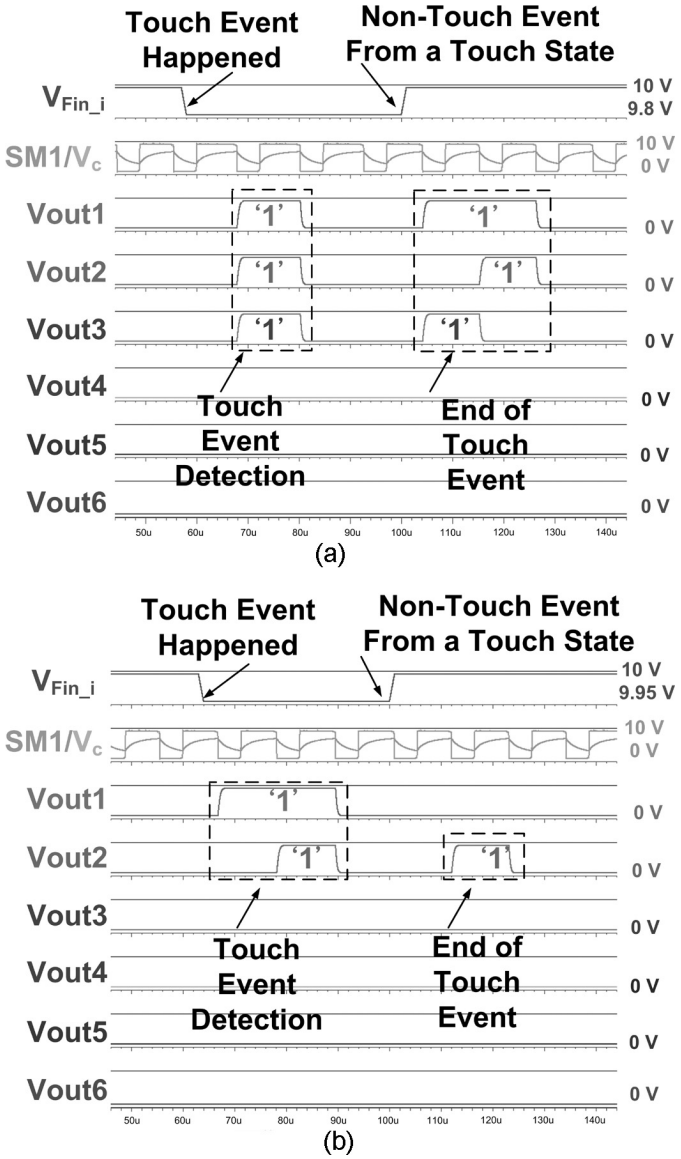

FIGURE 10 — The simulated waveforms of 6-bit outputs in the proposed circuit when it is changing with a successive non-touch event from a touch state for a (a) 2-pF and (b) 0.5-pF touch event.

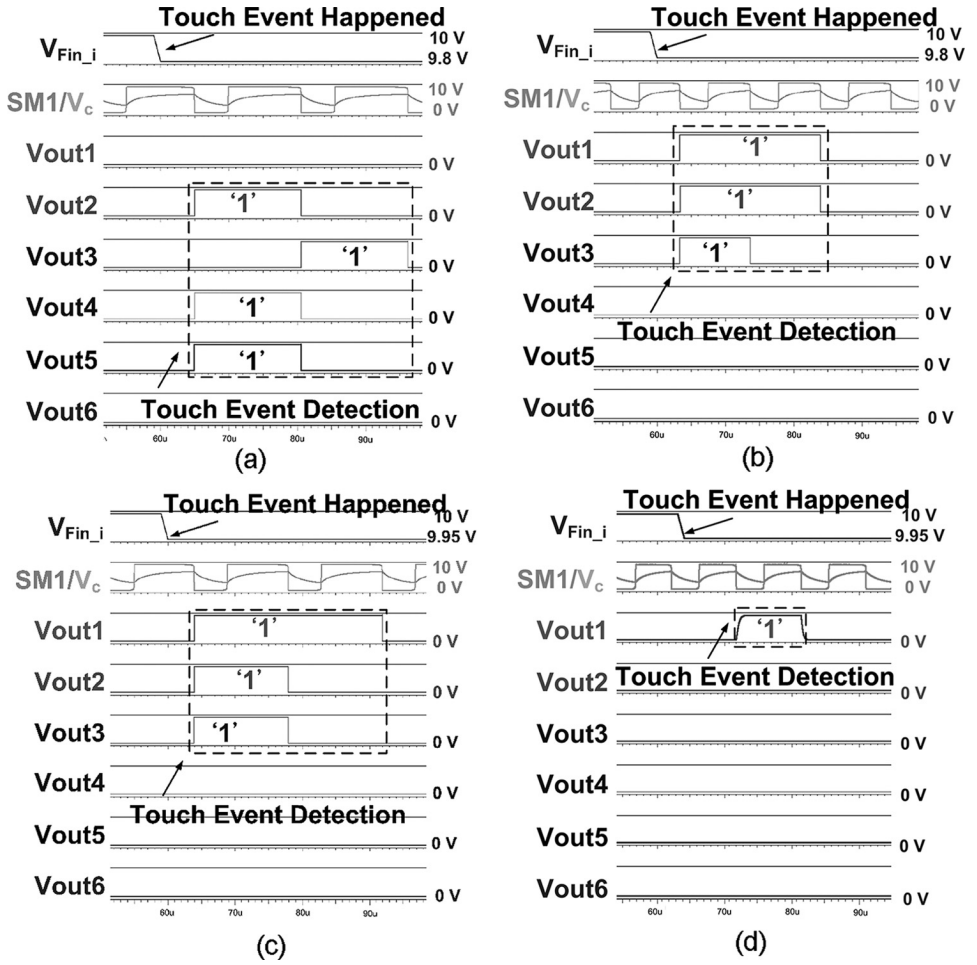

FIGURE 11 — The simulated results of the proposed readout circuit with (a) 2-pF touch event (V_{Fin_i} = 9.8 V) under +20% threshold voltage variation, (b) 2-pF touch event (V_{Fin_i} = 9.8 V) under –20% threshold voltage variation, (c) 0.5-pF touch event (V_{Fin_i} = 9.95 V) under +20% threshold voltage variation, and (d) 0.5-pF touch event (V_{Fin_i} = 9.95 V) under –20% threshold voltage variation.

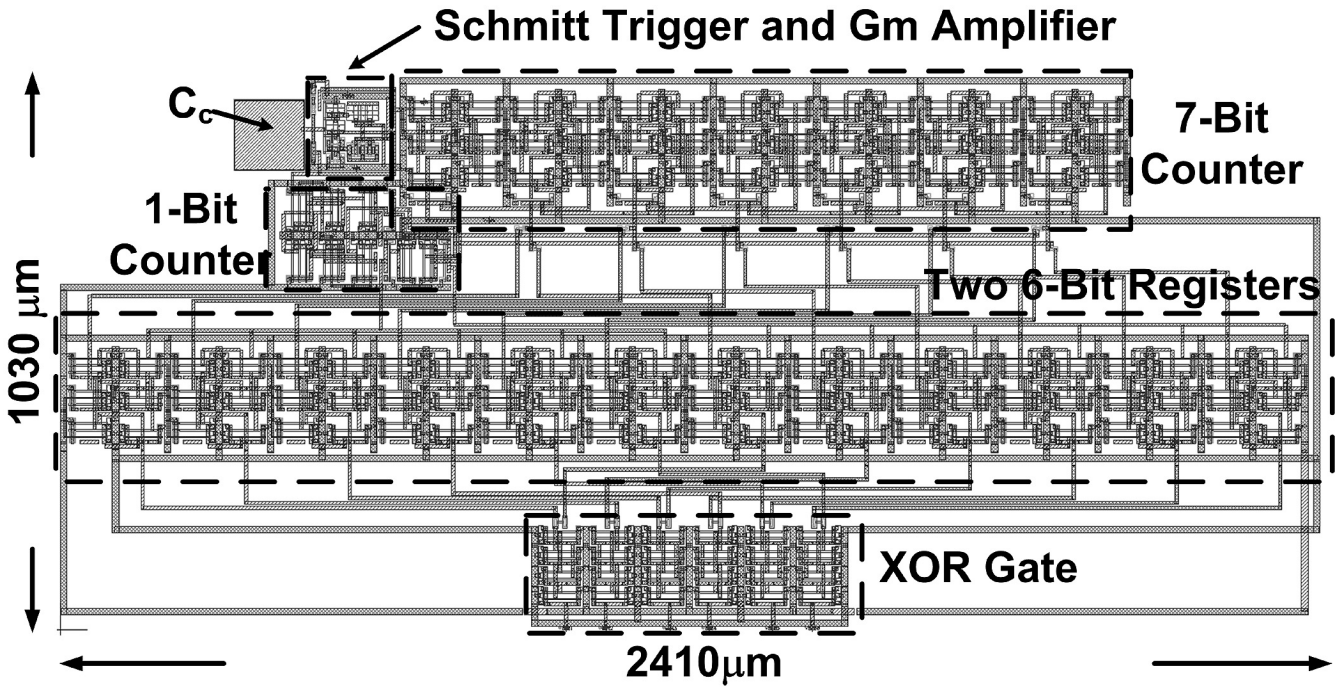

FIGURE 12 — The layout of the proposed circuit realized for 3-μm LTPS technology.

applying an algorithm to the touch-panel system mentioned in Fig. 1, the touch-panel system can correctly distinguish the touch state.

The weak part of the proposed circuit in Fig. 3 against the process variation is the Gm amplifier. According to the aforementioned circuit operation, the detection of a touch event is depended on the period of the SM1 signal for a high logic level, and this period is decided by the value of I_{Fin_i} from Gm amp. and Cc in the counter. Because the threshold voltage of Gm amp. will change due to process variation, it will result in different outputs of counter (A6–A0) in the different sensor lines even under the same touch event in the same LCD panel. Therefore, the output of the counters (A6–A0) cannot be directly utilized for the detection of a touch event. The digital correction circuit is essential to compensate for the influence of process variation and to ensure the accuracy of the detection of the touch event. By storing the outputs of the counter onto the two 6-bit registers periodically and comparing them through the XOR gate as SM1 is in the low logic level, some of the output from the XOR gate show a high logic level when some of the outputs from the two 6-bit registers show a different logic level. Therefore, the influence of process variation, which results in different outputs from the counters (A6–A0) in the different sensor lines for the same touch event in the same LCD panel can be compensated by the digital correction circuit.

By considering the influence of process variation of LTPS technology on the proposed circuit, the 20% threshold-voltage variation of pTFT and nTFT are simulated in a 3-μm LTPS technology. Figure 11 shows the simulated results of the proposed readout circuit with (a) a 2-pF touch event (V_{Fin_i} = 9.8 V) under +20% threshold voltage variation, (b) a 2-pF touch event (V_{Fin_i} = 9.8 V) under –20% threshold-voltage variation, (c) a 0.5-pF touch event (V_{Fin_i} = 9.95 V) under +20% threshold-voltage variation, and (d) a 0.5-pF touch event (V_{Fin_i} = 9.95 V) under a –20% threshold-voltage variation. Although the outputs of counters (A6–A0) are different under threshold-voltage variation even in the same touch event (2 or 0.5 pF), the proposed circuit can still distinguish the touch or non-touch event by comparing the outputs from two 6-bit registers and display a high logic level in some outputs from the digital correction circuit (V_{out6}–V_{out1}). According to the simulated results, the proposed readout circuit on glass substrate with digital correction can not only distinguish the touch or non-touch event, but also can compensate for the influence of process variation by a digital correction circuit.

The layout of the proposed circuit is illustrated in Fig. 12, realized in a 3-μm LTPS technology with an area of 1030 × 2410 μm. The proposed circuit is composed of a Gm amplifier, Schmitt trigger, 1-bit counter, 7-bit counter, two 6-bit registers, and one XOR gate. The fabricated chip used to verify this design is now under wafer fabrication. The measured results in a glass chip will be shown in the future.

3 Conclusion

A readout circuit on glass substrate with digital correction for touch-panel application, which contains a Gm amplifier, counter, and digital correction circuit, has been designed and simulated in a 3-μm low-temperature polysilicon (LTPS) technology. In this work, the voltage difference from a capacitance change due to a touch event on a panel is converted to current by the Gm amplifier. By charging and discharging the capacitor in the counter, the counter displays different digital output codes according to a touch or non-touch event. According to the simulated results, the proposed readout circuit on glass substrate with digital correction can successively distinguish the touch or non-touch events by using a digital correction circuit to compensate for the influence of process variation.

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Tzu-Ming Wang received his B.S. degree from the Department of Electronics Engineering, National Chiao-Tung University, Hsinchu, Taiwan, R.O.C., in 2005. He is currently working toward his Ph.D. degree at the Institute of Electronics, National Chiao-Tung University. His current research interests include analog circuit design on glass substrate and mixed-voltage I/O circuit design for low-voltage CMOS technology.

Ming-Dou Ker received his Ph.D. degree from the Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan, in 1993. From 1994 to 1999, he worked in the VLSI Design Division, Computer and Communication Research Laboratories, Industrial Technology Research Institute (ITRI), Hsinchu, Taiwan. Since 2004, he has been a full Professor with the Department of Electronics Engineering and Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan. From 2008, he was rotated to be Chair Professor and Vice-President of I-Shou University, Kaoshiung, Taiwan. In 2010, he became a Distinguished Professor in the Department of Electronics Engineering, National Chiao Tung University, and he also served as the Executive Director of the National Science and Technology Program on System-on-Chip (NSoC) in Taiwan. In the field of reliability and quality design for circuits and systems in CMOS technology, he has published over 400 technical papers in international journals and conferences. He has proposed many inventions to improve the reliability and quality of integrated circuits, which have been granted with 180 U.S. patents and 155 R.O.C. (Taiwan) patents. His current research interests include reliability and quality design for nanoelectronics and gigascale systems, high-speed and mixed-voltage I/O interface circuits, on-glass circuits for system-on-panel applications, and biomimetic circuits and systems for intelligent prosthesis. He has been invited to teach or to consult on reliability and quality design for integrated circuits by hundreds of design houses and semiconductor companies in the worldwide IC Industry. He has served as a member of the Technical Program Committees and the Session Chair of numerous international conferences. He served as the Associate Editor for the *IEEE Transactions on VLSI Systems*. He has been selected as a *Distinguished Lecturer* in the IEEE Circuits and Systems Society (2006–2010) and in the IEEE Electron Devices Society (2008–2009). He was the President of the Foundation of Taiwan ESD Associations. In 2009, he was selected as one of the top ten *Distinguished Inventors* in Taiwan; and one of the top hundred *Distinguished Inventors* in China. In 2008, Prof. Ker was elevated as an IEEE Fellow with the citation of "*for contributions to electrostatic protection in integrated circuits, and performance optimization of VLSI micro-systems.*"