Digital time-modulation pixel memory circuit in LTPS technology

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Abstract — A digital time-modulation pixel memory circuit on glass substrate has been designed and verified for a 3-µm low-temperature polysilicon (LTPS) technology. From the experimental results, the proposed circuit can generate 4-bit digital codes and the corresponding inversion data with a time-modulation technique. While the liquid-crystal-display (LCD) panel operates in the still mode, which means the same image is displayed on the panel, a data driver for an LCD panel is not required to provide the image data of the frame by the proposed pixel memory circuit. This pixel memory circuit can store the frame data and generate its corresponding inversion data to refresh a static image without activating the data driver circuit. Therefore, the power consumption of a data driver can be reduced in the LCD panel.

Keywords — *Memory-in-pixel (MIP), low-temperature polysilicon (LTPS), system-on-panel (SOP), time modulation.*

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1 Introduction

Low-temperature polysilicon (LTPS) technology exhibits numerous advantages over amorphous-silicon (a-Si) technology in display applications, resulting in high resolution, small size, low power, high reliability, and a further reduction in cost. For these features, LTPS thin-film transistors (TFTs) are utilized in system-on-panel (SOP) applications, where some peripheral functional circuits are integrated on the panel, such as driver circuits, a digital-to-analog converter, a timing controller, a DC–DC converter, and interface circuits.[1–3] The trends in mobile system-on-panel (SOP) liquid-crystal displays (LCDs) was reported in Ref. 3, where broadband services are in great demand as wireless transmission speed is increasing. Thus, the features of LTPS technology in high demand to encourage the further spread of SOP applications. In addition, LTPS TFT-LCD technology is widely used for mobile displays at a competitive price and with excellent visual performance.[4,5]

Figure 1 shows a cross-sectional view of LTPS TFT technology.[6] The fabrication process starts with the buffer layer, which was deposited on glass substrate. Then, the undoped 50-nm-thick a-Si layer was deposited and crystallized by using a XeCl excimer laser with a laser energy density varying from 340 to 420 mJ/cm^2. The recrystallized poly-Si films were patterned into the active islands. Afterwards, a 60-nm-thick oxide layer was deposited as the gate insulator. Then, the 200-nm-thick molybdenum layer was deposited and patterned as the gate electrode. The n^- doping was directly self-aligned to the gate electrode without the use of an additional mask process. The n^+ source/drain regions were defined by one mask. The dopants were activated by a thermal process. After the deposition of nitride passivation and the formation of contact holes, the 550-nm-thick titanium/aluminum/titanium trilayered metal was deposited and patterned to be the metal pads. Typical TFT properties provided by the foundry are listed in Table 1.

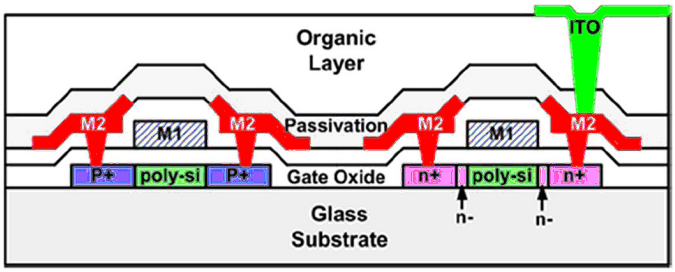

FIGURE 1 — Cross-sectional view of LTPS TFT technology (Ref. 6).

The market for mobile SOP LCDs has been rapidly expanding due to the aforementioned features of LTPS technology. Some practical implementations of SOP LCDs has been developed for mobile-phone displays with a 2.2–2.4-in. QVGA resolution.[7,8] In addition, a non-volatile memory was demonstrated on glass substrate for possible panel applications.[9] As the circuit-integration level progressed, the driving voltage and design rule should decrease resulting in low-power consumption. However, the power consumption of a SOP driver circuit tends to be higher than

TABLE 1 — Typical TFT properties in a 3-µm LTPS process.

	Threshold voltage (V)	Mobility (cm^2/V-sec)	T_{ox} (10^{-8} cm)
NTFT	1	135	5.87
PTFT	–0.8	115	5.87

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that of silicon ICs because poly-Si TFTs are fabricated with larger design rules, higher threshold voltages, and lower mobility. Therefore, power reduction in the SOP LCD circuit is one of the major challenges in expanding the mobile SOP-LCD market further.

Recently, a memory-in-pixel (MIP) circuit has attracted lots of interest for low-power applications. By refreshing the voltage level of the scan line with a MIP circuit, polarity inversion can be easily produced even though the data is no longer provided. The prior MIP designs are based on digital memory circuits, which require digital data to display gray levels on the pixel with SRAMs, DRAMs, or capacitors.[10,11] Although these digital memory circuits can produce normal frame data and easily reach the polarity inversion, the resolution and image quality of the display are limited by the number of bits in the digital memory circuit. On the contrary, analog memory uses storage capacitors and driving transistors to provide the normal and inversion voltages for panel applications.[12]

In this work, a 4-bit digital time-modulation pixel memory realized with TFTs on glass substrate has been proposed and successfully verified for a 3-μm LTPS process.[13] The proposed pixel memory is composed of one DRAM, one latch, and two control switches accompanied by time-modulation digital data to display different gray levels on the panel.

2 Conventional pixel memory

2.1 Concept of embedded pixel memory

An LCD frame displays can be separated into normal mode and still mode. The normal mode shows a continuous frame of an LCD, and the still mode shows a static frame on an LCD. For a conventional LCD driver, it sends data to the pixel through the data line; these data are the same in the still mode. Therefore, the data driver of conventional LCD panel causes unnecessary power consumption. Figure 2 shows a block diagram of the LCD panel which contains the display panel, data driver, scanning driver, and the embedded pixel memory circuit. The concept of the embedded pixel memory is to drive the LCD by only using the pixel itself when displaying a still image, which means that no additional charging current of the data driver is required in the still mode. This resulted in ultra-low-power operation for the LCD driver.[14]

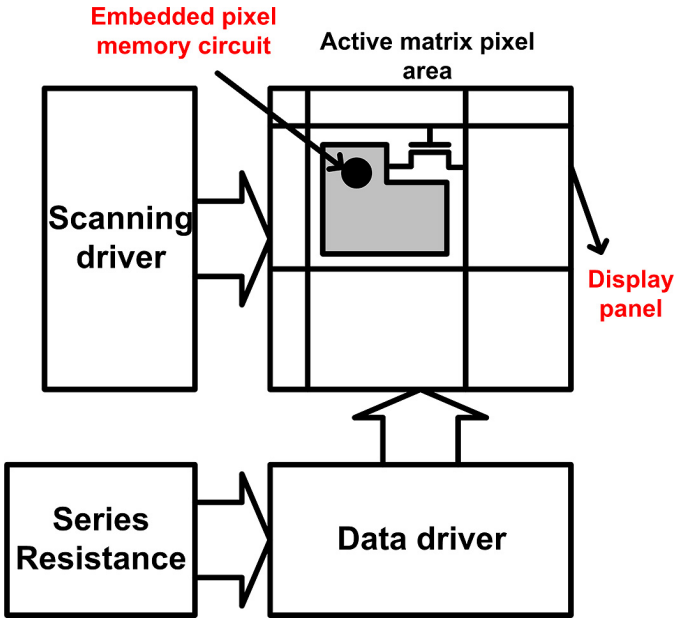

FIGURE 2 — Block diagram of LCD panel on glass substrate with an embedded pixel memory circuit (Ref. 12).

2.2 1-bit digital pixel memory

Recently, some works tried to reduce the power consumption of LTPS TFT-LCDs for portable electronic equipment,[13–15] that is, the operating frequency of the LCD panel can be reduced resulting in low power consumption in the still mode. The embedded memory circuits using LTPS TFTs in the pixel can display a still image without driving the data line from the data driver. There are two types of memory used to memorize the data for displaying the still image in the pixel. One is the dynamic memory and the other is the static memory.[15–17] In Fig. 3(a), it consists of a pixel gate switch (M1), digital memory (which stores the digital frame data), and two switches (M2, M3) to select frame data or its corresponding inversion data. C_{lc} is the liquid-crystal capacitor and C_s is the storage capacitor. Since the digital memory stores digital data (high or low voltage levels), the pixel can display only black or white to show a 1-bit RGB image (eight colors) in the still mode. Figure 3(b) shows the timing chart of such a pixel with a 1-bit digital memory from the normal mode to the still mode. For the normal mode, controller signals SPOLA and SPOLB are low in order to cut the electrical path between the pixel electrode and digital memory, and this pixel is driven as a conventional pixel. In the pre-still mode, the digital memory becomes active to read and memorize the data. Then, the data driver and gate driver are turned off, and the pixel is driven by the data stored in the digital memory in the still mode. When the memory circuit provides the normal frame data, SPOLA is high, SPOLB is low, and the counter electrode is at a low-voltage level. When the memory circuit provides the corresponding inversion frame data, SPOLA is low, SPOLB is high, and the counter-electrode is at a high-voltage level. Therefore, the data driver of the LCD panel is not required in order to operate in the still mode, and only a small amount of power is consumed to drive the control signals (SPOLA and SPOLB).

2.3 Area-coverage modulation

The characteristic of area-coverage modulation for the pixel memory is to store weighted digital data according to the area of the pixels. One pixel area is divided into the binary-

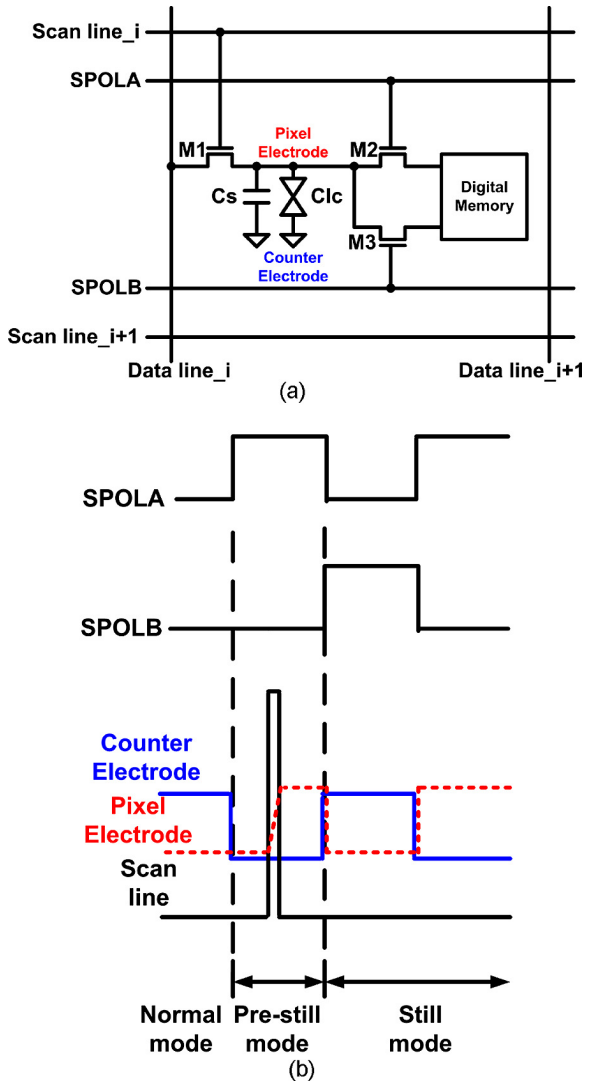

FIGURE 3 — (a) Schematic diagram of static memory in a pixel and (b) the timing chart of operations from normal mode to still mode (Ref. 13).

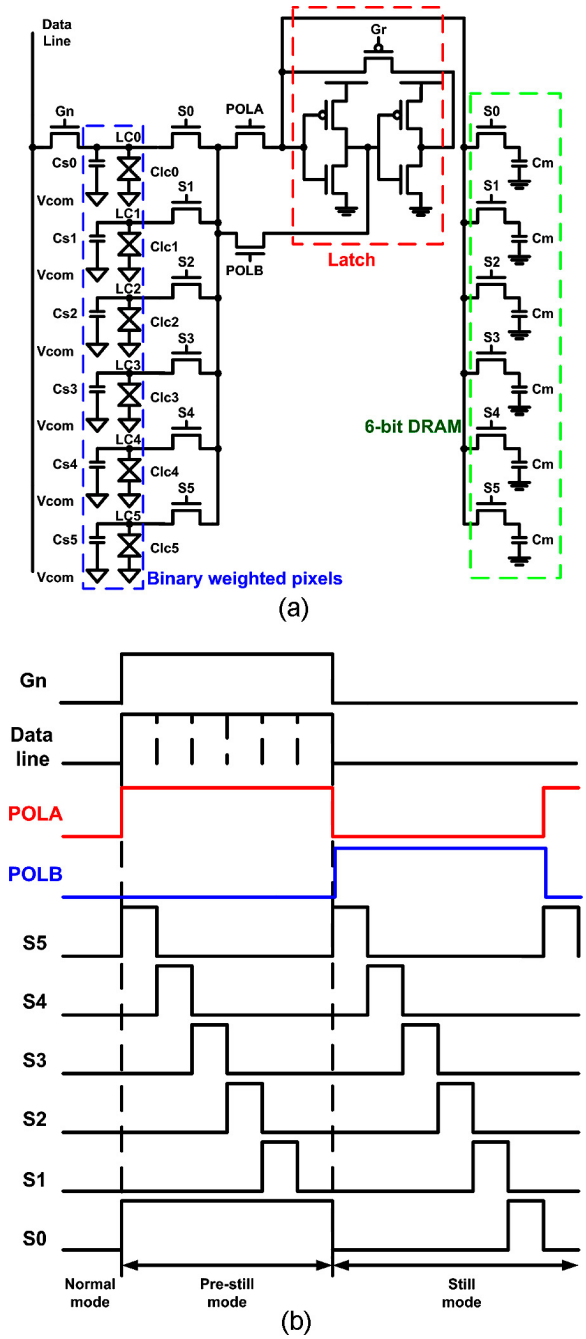

FIGURE 4 — (a) Schematic diagram of area-modulation pixel memory and (b) the corresponding time diagram of control signals (Ref. 17).

weighted area, and each area displays black or white according to the digital data of the area-coverage modulation technique. By mixing different white or black pixel areas, different gray levels can be displayed. An N-bit RGB image on the panel can be displayed in the still mode by dividing the pixel into n parts.[18] Figure 4(a) shows a schematic diagram of a 6-bit area-coverage modulation pixel memory, which contains one latch, a 6-bit DRAM, and binary-weighted pixels. Figure 4(b) shows the time diagram of the corresponding control signals.[19]

In Fig. 4(a), the pixel is divided into six parts: C_{lc0}–C_{lc5}, in a binary-weighted manner. So, the total area of the original pixel is divided into C_{lc0}–C_{lc5} with a ratio of 32:16:8:4:2:1. In the normal mode, POLA and POLB are low in order to cut the electrical path between pixel electrodes (LC_0–LC_5), latch, and 6-bit DRAM, and this pixel is driven as a conventional pixel. In the pre-still mode, the 6-bit DRAM is programmed to memorize data from the data line. S_0–S_5 turns on in turn to store the corresponding digital data into the 6-bit DRAM. Then, in the still mode, the data driver and gate driver are turned off, and the pixel is driven by the digital data stored in the 6-bit DRAM. When the 6-bit DRAM provides the normal frame data, POLA is high and POLB is low. However, when the 6-bit DRAM provides the corresponding inversion frame data, SPOLA is low and SPOLB is high. S_0–S_5, POLA, and POLB are alternated to reverse the voltage polarity applied at the pixel electrodes (LC_0–LC_5) in every frame time. As a result of this area-coverage modulation, the LCD panel consumes low power in the still mode because the data diver circuit does not require the same data to be sent to the pixel.

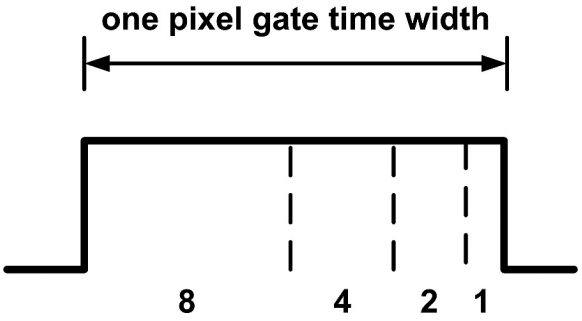

FIGURE 5 — Time-width dividing for time-modulation technique.

3 Design and realization of 4-bit digital time-modulation pixel memory

3.1 Theoretical operation and circuit implementation

There are two methods used to mix different gray levels for the for digital pixel memory. One is the aforementioned area-coverage modulation, which shows gray levels by displaying white and black for different area coverage of the pixel. The other method uses the time-modulation technique. In a fixed time period, the desired gray levels can be displayed by applying a high or low logical voltage on the pixel in different time widths.[20] Figure 5 illustrates the dividing time width for the time-modulation technique. For a 4-bit modulation, a fixed time period, which is a one-pixel gate time width, is divided into the binary-weighted ratio of 8:4:2:1. By deciding the white or black pixel for each binary-weighted time width to provide a high or low voltage level in these time periods, the pixel can mix different time widths to display the desired gray levels.

Figure 6(a) shows a schematic diagram of the proposed 4-bit digital time-modulation pixel memory which contains a latch (M4, M5, M6, M7, and R1), a 4-bit DRAM (M8, M9, M10, M11, and C_m), and two controlling switches (M2, M3) used to decide whether to select the inversion data or not. Compared to the area-coverage modulation, the proposed circuit does not have to divide the pixel into several parts, so the aperture for the LCD panel can be increased. In the latch, it has two stable states and is built by a pair of cross-coupled inverters and one resistor. While the data line provides a high or low voltage level to the latch (V_{Lc}), the given signal will be written to the 4-bit DRAM sequentially. Therefore, the 4-bit signals can be maintained to avoid the leakage charge issue under the operation of the proposed circuit. Besides, to further increase the state's writing efficiency, one capacitor is designed and located in the feedback loop to reduce the budgets from state renewing. Figure 6(b) shows the control signal for this time-modulation design. In the normal mode, M2 and M3 are off so that the LCD panel works as the original pixel circuit. In the pre-still mode, the corresponding digital value for each time interval are stored in 4-bit DRAMs with M2 on, M3 off, and S_0–S_3 become high in turns. In the still mode, M1 is off and the pixel memory circuit can produce the time-modulation

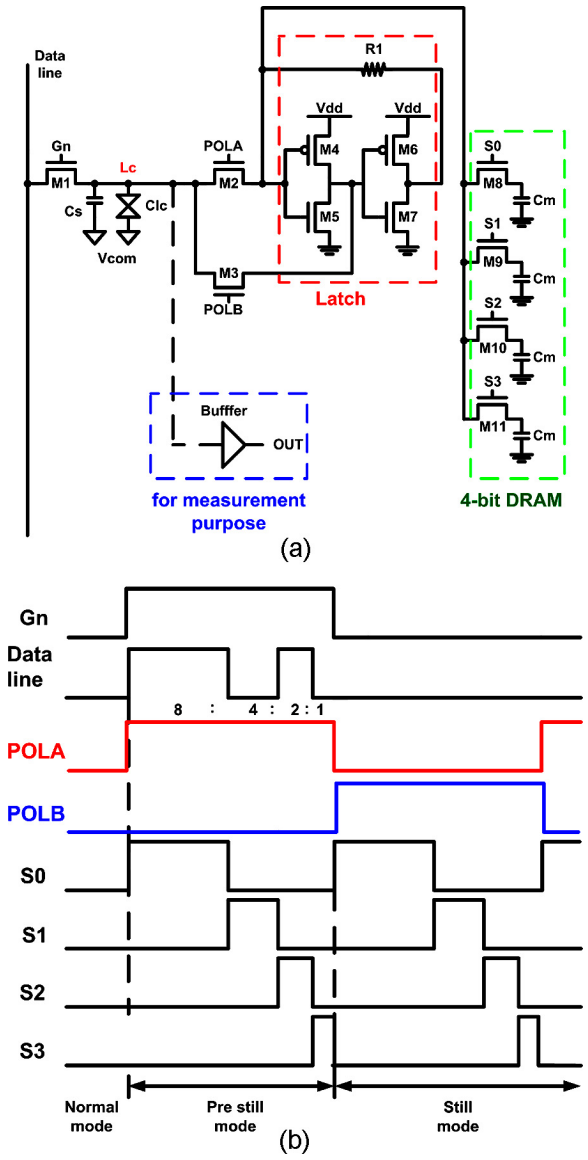

FIGURE 6 — (a) Schematic diagram of time-modulation digital pixel memory and (b) the corresponding time diagram of the control signals.

digital signal at the LC node without data provided from the driver circuit. As the proposed circuit operates in the still mode, M2 and M3 will turn on alternatively. When the normal frame data is applied, M2 will turn on and M3 will turn off. When the corresponding inversion data is needed, M3 will turn on and M2 will turn off, and the corresponding digital value will produce an inverting value at the LC node through one inverter (M4, M5). By turning M2 and M3 on in turn, the pixel memory circuit can perform inversion without reading the data from the driver circuit.

The desired gray levels can be displayed by applying a high or low logical voltage on the pixel in different time widths in a fixed time period in the proposed circuit. With higher operating frequency, the fixed time period is smaller and the binary-weighted time ratio is more difficult to achieve. The operating margin is highly relative to the process and requirement of the display panel.

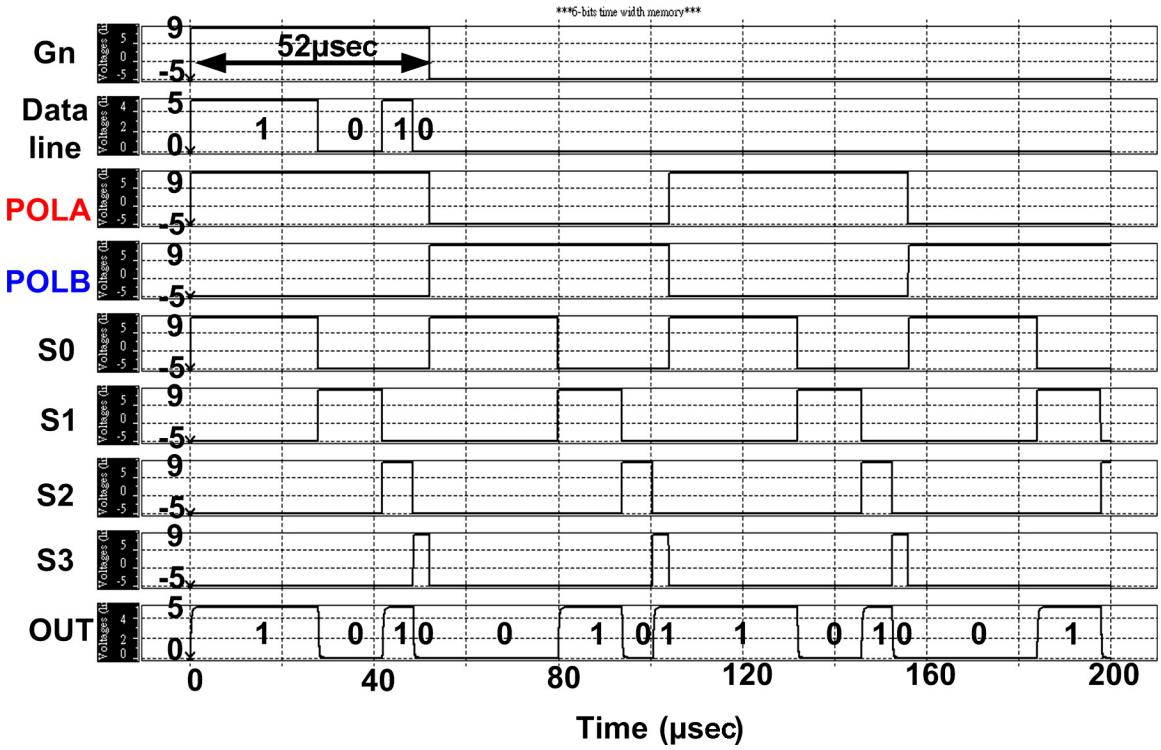

FIGURE 7 — The simulated result of the digital time-modulation pixel memory circuit.

3.2 Simulation results

Considering the parasitic capacitor in the experimental measurement, a buffer is added to the LC node. Such a buffer is especially drawn in the test panel to verify the function of the proposed time-modulation design. In real panel applications, the pixel does not need this buffer. A test pattern and its simulation timing chart are shown in Fig. 7. The controlling signal of G_n, POLA, POLB, and S_0–S_3 are set as from –5 to 9 V to make sure that all TFT switches fully turn on and off. The test pattern is given as "1010" with a binary-weighted ratio of 8:4:2:1 for 4-bit time-modulation on the data line and its voltage range is from 0 to 5 V. Because one frame time for a 2.8-in. QVGA display is 16.7 msec, the time width of G_n is 16.7 msec/320 = 52 µsec, and the duty cycle of S_0:S_1:S_2:S_3 is 8:4:2:1 with a V_{dd} of 5 V, V_{ss} of 0 V, $C_{lc} + C_s$ of 300 fF, and C_m of 600 fF. In Fig. 6, G_n is high, so the data "1010" from the data line is directly delivered to the OUT node in the pre-still mode. Besides, the corresponding digital value for each time interval are stored in a 4-bit DRAM as M2 is on and S_0–S_3 becomes high in turns. When G_n is low, the pixel memory is operated in the still mode. "0101" is shown in the OUT node when M3 is on, which means the inversion data has been produced by the proposed circuit successfully. Through such a simulation, the operation of the proposed time-modulation circuit can be verified.

According to the simulated results, the power consumption of the proposed circuit in the normal and still modes are 25.15 and 0.46 µW per pixel, respectively. The scan driver and data driver are not included in the proposed circuit for power-consumption simulation due to the limited chip area. However, by storing the frame data and generating its corresponding inversion data to refresh the static image without activating the data driver circuit, the power consumption of the proposed circuit can be reduced. Also, the aperture for the LCD panel in the proposed circuit is higher because the occupied area from a complicated routing for each binary-weighted pixel can be further decreased.

4 Experimental results

The proposed 4-bit time-modulation digital pixel memory circuit has been fabricated on glass substrate in 3-µm LTPS

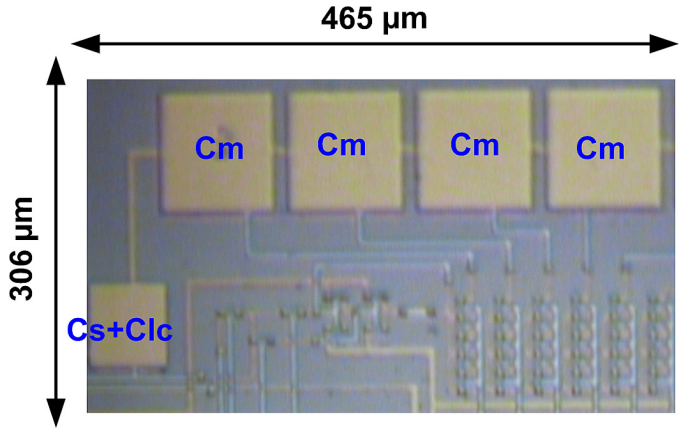

FIGURE 8 — Photograph of the fabricated 4-bit time-modulation digital pixel memory in 3-µm LTPS technology.

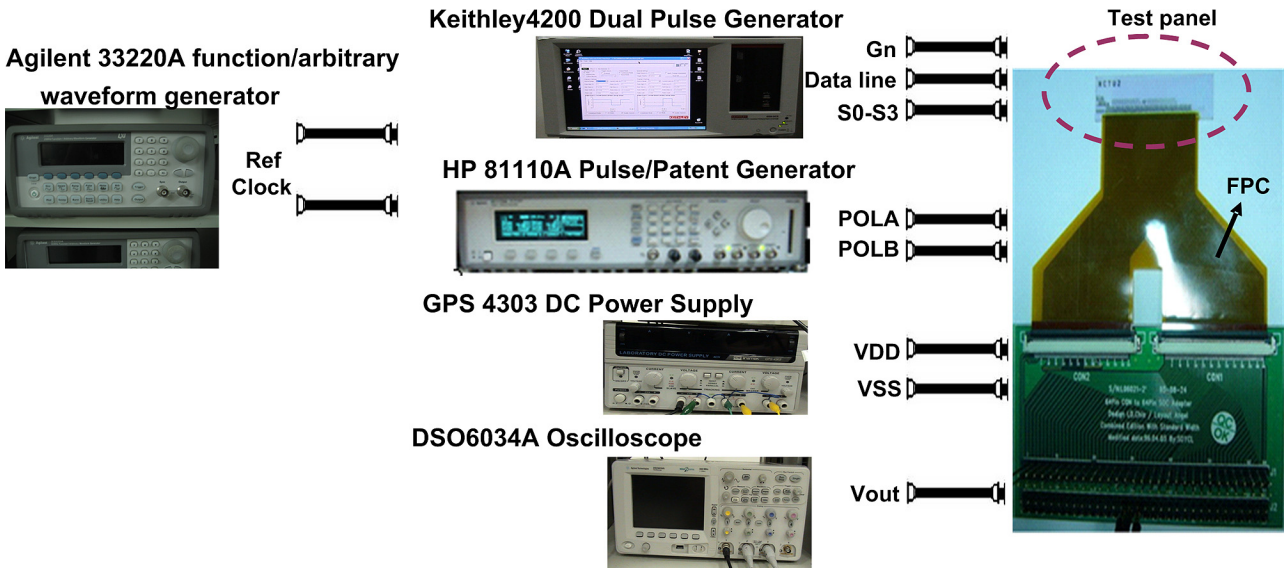

FIGURE 9 — The measurement setup to verify the fabricated pixel memory.

technology. A photograph of the fabricated pixel memory circuit is shown in Fig. 8 for a size of 306 × 465 µm in a test panel. The capacitors, C_{lc}, C_s, and C_m, utilized in the proposed circuit are implemented by placing a metal–insulator–metal between M1 and M2. The equivalent capacitance of C_{lc} and C_s is 0.3 pF, and the capacitance of C_m is 0.6 pF. To observe the operations of the proposed time-modulation pixel memory circuit with the parasitic loading capacitance (about 10 pF), a buffer is added to the LC node for measurement purposes.

The measurement setup is shown in Fig. 9. A Keithley- 4200 Dual Pulse Generator is used to produce G_n, data signal and S_0–S_3, which are set from 9 to –5 V. A pulse/pattern generator (Agilent 81110A) provides a pair of non-overlapping clock signals, POLA, and POLB. To synchronize 81110A and the Keithley4200, a reference clock generated by another function/arbitrary waveform generator (Agilent 33220A 20 MHz) is utilized. A digital oscilloscope DSO6034A is utilized to observe the output waveforms.

The measurement result of a 4-bit digital time-modulation pixel memory is shown in Fig. 9. Figure 10(a) shows the operating voltage waveforms of the signals of S_0, S_1, S_2, and S_3. In order to follow the concept of time modulation, the duty cycle of S_0:S_1:S_2:S_3 is 8:4:2:1. When G_n is on, the data line produces the test pattern "1010" shown in Fig. 9(b). Figure 9(b) shows the measured voltage waveforms of the proposed circuit for G_n, data line, and OUT. The pixel memory circuit can provide the data and corresponding inversion data on the LC node by itself. Since the data line produces "1010" when G_n is on, OUT shows "0101" and "1010" alternatively when G_n is off.

The area impact is one of the most important issues in the proposed circuit. Because the time-modulation technique is utilized in the proposed circuit, the desired gray levels can be displayed by applying a high or low logical voltage on the pixel in different time widths in a fixed time period. Therefore, the pixel does not need to be divided in a binary-weighted manner as is aforementioned in area-coverage modulation,[17] which means the occupied area from complicated routing for each binary-weighted pixel can be further decreased, and the aperture for the LCD panel can be increased in the proposed circuit.

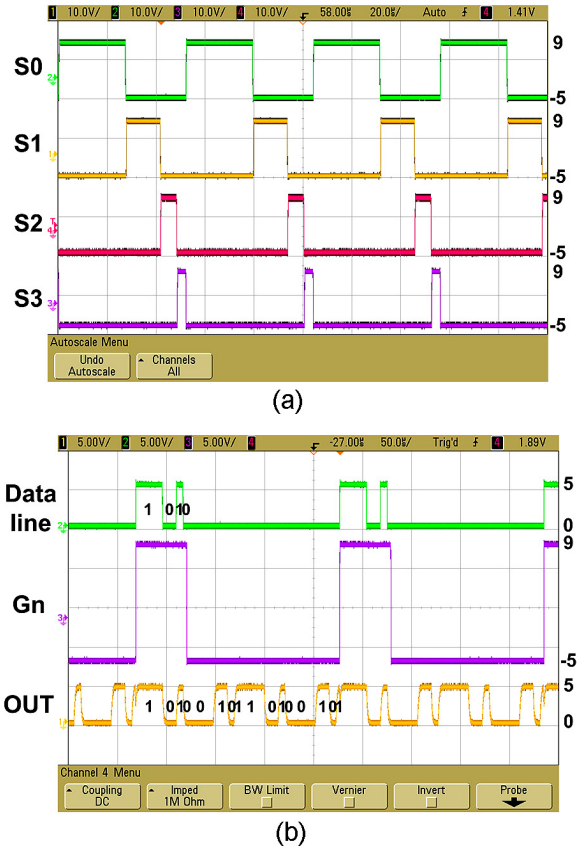

FIGURE 10 — Measured voltage waveforms of the 4-bit time-modulation digital pixel memory with the signal operations at (a) S_0, S_1, S_2, and S_3, and (b) data line, G_n, and OUT. The operating data code demonstrated in this measurement is "1010".

5 Conclusion

A 4-bit digital time-modulation digital pixel memory on glass substrate for panel integration has been successfully designed and fabricated in 3-μm LTPS technology. A time-modulation digital pixel memory was formed with a 4-bit DRAM, latch, and control switches to produce time-modulation data and its corresponding inversion data. This pixel memory circuit can provide frame data and its corresponding inversion data to refresh the static image without an operating data driver circuit, which enables the feature of lower power consumption in the still mode for an LCD panel.

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