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REVIEW

Overview of on-Chip Stimulator Designs for Biomedical Applications

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In recent years, the electrical stimulations have been used for biomedical applications, such as cardiac pacemaker, cochlear implant, muscle exercising, vision restoration, and seizure suppression. Comparing with the traditional treatments by using medicine or surgery, the electrical stimulation was more harmless, flexible, recoverable, and less-destructive. Moreover, with the potential for mass production, CMOS integrated circuits have been designed to implement the electrical stimulators. A comprehensive overview in the field of integrated circuit design for implantable stimulator was presented in this paper. Some basic topologies of output driver designs for implantable stimulators were reviewed. Some advanced techniques based on the reviewed designs to improve the performances were also presented. Since the safety and reliability are the primary concerns when realized the biomedical electronic devices, the on-chip stimulator designs for biomedical applications will continuously be an important design task in advanced CMOS technologies.

KEYWORDS: Electrical Stimulation, Implantable Device, Integrated Circuit, Stimulator.

CONTENTS

INTRODUCTION

As medical science and electronics engineering evolving, bioelectronics combined the microelectronics technology with medicine knowledge results in a new generation of healthcare and therapy. In recent decades, the inseparable relationship between electrical transaction and nervous system has been studied [1]. The electrical stimulation that transmitted artificial electrical signals into nervous system has been verified for innovative medical treatments, including the therapeutic electrical stimulation (TES) and the functional electrical stimulation (FES) [2–4]. The electrical stimulations have been successfully used in a large set of applications, such as cardiac pacemaker, cochlear implant, muscle exercising, vision restoration, and seizure suppression. Comparing with the traditional treatments by using medicine or surgery, the electrical stimulation is more harmless, flexible, recoverable, and less-destructive [5, 6].

Figure 1 shows a general block diagram for the stimulator. In this case, it consists of a power supply, a digital-to-analog converter (DAC), and an output driver. The DAC can achieve good control of the stimulus current amplitude, depending on the number of bits of the DAC.

Safety is the primary consideration in the electrical stimulation [7, 8]. First of the safety issue is the instantaneous electrical shock due to the high charge injection within short time period. Second of the safety issue is the limitation on current injection density. Third of the safety issue is the continuous charge accumulation from the imbalanced biphasic stimulation. Generally, the rectified power for the stimulation is constrained, so the instantaneous electrical shock is preventable because of limited intensity of the injection current level. The limitation on current injection density and the charge accumulation issue should be considered during circuit design to prevent

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from the electrolysis with electrode dissolution and tissue destruction.

IMPEDANCE OF ELECTRODE AND TISSUE

In Figure 2, the equivalent circuit model of the electrode and tissue is described [9, 10]. The spreading resistance (R_s) represents the combination of the tissue, the electrode conductor, and the electrode-wire contact. The electrode-tissue interface capacitance (C_i) represents the capacitance of the double layer interface, and the electrode-tissue interface resistance (R_i) represents the Faradaic resistance which conducts reduction and oxidation currents in electrochemical equilibrium. For the implantable stimulations, the R_s is usually in the order of 1 kΩ∼100 kΩ, the C_i is usually in the order of 10 nF∼1000 nF, and the R_i is usually higher than 1 MΩ [11].

MONOPOLAR AND BIPOLAR STIMULATORS

Some fundamental biophysical analyses of excitable membrane properties have used monophasic stimulation in order to simplify interpretation of the results [12, 13]. However, the monophasic stimulation can be safely used only during short pulses and at low intensities [14]. Using the biphasic stimulation could avoid charge accumulation in tissues. Figure 3 compares the stimulus current (I_{stim}) waveforms of the monophasic and biphasic stimulation.

The biphasic stimulation can be arranged with different positive and negative current, as shown in Figure 4 [15, 16]. The $+I_1$ and $-I_2$ denote the amplitude of positive and negative current, respectively, and the t_1 and t_2 denote the duration of positive and negative current, respectively. As shown in Figure 4(a), the smaller I_2 with longer duration follows the larger I_1. On the contrary, Figure 4(b)

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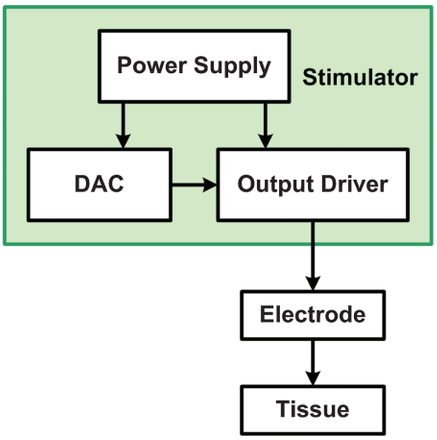

Fig. 1. Block diagram of electrical stimulator.

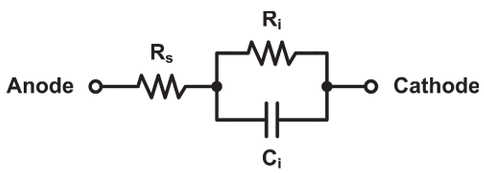

Fig. 2. Equivalent circuit model of electrode and tissue.

shows the smaller I_1 with larger I_2. Once $I_1 \times t_1 - I_2 \times t_2 = 0$, the charge can be balanced without accumulation. With the lower amplitude of positive or negative current, the advantages may include the smooth transition and minimizing charge buildup and spiking. Besides, the circuit design of stimulator may be simplified, since the high current/voltage part can be reduced. If the negative high voltage is needed in the integrated circuits, the challenges include the substrate leakage and reliability issues [17].

To realize the biphasic stimulation, the commonly used configurations of monopolar and bipolar stimulators are shown in Figures 5 and 6 [11, 18]. In Figure 5, the monopolar stimulator utilizes the dual supply voltages (V_{DD} and V_{SS}) with anodic and cathodic output drivers to deliver anodic and cathodic stimulus currents. In Figure 6, the bipolar stimulator utilizes the single supply voltage (V_{DD}) with single output driver from V_{DD} or ground. The anodic and cathodic stimulus currents of the bipolar stimulator are generated by reversing the current paths using switches. The monopolar stimulation is preferred over a bipolar counterpart if the current is intended to spread over

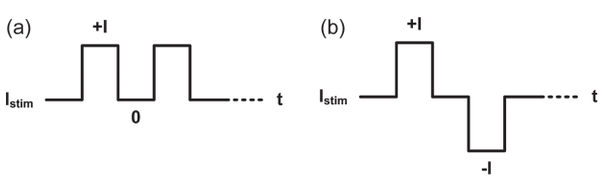

Fig. 3. Current waveforms of (a) monophasic stimulation and (b) biphasic stimulation.

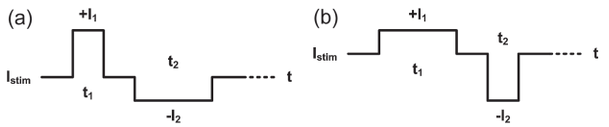

Fig. 4. Current waveforms of different biphasic, charge-balanced stimulation.

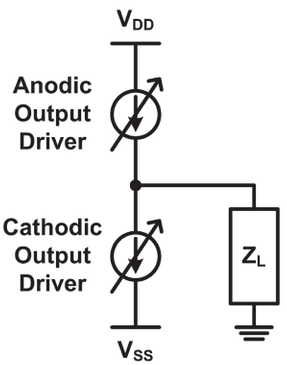

Fig. 5. Monopolar configuration with anodic and cathodic output drivers for biphasic stimulation.

a wider area, and the monopolar stimulation is usually more efficient than the bipolar stimulation [19]. On the other hand, in the simultaneous stimulation using electrode arrays, the bipolar stimulation is preferred to monopolar stimulation, as the former can reduce crosstalk among neighboring sites [20].

BASIC TOPOLOGIES OF OUTPUT DRIVER DESIGNS

Several output driver designs for implantable stimulators have been reported in the literature. The output currents vary from several μA to several mA, depending on the application. The design considerations of the output driver for on-chip stimulator include high output impedance, good linearity, low power consumption, and small silicon

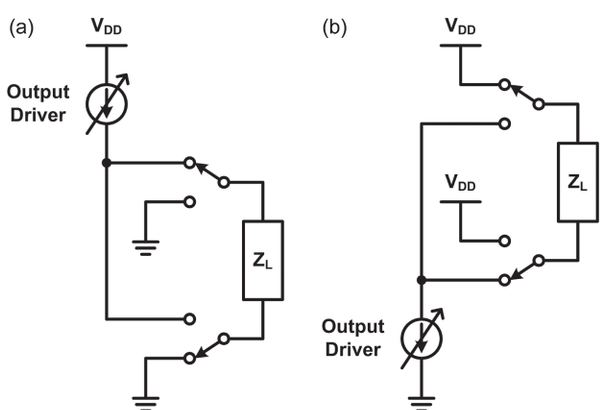

Fig. 6. Bipolar configuration with output driver of (a) current source and (b) current sink, for biphasic stimulation.

area. Some output driver designs for on-chip stimulator are reviewed in following sections. These output drivers are shown with p type to perform a current source. Besides, they can be used with *n* type to perform a current sink.

Current-Mode DAC

A current-mode DAC can be used to output the stimulus current, as shown in Figure 7 [21–26]. The current-mode DAC is usually composed of binary-weighted transistors which gates are connected to a common bias voltage. It is also possible to employ identical transistors with binary-weighted bias voltages.

In Ref. [21], the bidirectional DAC enabled by the binary coded amplitude is reported. The DAC output range can be scaled by the controllable aspect ratio of the mirrors' inputs. This design presents both high output impedance and large output voltage compliance.

In Refs. [22] and [23], the stimulator consists of the complementary DAC to perform the biphasic stimulation. Each current source consists of several pairs of serially connected MOS current regulators and MOS injection switches. The stimulus current can be controlled by the current regulators to be different current values. In Ref. [24], additional pair of polarity switches is added to select the positive or negative DAC output to achieve monopolar biphasic stimulation.

To maintain the stability and linearity of the stimulus current, the thermometer code scheme with small glitch error is employed in the DAC design in Ref. [25]. In this design, the stimulus current of DAC can be varied in 256 different levels ranging from 0 to 1 mA.

In Ref. [26], the stimulator is based on a 4-bit binary-weighted DAC. The biases for the current source and cascode transistors in DAC are provided by a wide-swing cascade bias circuit such that the required supply-voltage overhead is minimized. The cascode transistors also improve the output impedance and linearity of control.

Current-Mode DAC with Current Mirror

The current-mode DAC with a current mirror is another way to duplicate the source current to the stimulus current,

Fig. 7. Output driver implemented by current-mode DAC.

as shown in Figure 8 [27–30]. This design works properly as long as all transistors are kept in the saturation region. The output impedance of the DAC with current mirror can be higher than that of the stand-alone DAC, which is better for biomedical microstimulation applications. However, both source current and stimulus current consume power from the supply.

In Ref. [27], the stimulus current is mirrored from the DAC through an operational amplifier, while in Refs. [28] and [29], the output driver consists of a current source, bias circuit, and current mirror to constantly deliver the stimulus current. The output driver in Ref. [30] further consists of an exponential current mirror to produce the flexible exponential stimulus current.

To perform the better output impedance, the DAC with a fully cascode current mirror has been reported, as shown in Figure 9 [31, 32]. The fully cascode current mirror increases the output resistance by a factor of $g_m r_o$, where g_m and r_o are the transconductance and output resistance of a transistor, respectively.

The designs using current steering DAC with the fully cascode current mirror have been reported in Refs. [31]

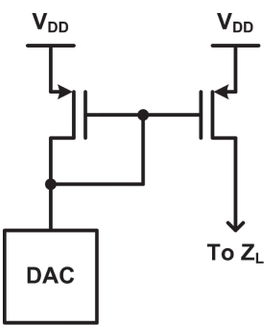

Fig. 8. Output driver implemented by current-mode DAC with current mirror.

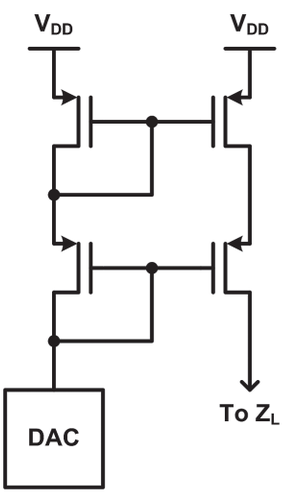

Fig. 9. Output driver implemented by current-mode DAC with fully cascode current mirror.

and [32]. The supply voltages of these circuits are usually higher, and the transistors are high-voltage transistors to allow sufficiently high compliance. Some low-voltage transistors can be used with high-voltage transistors to reduce mismatch of current gain and save some chip area.

The DAC with a wide swing cascode current mirror is shown in Figure 10 [33, 34]. In this design, the required supply-voltage overhead can be minimized. In other words, the wide-swing cascode current mirror is used to achieve maximum stimulus current per supply voltage while maintaining transistors operating in the saturation region. This method reduces the power consumed by the headroom. In Ref. [33], the minimum allowable headroom for the output driver with wide-swing cascode current mirror decreases to about 1 V, while that with the conventional current mirror is about 2.5 V. However, the output driver with wide-swing cascode current mirror requires more chip area due to the routing overhead of the additional bias potentials.

The output driver consists of an output cascode transistor and current mirror assisted with the DAC is shown in Figure 11 [16]. The additional output cascode transistor can be further designed as electrostatic discharge (ESD) protection device. By connecting the body terminals of PMOS and NMOS to the power supply rails, the ESD protection can be achieved by using the parasitic drain-body diodes of transistors.

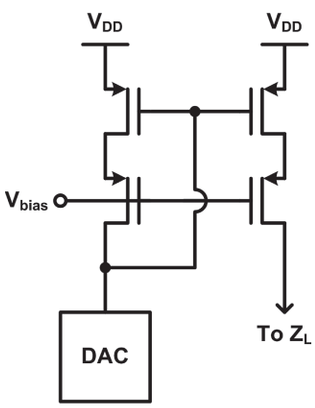

Fig. 10. Output driver implemented by current-mode DAC with wide-swing cascode current mirror.

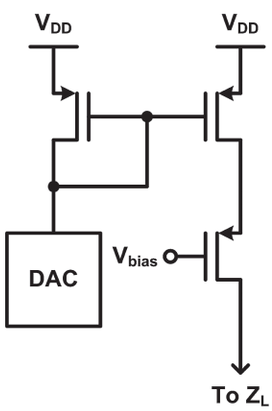

Fig. 11. Output driver implemented by current-mode DAC with output cascode transistor and current mirror.

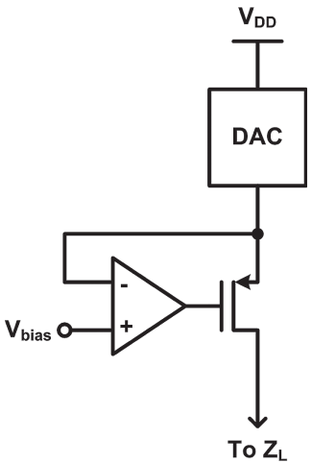

Fig. 12. Output driver implemented by DAC with voltage-controlled resistor.

DAC with Voltage-Controlled Resistor

A stimulator based on the DAC and a voltage-controlled resistor has been presented, as shown in Figure 12 [35]. It is used to increase the output impedance by biasing the transistor with active feedback. The DAC delivers the stimulus current to Z_L through the voltage-controlled resistor. The voltage-controlled resistor is implemented by a MOS transistor with an operating amplifier. When the V_{bias} is small, the transistor of voltage-controlled resistor operates in deep triode region and represents a linear resistor between the drain-source terminals. With the implementation of DAC with voltage-controlled resistor, the DAC output is used to bias the transistor to generate the stimulus current. This configuration yields the output driver with small voltage compliance.

Another current-mode DAC with the current mirror and additional voltage-controlled resistor has been reported, as shown in Figure 13 [36, 37]. The voltage-controlled resistor is implemented by a MOS transistor with the active-feedback operating amplifier. The operating amplifier locks the drain voltages of two transistors used in current mirror, which makes the stimulus current proportional to the source current. The output impedance of this design is much higher than that of the current mirror only. The active feedback current mirror also minimizes the voltage headroom requirement for the current mirror. As reported in Ref. [36], the output voltage is 6 V and the supply voltage is 6.5 V.

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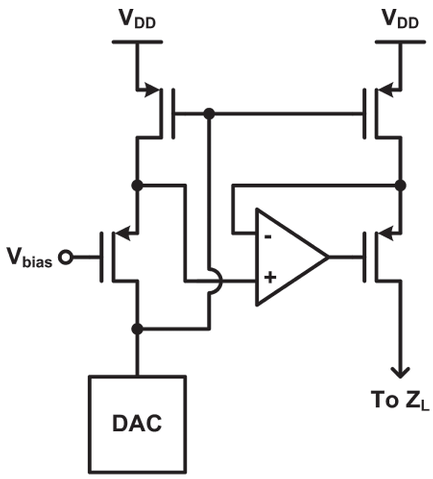

Fig. 13. Output driver implemented by DAC with current mirror and voltage-controlled resistor.

Voltage-Mode DAC with Voltage Follower

The stimulator by using a voltage-mode DAC with voltage follower to bias a fixed resistor is shown in Figure 14. The voltage-follower is implemented by a negative feedback operating amplifier and MOS transistor. The input of the voltage follower is controlled by the DAC, which is also the bias voltage across the resistor. The stimulus current is V_{DAC}/R, where V_{DAC} is the output voltage of DAC and R is the resistance. The stimulus current can be controlled by changing the DAC output voltage. Once the DAC output voltage has been chosen, the voltage across the resistor is kept constant by a negative feedback. If the gain of operating amplifier and the size of transistor are large enough, the voltage compliance of this circuit can be very high.

A similar method using a voltage-mode DAC with voltage follower to bias an active load is shown in Figure 15 [32]. It is the best choice for implementing the load resistance in CMOS technology by using a MOS transistor biased in deep triode region. The active load of MOS transistor is controlled by a bias voltage. By changing the bias voltage within a fixed range, this circuit can obtain small changes on the resistance of the active load.

Voltage-Mode-DAC-Controlled Resistor with Voltage Follower

As shown in Section 4.4, controlling the output driver by changing the resistance is another way to generate the stimulus current. A voltage-controlled resistor with a constant bias will also act the output driver, as shown in Figure 16 [38, 39]. Controlled by the DAC output, the voltage-controlled resistor is implemented by a MOS transistor in the triode region. As long as the MOS transistor is kept in the triode region, the stimulus current in this circuit will be proportional to the DAC output voltage. This

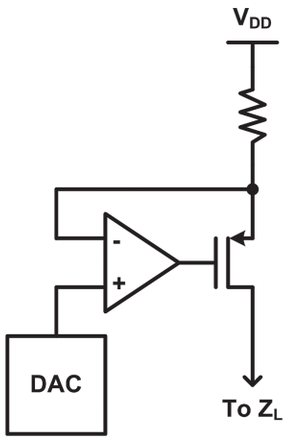

Fig. 14. Output driver implemented by voltage-mode DAC with voltage follower.

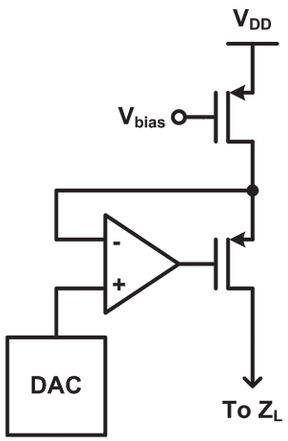

Fig. 15. Output driver implemented by voltage-mode DAC with voltage follower and active load.

configuration yields the output driver with small voltage compliance.

A stimulator based on this topology has been present in Refs. [38] and [39] to support multiple stimulating sites. The voltage-mode-DAC-controlled MOS transistor in deep triode region is used as linearized voltage-controlled resistor. The stimulus current is controlled by the MOS gate voltage, which is digitally programmable by the voltage-mode DAC. In this design, the high output impedance can keep the stimulus current constant.

ADVANCED TECHNIQUES OF OUTPUT DRIVER DESIGNS

The reported output driver designs for implantable stimulators have been reviewed in previous section, which can provide the information for circuit designers to design the suitable stimulator. The different applications have different requirements on stimulus current, output

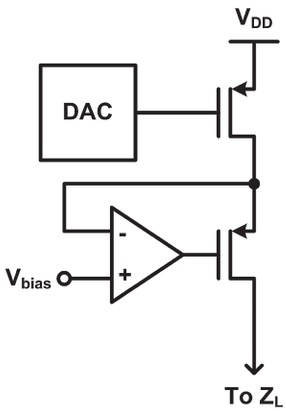

Fig. 16. Output driver implemented by voltage-mode-DAC-controlled resistor with voltage follower.

impedance, power consumption, and other specifications for the designs.

Some advanced techniques based on the reviewed designs have also been reported to improve the performances, such as fail safe, avoiding charge accumulation, low power, and high-voltage tolerance.

Fail-Safe Design with High-Frequency Current-Switching

For safety consideration, the blocking capacitor of output stage in series with the electrode serves the purpose to prevent from prolonged dc current flowing into the tissue in the event of semiconductor failure. The required blocking capacitance can be calculated as $I_{\text{stim}} \times dt/dV$, where I_{stim} denotes the stimulus current, dt denotes the stimulation duration, and dV denotes the variation of voltage across the load. In order to output the stimulus current with the required duration, the size of blocking capacitor would be too large to be integrated into a chip. For example, a stimulation with 30-μA current and 0.5-ms duration on 20-kΩ load, the required blocking capacitance is $\sim$0.2 μF to keep the stimulus current within 10% variation [28]. In order to solve the problem of large-sized blocking capacitor, a technique of high-frequency current-switching has been studied to reduce the size of blocking capacitor, as shown in Figure 17 [35, 40]. For a given stimulus current, the reduction of duration (dt) can also reduce the required size of blocking capacitor. The technique of high-frequency current-switching utilizes two complementary output drivers with blocking capacitors. The complementary stimulus currents (I_{stim1} and I_{stim2}) converge and form a complete stimulus current ($I_{\text{stim}} = I_{\text{stim1}} + I_{\text{stim2}}$). Thus, each stimulation duration is reduced, while the stimulus current and the variation of voltage across the load are not changed. The reduction ratio of blocking capacitor can be designed according to the switching frequency.

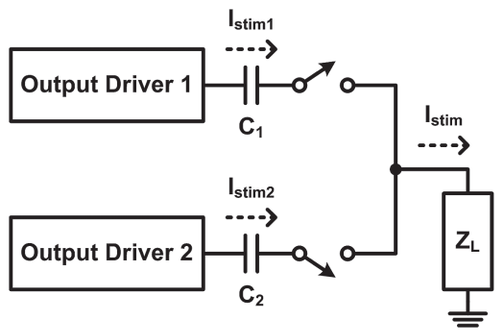

Fig. 17. Stimulator with fail-safe blocking capacitors realized by using high-frequency current-switching technique.

Avoiding Charge Accumulation Without Blocking Capacitor

The charge accumulation caused by the dc leakage current or by the mismatch during biphasic stimulation will result in undesirable effects to the tissue. Besides adding the blocking capacitor to block the dc leakage current, an alternative method for avoiding the charge accumulation in the tissue is to use a charge cancellation switch, as shown in Figure 18 [31]. When the charge cancellation switch turns on, it provides the current path to ground. Therefore, the leakage current or the mismatched charge will be bypassed to ground, and the charge will not accumulate in the tissue.

Low Power

The required operating voltage of output driver is $V_R + V_C$, where V_R denotes the voltage across the resistive load ($I_{\text{stim}} \times R$), and V_C denotes the voltage across the capacitive load ($I_{\text{stim}}/C \times \int dt$). It is obvious that the operating voltage can be adjusted due to the changing voltage across the capacitive load. If the operating voltage of output driver keeps constant during stimulation, some power will be wasted. To eliminate the wasted power, the output driver can be designed whose voltage tracks the back voltage on the electrode, as shown in Figure 19 [29, 41, 42]. This output driver will have virtually no wasted power dissipation. Comparing the constant operating voltage with the adjustable operating voltage, the power consumption of the design with adjustable operating voltage can be reduced.

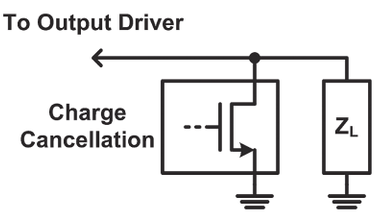

Fig. 18. Stimulator with charge cancellation to avoiding charge accumulation.

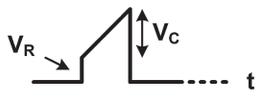

Fig. 19. Stimulator with low power design.

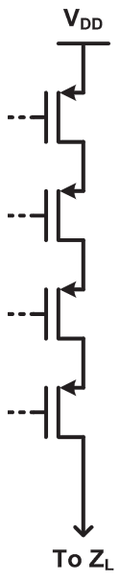

Fig. 20. Stimulator with high-voltage tolerance by using stacked transistors.

High-Voltage Tolerance

With the potential for mass production, low-voltage CMOS technologies have been used to implement the integrated circuits for biomedical applications. The gate-oxide thickness of MOS transistor has been shrunk to improve circuit performance and operating speed in advanced CMOS technologies. In addition, the power supply voltage in CMOS integrated circuits has also been scaled down to follow the constant-field scaling requirement and to reduce power consumption. However, the stimulator with low-voltages devices must deliver the stimulus current with high voltage across the load. The high-voltage-tolerant output driver must be designed in low-voltage CMOS technologies to prevent from the reliability issues, such as electrical overstress on gate oxide.

The stacked MOS configuration has been reported to allow high voltage across the output driver, as shown in Figure 20 [36, 43]. For example, the design with four 1.8-V transistors can safely operate up to 7.2 V. The high-voltage-tolerant design can be further integrated for an electronic prosthetic system-on-chip (SoC).

CONCLUSION

A comprehensive overview in the field of integrated circuit design for implantable stimulator is presented. The power supply, DAC, and output driver are generally used to construct the electrical stimulators. Some basic topologies of output driver designs have been presented. Besides, some advanced techniques of output driver designs have also been presented to improve the performances. Since the safety and reliability are the primary concerns when realized the biomedical electronic devices, the on-chip stimulator designs for biomedical applications will continuously be an important design task in advanced CMOS technologies.

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