PAPER

An Ultra-Low Voltage CMOS Voltage Controlled Oscillator with Process and Temperature Compensation

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SUMMARY Process and temperature variations have become a serious concern for ultra-low voltage (ULV) technology. The clock generator is the essential component for the ULV very-large-scale integration (VLSI). MOSFETs that are operated in the sub-threshold region are widely applied for ULV technology. However, MOSFETs at subthreshold region have relatively high variations with process and temperature. In this paper, process and temperature variations on the clock generators have been studied. This paper presents an ultra-low voltage 2.4GHz CMOS voltage controlled oscillator with temperature and process compensation. A new all-digital auto compensated mechanism to reduce process and temperature variation without any laser trimming is proposed. With the compensated circuit, the VCO frequency-drift is 16.6 times the improvements of the uncompensated one as temperature changes. Furthermore, it also provides low jitter performance.

key words: *ultra-low voltage (ULV), subthreshold region, voltage-controlled oscillator, temperature and process variation*

1. Introduction

With the explosive growth of portable devices and biotechnology, wireless has become one of the most important design criteria in digital, analogy, and radio frequency (RF) circuits [1]. The clock generator is an essential component for such applications. However, power consumption and frequency drifts are the key factors to be overcome in the clock generator. The crystal oscillators (XOs) had been widely applied for most conditions. XOs provide a precise reference clock to PLLs or DLLs for high-speed applications. However, the crystal (XTAL) is an off-chip component with high power consumption [2]–[4].

Process, voltage and temperature (PVT) variations are the critical factors of frequency drifts for clock generators. Typically, PVT compensations include material and electronic compensations [5]. Material compensation applies a substance with a positive temperature coefficient of frequency (TCF) in the resonator such as SiO_2 to neutralize the effect of negative TCF of the silicon resonator [6], [7]. Electronic compensations include off-chip and on-chip calibrations. Both above methods mostly combine proportional to absolute temperature (PTAT) circuit and the complementary to absolute temperature (CTAT) circuit to compensate temperature variations. Off chip calibrations compensate the variation by off-chip circuits or external control signals [8], [9]. On-chip compensation, also known as auto calibrations, integrate sensors and compensated circuits and could be all accomplished in the chip [10]–[13]. Since the additional testing procedure and off-chip circuitry are reduced, low cost will then become another advantage in on-chip compensation. Nowadays, on-chip compensation has been widely implemented with increasing precision.

The industrial, scientific, and medical (ISM) band of 2.4 GHz is reserved internationally for the use of RF energy for industrial, scientific and medical purposes [14], [15]. Wireless body-area networks (WBAN) which are rapidly growing applications, and are used for communication among sensor nodes operating in, on or, around the human body [16], [17]. The human body communication (HBC) is a wireless communication method used to connect devices through the human body as a transmission media. HBC has high speed and low power characteristics and is suitable for contact-based services [18], [19]. Hence, the clock generator operating at 2.4GHz is the critical and essential component for healthcare purposes.

In this work, an ultra-low-voltage 2.4 GHz crystal-less clock generator with an auto-calibrated process and temperature circuit is proposed. The auto-calibrated process and temperature compensated circuit includes a process detector to detect process variation and all digital compensation circuit. Besides, a temperature voltage controlled compensated circuit is applied to calibrate the variation from temperature.

The proposed circuit was fabricated in a 65 nm CMOS technology. It makes the operation of CLCG with very low supply voltages, down to 0.5 V, as well as achieves sufficient high frequency stability and accuracy against the variations from process and temperature.

2. Architecture and Circuit Implementation

2.1 Architecture of Proposed CLCG

Figure 1 shows the structure of the proposed ultra-low-voltage (ULV) CLCG. It includes the LC oscillator, auto-calibrated process and temperature circuit, and digital controlled varactors and temperature compensation circuit.

The LC voltage-controlled oscillator (LC VCO) is shown in Fig. 2. By utilizing the capacitive feedback and

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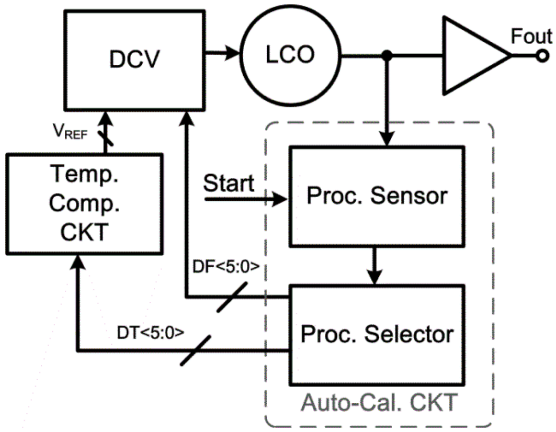


Fig. 1 Block diagram of the proposed CLCG.

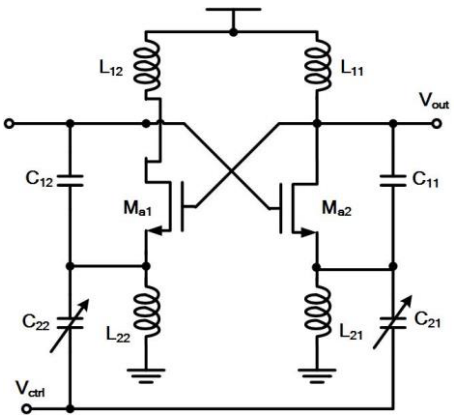


Fig. 2 Schematic of the voltage-controlled LC oscillator.

the forward-body- bias (FBB) technique [20], the LC VCO can be operated with reduced supply voltage and power consumption while maintaining remarkable circuit performance in terms of phase noise, tuning range, and output swing. As $C_{11} = C_{12} = C_1, C_{21} = C_{22} = C_2, L_{11} = L_{12} = L_1$ and $L_{21} = L_{22} = L_2$, the oscillation frequency and transconductance can be approximated by

$$\omega_0 \approx \sqrt{\frac{1}{L_2C_2} + \frac{C_1 + C_2}{L_1C_1C_2}} \tag{1}$$

As $L_1 = L_2 = L_P$, the Eq. (1) can be simplified as

$$\omega_0 \approx \sqrt{\frac{1}{L_p}\left(\frac{1}{C_1} + \frac{2}{C_2}\right)} \tag{2}$$

From (2), it is clear that the variation of C_2 has more influence on ω than C_1. Therefore, the capacitor C_2 is applied as tuning varactors to a reasonable tuning range of the LC VCO under ultra-low-voltage operations. Besides, increasing the capacitance of C_1 can get wider tuning range. Therefore, C_1 are implanted with metal-insulator-metal (MIM) capacitors, which have high capacitance and better stability.

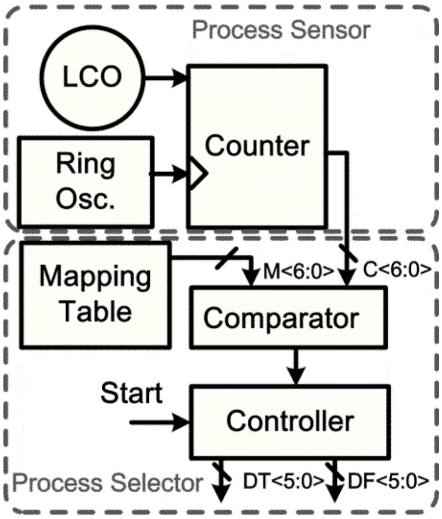


Fig. 3 The block diagram of auto-calibrated compensated circuit.

2.2 Auto-Calibrated Process and Temperature Circuit

Figure 3 shows the block diagram of an auto-calibrated process and temperature compensated circuit. It consists of a process detector and a digital process and temperature compensated circuit. The ring oscillator, a LC VCO, and a counter consist of the process sensor.

The signals of a LC VCO and a ring oscillator are taken as the input and clock of counter, respectively. The output digital codes of the counter (C<6:0>) are dependent on the process variation. The mapping table is based on the process and temperature variations in the mapping table detection (MTD) [21]. Three process corners which are slow-slow (SS), typical-typical (TT), and fast-fast (FF) with 5% V_{DD} variation are considered. The output digital signal of mapping table (M<6:0>) is the calibration parameter that depends on the process variation and used to adjust the target frequency DCO.

Figure 4(a) shows the simulated frequency versus temperature for the proposed LC VCO without any calibration. Temperature coefficient (TC) are 705, 550, and 534 ppm/°C of the slow-slow (SS), typical-typical (TT), and fast-fast (FF) corners, respectively. The LC VCO frequency differences of corners are too slight (about 50MHz) to be distinguished. Then, a low speed ring oscillator operated at 60MHz with TT corner is introduced to sense the process variation.

Figure 4(b) shows the simulated frequency versus temperature for the ring oscillator with different corners. TC of ring oscillators are 25500, 16000, and 10200 ppm/°C of the SS, TT, and FF corners, respectively. The highly process, voltage, and temperature (PVT) dependent characteristic of a ring oscillator can be used to detect the PVT variations efficiently.

Figure 5(a) shows the flow charts of mapping table selection. The mapping table selection mechanism can be the-

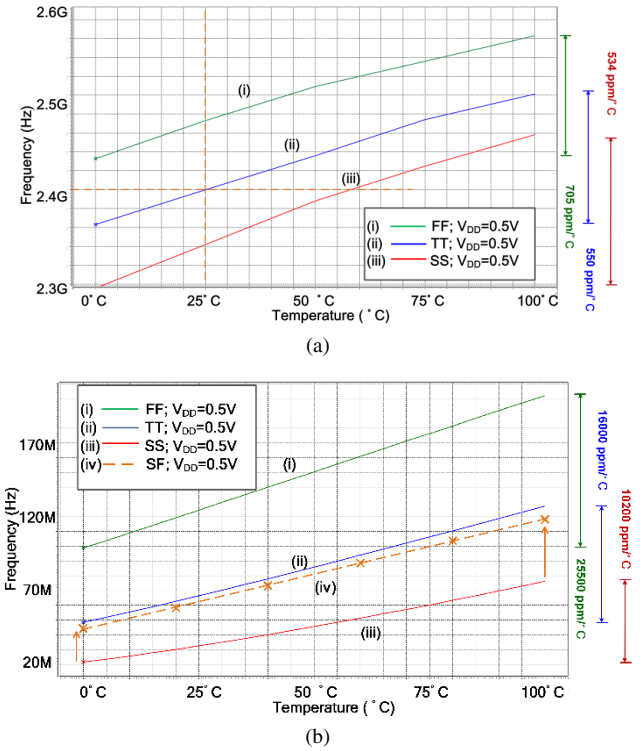


Fig. 4 (a) Simulated result of frequency versus temperature for the LC VCO without any calibration. (b) Simulated result of frequency versus temperature for the ring oscillator without any calibration.

oretically considered as the sequence of four operations:

1. Initialization: The calibration must be operated at initial temperature (30°C) to avoid temperature variations. As Start goes high, outputs of the registers must be set or reset. The counter outputs C<6:0> are decided by the frequency of the ring oscillator and LC oscillator, and then the counter output C<6:0> saves to the register LCCNT.
2. Mapping table selection: When the initialization is completed, the mapping table value M<6:0> according to its mapping address MAPADR saves to the register MAPDATA. If MAPDATA > LCCNT, the corresponding M<6:0> can be found. Otherwise, it increases the MAPADR value and compares the MAPDATA and LCCNT again until finds out the applicable M<6:0>.
3. After completing mapping table detection, the controller gets the matching M<6:0>. The mapping table value M<6:0> and its corresponding process code DF<5:0> and temperature code DT<5:0> are shown in Fig. 5(b) Thus, the corresponding DF<5:0> and DT <5:0> of this chip can be defined. Then, the controller uses the mapping value to achieve the target frequency by switching varactors for temperature and process compensation.
4. One-point calibration: At the fine tuning stage, single point calibration is applied to modify the output frequency at room temperature. The mechanism maintains that the function of the calibration system can

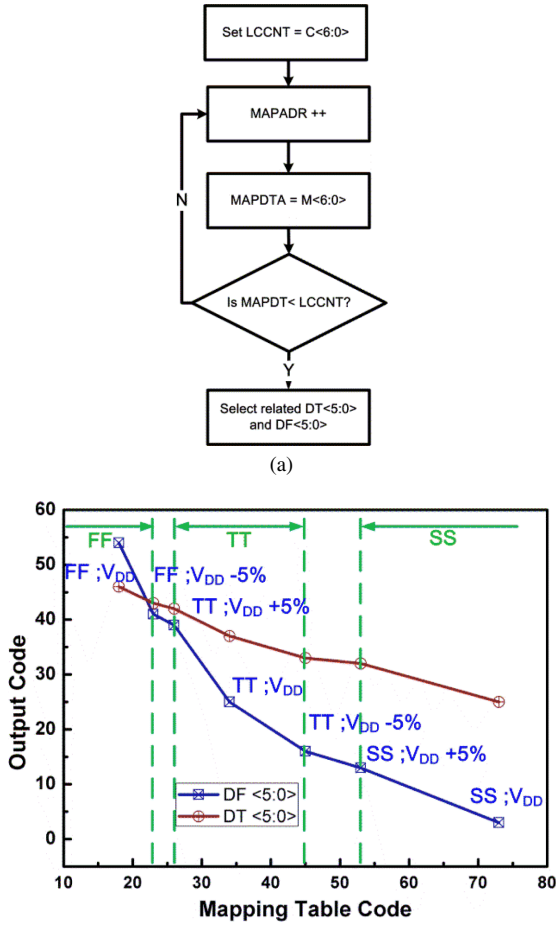


Fig. 5 (a) Flow charts of mapping table selection for the proposed mechanism of auto calibrated process and temperature circuit. (b) Relationship between mapping table code and output code.

work under the operational frequency of the CLCG.

The frequency resolution of DF<5:0> is $\frac{\text{Tuning Range}}{\text{N}} = \frac{192\text{MHz}}{64} = 3\text{MHz}$. The frequency tuning step is 12.5 ppm/°C where is sufficient for this condition. The frequency resolution of DT<5:0> is also 3MHz. The resolution depends on the frequency of a LC VCO and a ring oscillator. The resolution increases with high speed of a LC VCO and low speed of a ring oscillator. The mapping table selection is cover by SS, TT, FF corners. However, if the ring oscillator speed is higher than above situations and the LC-VCO speed is kept at relative low speed, such as slow-fast (SF) corner. The counter output code might be out of range. Therefore, the design should be increased the compensated range to overcome this situation.

2.3 Architecture of Digital Controlled Varactors

Figure 6(a) illustrates the circuit of the DCV (Digital controlled varactors). Figure 6(b) shows the capacitor value of DCV versus its controlled voltage with different devices. DCV should produce a smaller capacitor value to maintain

a higher operating frequency of DCO. The complementary signal of F<0> is applied to NMOS source/drain of DCV to produce two quantized levels of capacitor values. Besides, the source/drain- to-bulk junctions are forward biased at 0.5 V. Accordingly, DCV has two different timing resolutions and provides the same output loading for DCO. In Fig. 6(b), (i) and (iv) produced by Low Vth (LVT) MOSFET has wider tuning range of the capacitor than (ii) and (iv) produced by Low Vth (LVT) MOSFET. Therefore, DCV can be realized for a wide tuning range and high-speed frequency by selecting LVT MOSFETs in the proposed circuit.

2.4 Architecture of Temperature Compensated Circuit

The temperature coefficient of the LC VCO is proportional to absolute temperature (PTAT), as can be seen in Fig. 4(a). Therefore, the complementary to absolute temperature (CTAT) frequency has been applied to compensate the temperature variation. As temperature increases, the frequency should be decreased by increasing the capacitance of DCV. Hence, the V_{out} is the PTAT voltage to accomplish the temperature compensation.

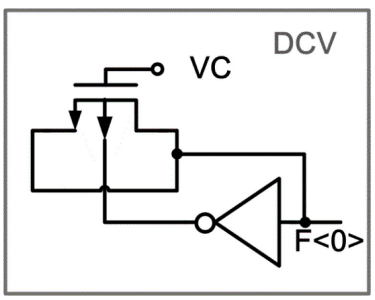
Figure 7 shows the temperature compensation circuit (TCC). The current reference provides a stable PTAT voltage reference, V_{out} [22], [23]. The temperature compensated mechanism relies on switching DCV.

The current reference provides a stable current, which compensates for temperature effects on V_{out}, and voltage variations can be reduced the supply voltage by an OP Amp. Transistor M2 is the native NMOS, and others are operated in the subthreshold region. The gate of M1 and M2 are also connected to the gate of M6 and M7, its purpose is to keep M1 and M2 always on by the diode connected transistor M8. The reference output voltage V_{out} can be approximately expressed as

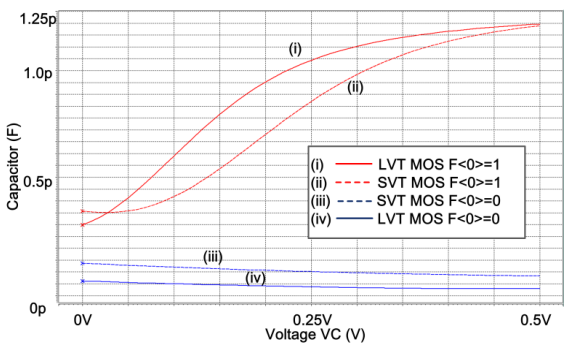
$$V_{out} = V_{GS1} - V_{GS2} = V_{th1} - V_{th2} - \frac{\Delta V_{th}}{BV_T} + \eta V_T \ln\left(\frac{A\beta}{\mu S_1 V_T^2}\right) \quad (3)$$

where $S = \left(\frac{W}{L}\right) C_{OX}(\eta - 1)$. (W/L is the transistor aspect ratio, C_{OX} is the gate oxide capacitance per unit area, and η is the subthreshold slope factor). $V_T = K_B T/q$ is the thermal voltage (K_B, is the Boltzmann constant, q the elementary charge, and T is the absolute temperature). V_{th} is the MOSFET threshold voltage. Assume the ratio of mirror $(I_{out}/I_1 = (W_5/L_5)/(W_3/L_3))$ is β. $A = (S_7 S_8/a^2 S_6)$ and $B = (\eta_7 + \eta_8 - \eta_6)$. The temperature dependence of the reference voltage, V_{out}, is firmly related to the thermal behaviour of V_T and V_{th}. The temperature reference circuit can be design by setting $\delta V_{REF}/\delta + T > 0$ to achieve PTAT circuit.

As turns on the switch (DT<0> = 0), MS turns off and V_{out} is equal to F<0> = 1 of DCV. On the contrary, MS turns on and V_{out} is equal to F<0> = 0 of DCV when turns off the switch (DT<0> = 1). There are three sets of active load, MS, and DCVs for three corners (SS, TT, and FF) in



(a)



(b)

Fig. 6 (a) Schematic of digital controlled varactors for frequency calibration. (b) Capacitor value of DCV versus its controlled voltage.

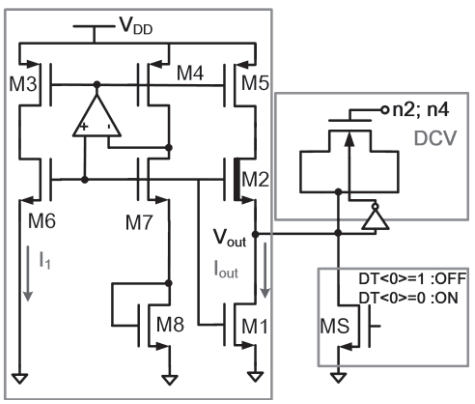


Fig. 7 Schematic of temperature compensation circuit.

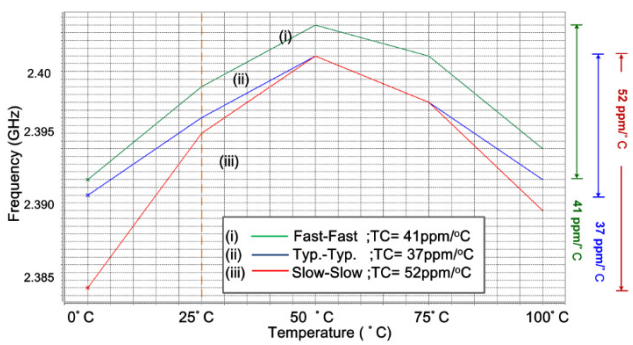


Fig. 8 Simulation Results of frequency versus temperature for the proposed CLCG after calibration.

this design. After the auto-calibration circuit selects the corners, the code of DT<5:0> is decided. Figure 8 shows the simulated frequency versus temperature for the proposed LC VCO after calibration. The TC of the SS, TT, and FF are 52, 37, and 41 ppm/°C, respectively.

3. Experimental Results

The proposed frequency generator has been fabricated in a 65nm GP (general purpose) CMOS process without specialized analogy process options. The die photograph is shown in Fig. 9. The core dimension which includes inductors is 660μm x 1040μm. The output buffer includes tap buffers and an open drain circuit. Figure 10 shows the measurement setup with bias tee for output signal. F_{ct}<5:0> is a 6-bit manual frequency controlled code for one-point calibration. Temperature measurements were performed in a programmable thermal chamber. The MOSFETs of high frequency devices such as varactors and the –gm part (M_{a1} and M_{a2} in Fig. 2) of LCO are applied deep n-well devices. Deep n-well structure is used to block substrate noise. The devices are also applied double guard rings to isolate each body. Therefore, the LVT devices have isolated body but not sharing the same substrate with other NMOS devices by deep n-well and guard ring structure. The layout view are shown in Fig. 11.

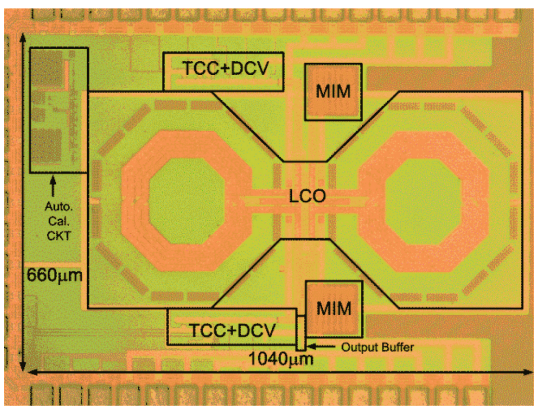


Fig. 9 Die photograph of the proposed circuit fabricated in a65-nm CMOS process.

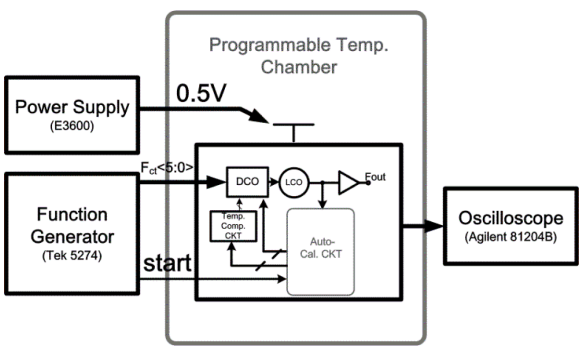


Fig. 10 Measurement setup.

3.1 Temperature Compensation

Frequency drift over temperature and power supply voltage was measured with the real-time oscilloscope (Agilent 81204B). Measured results with temperature compensation are shown in Fig. 12(a). After auto-calibration mechanism,

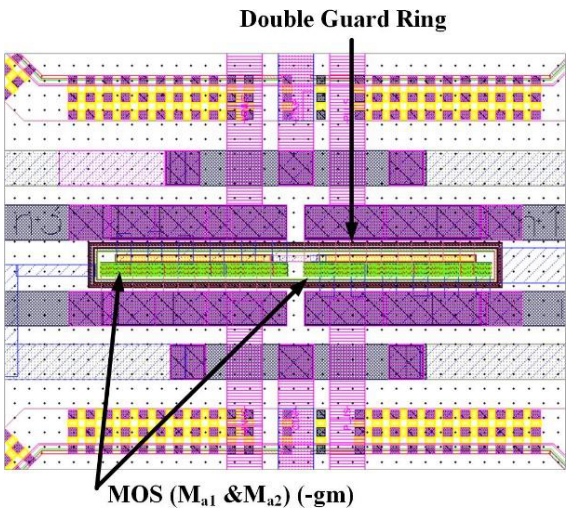
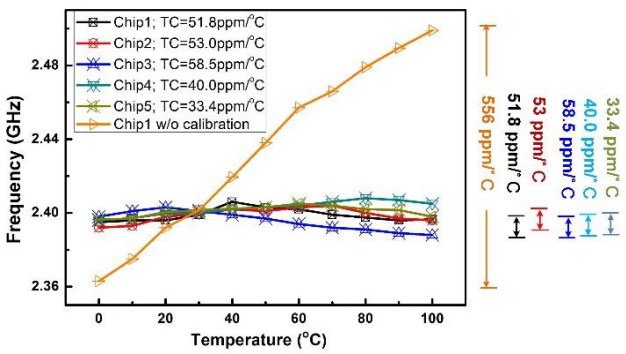
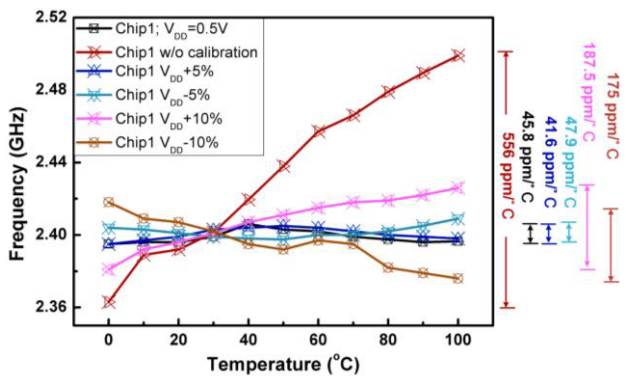


Fig. 11 Layout view of –gm.



(a)



(b)

Fig. 12 (a) Measured results of frequency versus temperature of the tested dies after temperature and process calibration. (b) Measured results of frequency versus temperature with the supply voltage variation.

one-point calibration which calibrates the initial frequency to 2.4 GHz at 30°C has been applied. The total measured temperature coefficient is 33.4 to 58.5 ppm/°C in the external 0.5-V unregulated power supply and over a temperature range of 0 to 100°C. The temperature variation of 5 chips is less than 0.5%. The worst case (Chip 3) is slightly overcompensated. The bits of digital temperature code DT<5:0> is insufficient to set a response with a less positive coefficient, though to add that functionality into future revisions is necessary.

The TC without auto-calibration is 556 ppm/°C. The result is similar to the simulation of TT corner. Therefore, frequency-drift of the VCO with the compensated circuit is 16.6 times of the original one without compensation. Figure 12(b) shows the measured results of TC with supply voltage variation. TC of V_{DD} +5%, −5%, +10%, −10% is 41.6 ppm/°C, 47.9 ppm/°C, 187 ppm/°C, and 175 ppm/°C separately. We can see that the temperature compensation of +/−10% is not enough to compensate the frequency. Because the mapping table only has with 5% variation in order to keep 1-to-1 mapping. On the contrary, TC of V_{DD} +5% is close to the V_{DD} = 0.5V. It means that the compensation mechanism is work at the condition of V_{DD} +5%.

3.2 Jitter Performance

Figure 13 represents the operating frequencies at 25°C and the jitter histogram at 0.5 V, which demonstrates a 1.45-ps RMS jitter and a 10.47-ps peak-to-peak jitter (P2P jitter) at 2.4 GHz within 12.95k hits. The RMS and P2P period jitters are less than 0.35% and 2.53%, respectively. The voltage amplitude is 0.78V where bias tee voltage is 1.2V at V_{DD} = 0.5V. The total power consumption is 2.5mW at V_{DD} = 0.5V.

Table 1 summarizes the results of this work and compares with previous temperature compensated clock generators. Comparing to other on-chip works, such as AD-PLL, DLL and RC oscillator, the proposed ULV CLCG exhibits the lowest temperature sensitivity and comparable low jitter performance. The oscillators of MEMS and FBAR have lower TC and better phase noise than others structures. However, the MEMS oscillator needs additional MEMS mask process, and FBAR resonator has to fabricate with BiCMOS process. In addition, above MEMS or FBAR

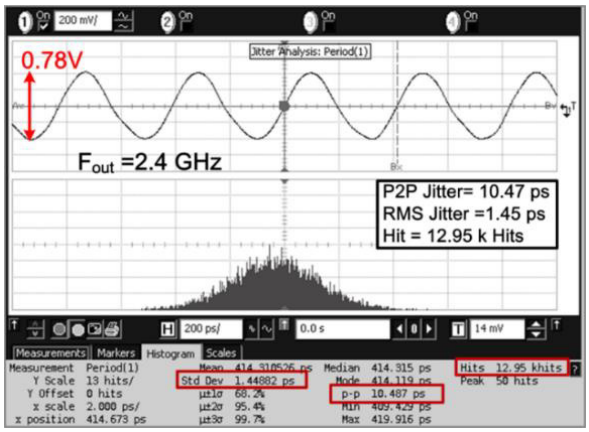


Fig. 13 Jitter performances where RMS = 1.45ps and P2P = 10.47ps of 2.4GHz output at V_{DD} = 0.5V.

Table 1 Performance comparisons of clock generators

Parameter	JSSC'12 [5]	IUS'06 [7]	TCASII'14 [8]	JSSC'13 [9]	TCASII'14 [11]	ISSCC'14 [12]	JSSC'16 [13]	ASSCC'12 [21]	This work
Temp. Comp. Method	Material+ Off Chip	Material	Material	Off Chip	On Chip	On Chip	On Chip	On Chip	On chip
Technology (nm)	180*	Bi-CMOS	130	350	180	40	65	65	65
Supply voltage (V)	2.5	2.7	1.8	2.5	1.8	1.1	1.2	0.3	0.5
Frequency (MHz)	427	2000	1.2	52	1.1	2418	1200~ 2000	12	2400
Power (mW)	13	4.05	0.0058	14.25	0.00086	6.4	3.6	0.005	2.5
TC(ppm/°C)	0.805	5	296	0.02	64.3	166	6.9	<860	33.4
Jitter (ps) (RMS)	N/A	N/A	33n	3.2	N/A	3.29 N/A	0.44	0.294ns 287ps	1.45 10.47
Phase Noise (dBc/Hz)	-145 @1MHz	-138 @1MHz	N/A	-142 @1MHz	-74.2 @1MHz	-94.3 @1MHz	-122.53 @1Mhz	-105.69 @1MHz	-123.29 @1MHz
Area (mm^2)	0.7	5.6	0.016	5.049	0.075	0.02	0.032	0.0048	0.665
FOM (nW/KHz)	30.44	2.025	4.83	274	0.78	2.647	1.8	0.416	1.04

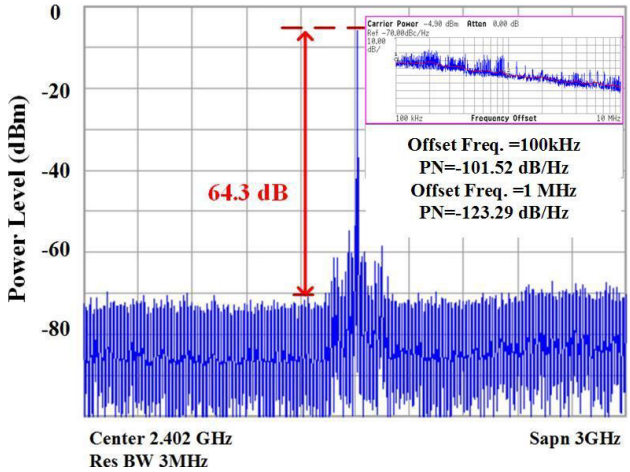


Fig. 14 Measured output spectrum and phase noise of 2.4 GHz output of the VCO with a supply voltage of 0.5V.

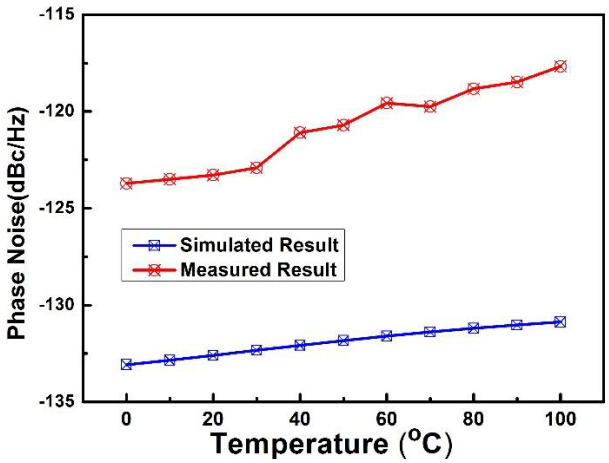


Fig. 15 Measured and simulated results of the relationship between phase noise and temperature.

designs are high power consumption with large die dimension.

3.3 Output Power Spectrum and Phase Noise

Figure 14 shows the measured results of the output spectrum and phase noise of 2.4 GHz output of the VCO with V_{DD} = 0.5V. As shows in Fig. 14, the phase noise is −101.52 dBc/Hz @100kHz offset and −123.29 dBc/Hz @ 1MHz as T = 20°C. Simulated and measured results of the relationship between phase noise and temperature are shown in Fig. 15. Phase noise becomes worse as temperature increases. The gm of LC-VCO MOSFETs is getting worse at high temperature, and the Q value of an inductor in low temperature is higher than high temperature [24]. The two main reasons lead to high phase noise at high temperature.

Measurement of power consumption and output power are summarized in Fig. 16. Output power change from −4.06 dBm to −5.23 dBm over a temperature range of 0 to 100°C. Measured results show that temperature variations barely influence all of the output power. There are two main reasons to support the measured results. First, all the measured results are calibrated to a fixed frequency = 2.4GHz by our calibrated mechanism. As output frequency does not vary with temperature, the variation of output power vary inconspicuously. Second, the output stage of CLCGs usually dominate the output power. The buffers are designed for ensuring stable output signals in every simulation under different situations, and the stable measured output power reflect an achievement of the design purpose of the buffers and an open drain circuit.

The power consumptions are 2.5 and 2.64 mW at T = 20 and 100°C respectively (excluding the output buffers and open drain circuit). We can infer that the power consumption increases as temperature raises from Fig. 16. Considering the fact that LC VCO dominates power consumption, the total power consumption would be increased while LC VCO frequency increases resulting from increasing temperature. Moreover, the minor correlation of frequency and temperature calibrated by the compensated circuit is applied to mitigate the situation such that the power consumption is not supposed to be increased theoretically. However, our inference from Fig. 16 is disaccord with the effect introduced by the compensated circuits. The explanation to this contradiction relies on the absence of compensated circuits in other circuits, such as digital parts. This absence undoubtedly enlarges the power consumption since increasing currents of MOSFETs lead to increasing power consumption as temperature increases.

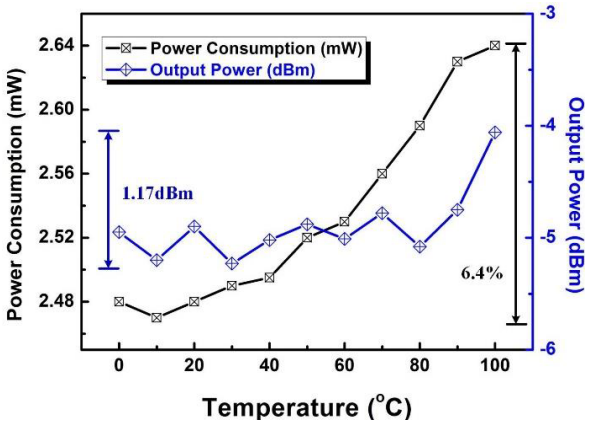


Fig. 16 Measured results of power consumption and output power

3.4 Figure of Merits

Figure 17 shows the figure of merits (FoM) versus temperature coefficients. The FOM is defined as the ratio of the power consumption to the oscillation frequency (nW/kHz) [10]. Calculated FOM is 1.04 nW/kHz for the proposed circuit. The crystal-less clock generators in Table 1 are classified into two categories by their operating frequency. One aims to replace XOs and is operated around MHz, such as [11] and [21]. The other is a substitute for

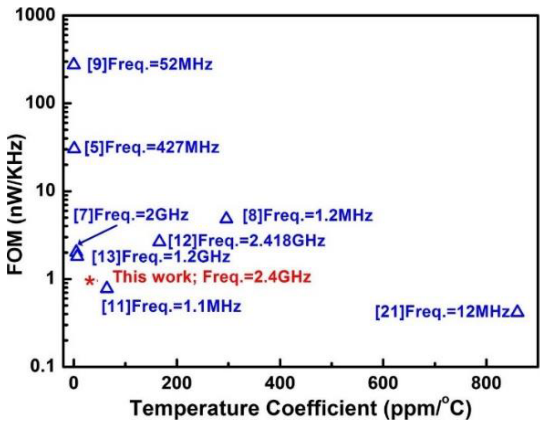


Fig. 17 FoM versus temperature coefficients

XOs and multipliers and is operated around GHz, such as [7] and [12]. The low operating frequency have better FOM because the existence of large noise provided by frequency multipliers is not included in FOM. Although, the FOM of our proposed work are slightly higher than [11] and [21], the TC of our work is actually better than [11] and [21]. In other word, our proposed work is considerably competitive if the above papers are operated at around GHz.

The proposed technique could not only be operated at ultra-low voltage, 0.5 v, and high frequency around GHz, but also automatically calibrate its temperature and process. As the related works only focus on a part of scenarios, either on supply voltage, power consumption, or frequency accuracy, the main contribution of the proposed method is the very first design investigating the whole situations.

4. Conclusion

The proposed ultra-low-voltage crystal-less clock generator with auto calibrated process and temperature compensated circuit has been successfully verified in a 65 nm CMOS technology. LC VCO provides low jitter and high phase noise performance, and TCC with an auto-calibration technique can detect and compensate the variations from the process and temperature. As demonstrated in this work, the proposed design that makes the operation of CLCG with very low supply voltages, down to 0.5 V, as well as achieve sufficient high frequency stability and accuracy against the variations from process and temperature for the HBC application.

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