On-Chip ESD Protection Device for High-Speed I/O Applications in CMOS Technology

Jie-Ting Chen, Chun-Yu Lin, *Member, IEEE*, and Ming-Dou Ker, *Fellow, IEEE*

***Abstract*— The diode operated under forward-biased condition has been widely used as an on-chip electrostatic discharge (ESD) protection device for high-speed circuits to sustain high ESD robustness, but the parasitic capacitance of diode may bring a negative impact to the circuits operating at higher speed. The ESD protection design with low parasitic capacitance has been strongly requested in high-speed I/O applications. The traditional methods to reduce parasitic capacitance were using a stacked diode or a stacked diode with embedded silicon-controlled rectifier (SCR). The stacked diode or the stacked diode with embedded SCR would have larger turn-on resistance to cause a higher clamping voltage. It should be further improved to achieve good ESD protection effectiveness for the high-speed I/O applications. In this paper, a new ESD protection device with reduced parasitic capacitance and smaller turn-on resistance to improve ESD protection effectiveness is proposed. The measurement results from the silicon chip have demonstrated that the proposed ESD device can achieve smaller parasitic capacitance, lower turn-on resistance, and higher ESD robustness, compared with the conventional devices. The proposed ESD protection device is very suitable to protect the high-speed I/O circuits in nanoscale CMOS technology.**

***Index Terms*— Diode, electrostatic discharge (ESD), ESD protection, high-speed I/O, silicon-controlled rectifier (SCR).**

I. Introduction

With the development of high-speed integrated circuits, improving circuit performance has been the direction of the industry efforts. These high-speed ICs prefer to being fabricated in nanoscale CMOS technology. Unfortunately, devices in nanoscale CMOS process are very sensitive to electrostatic discharge (ESD) events. The lower gate oxide breakdown and junction breakdown voltages seriously degraded the ESD robustness of ICs [1], [2], but the IC products still need to pass the ESD tests. The major component-level ESD test standard is human-body model (HBM) [3]. This model described the phenomenon of human body accumulated charge that induced device damage. In order to sustain required ESD robustness, the ESD protection devices must be a large device dimension. However, the parasitic capacitance of ESD protection devices is one of the most important issues of high-speed circuits [4]. A typical on-chip ESD protection scheme for high-speed I/O applications is shown in Fig. 1, where the parasitic capacitance of ESD protection diodes will cause the signal loss and induced the circuit's performance degradation. Therefore, the challenging of ESD protection designed for high-speed I/O applications has become the most important issue.

In order to minimize the parasitic capacitance of ESD protection devices and achieve the required ESD robustness, several high-speed ESD protection designs have been reported [5]–[10]. For instance, as shown in Fig. 2, using stacked diodes to reduce parasitic capacitance of

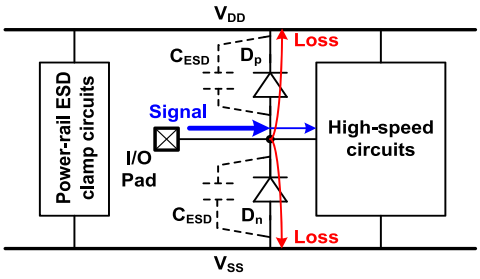

Fig. 1. Traditional ESD protection scheme with diodes at I/O pad for high-speed applications.

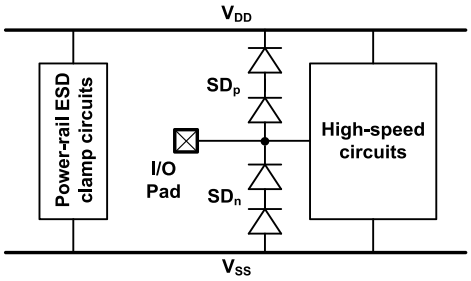

Fig. 2. Traditional ESD protection scheme with stacked diodes at I/O pad for high-speed applications.

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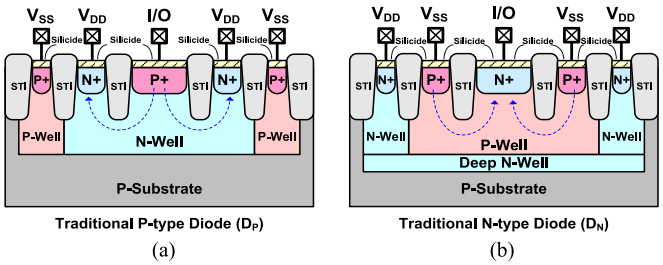


Fig. 3. Device cross-sectional view of (a) P-type diode (D_P) and (b) N-type diode (D_N).

ESD protection diodes has been presented [7]. Besides the traditional stacked diode, another method to reduce parasitic capacitance is the stacked diode with embedded silicon-controlled rectifier (SCR) [8]–[10].

Besides the component-level ESD test, the system-level ESD gun has been used to test the microelectronics products [11]. A special test method, human-metal model (HMM) [12], uses the system-level ESD gun to directly zap the I/O ports of the stand-alone devices or circuit module. The HMM test method will cause serious ESD damage on the I/O pins of IC products, even if the on-chip ESD protection devices were added in the IC chip. Recently, testing the HMM to the on-chip ESD protection devices are requested from the industry.

In this paper, a new ESD protection design for high-speed I/O applications is proposed and fabricated in nanoscale CMOS process. The performances of the new proposed ESD protection design are compared with several prior ESD protection designs. In addition to the traditional ESD test method, this paper performed the HMM test method on test circuits.

II. Test Structures of ESD Protection Design

The devices studied in this paper are implemented in a 130-nm 1.2-V fully silicide CMOS technology, according to the need of real product which operating frequency of the signal is from 0.1 to 5 GHz, and the capacitance limit of the ESD cells is 300 fF. Since four ESD current paths are needed to provide for I/O pad, including positive I/O to V_{SS} (PS), positive I/O to V_{DD} (PD), negative I/O to V_{SS} (NS), and negative I/O to V_{DD} (ND), the complementary structures are needed to protect the I/O. The P-type (P+/N-well) and N-type (N+/P-well) diodes are conventional ESD protection devices for high-speed I/O applications. The device cross-sectional view of diodes is shown in Fig. 3. In Fig. 3(a), the P+ of P-type diodes (D_P) is connected to I/O and the N+ is connected to V_{DD}. In Fig. 3(b), the N+ of N-type diodes (D_N) is connected to I/O and P+ is connected to V_{SS}. In order to decrease the parasitic capacitance of conventional diodes, using a stacked diode structure like a series capacitance can reduce parasitic capacitance. The device cross-sectional view of P-type stacked diode (SD_P) and N-type stacked diode (SD_N) are shown in Fig. 4. However, although the use of stacked diode can reduce parasitic capacitance, it will decrease ESD robustness because their overall turn-ON resistance and the clamping voltage will induce damage of internal circuits.

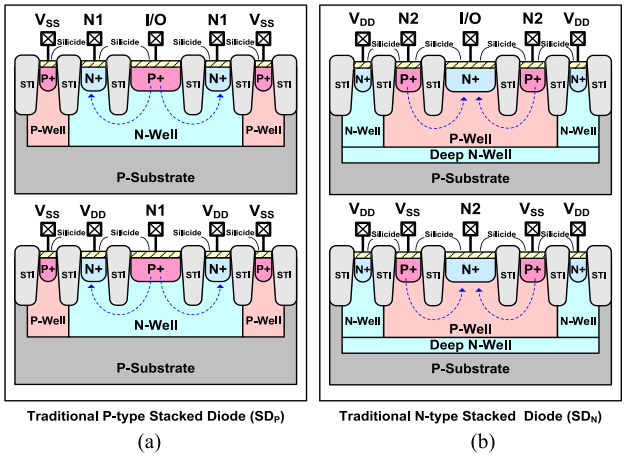


Fig. 4. Device cross-sectional view of (a) P-type stacked diodes (SD_P) and (b) N-type stacked diodes (SD_N).

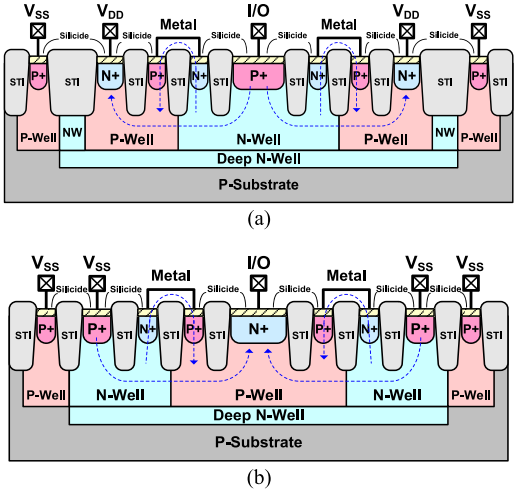


Fig. 5. Device cross-sectional view of (a) P-type stacked diodes with embedded SCR ($SDSCR_P$) and (b) N-type stacked diodes with embedded SCR ($SDSCR_N$).

Therefore, new stacked diodes with improving ESD robustness will be needed.

The ESD protection by using SCR for high-speed I/O applications has been reported [13]. The SCR has the characteristic of low parasitic capacitance and high ESD robustness. Furthermore, the stacked diodes with embedded SCR (SDSCR) have been reported for ESD protection with low turn-ON voltage [8], [9]. Fig. 5(a) and (b) shows the device cross-sectional views of P-type and N-type stacked diodes with embedded SCR ($SDSCR_P$ and $SDSCR_N$). The main path of SCR is formed by P+, N-well, P-well, and N+. In order to connect the N-well and P-well to reduce the trigger voltage, these devices use a metal to short N-well and P-well. In Fig. 5(a), the P+ of $SDSCR_P$ is connected to I/O pad and the N+ is connected to V_{DD}, and in Fig. 5(b), the N+ of $SDSCR_N$ is connected to I/O pad and the P+ is connected to V_{SS}. In the testing of ESD stress, ESD current will flow through the metal and turn ON the stacked diodes at first, and then the path of SCR will be triggered and take over

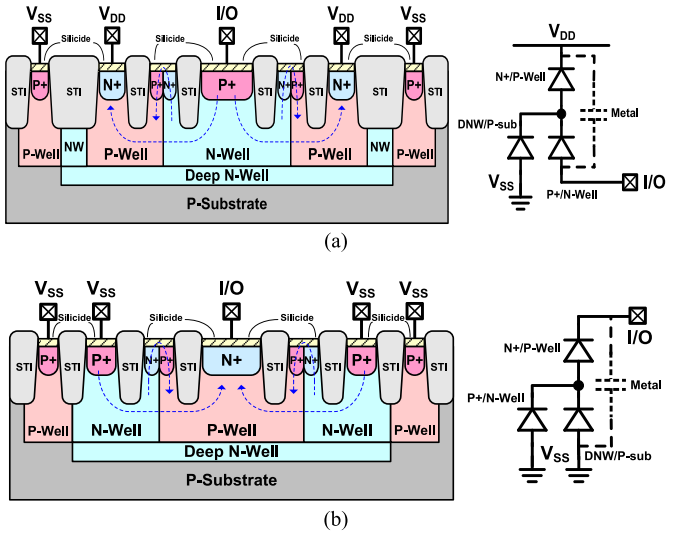


Fig. 6. Device cross-sectional views and effective circuits of (a) proposed P-type ESD protection device and (b) proposed N-type ESD protection device.

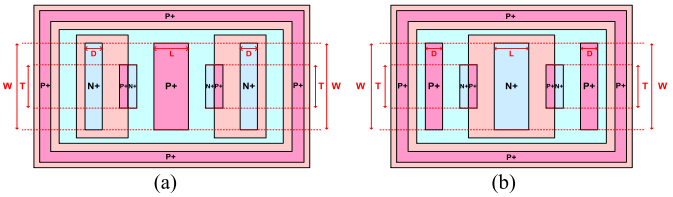


Fig. 7. Layout top views of (a) proposed P-type ESD protection device and (b) proposed N-type ESD protection device.

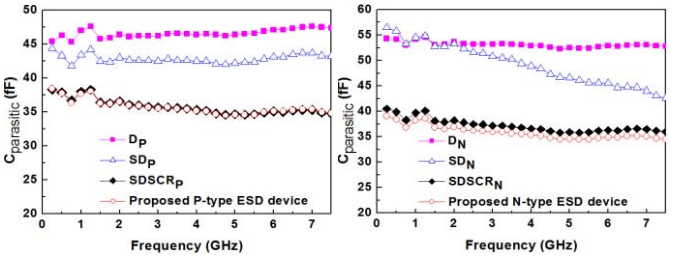


Fig. 8. Parasitic capacitance of (a) P-type devices and (b) N-type devices.

to discharge the primary ESD current. This mechanism is shown in Fig. 5. In fact, the device characteristics, including turn-ON resistance, layout area, and ESD robustness, can be further improved.

The proposed protection device for ESD protection is shown in Fig. 6. In order to reduce the turn-ON resistance and improve the ESD robustness, the design of proposed ESD protection device must have the shortest SCR path. In the proposed design, butting the P+ and N+ junction and using silicide to short N-well and P-well can achieve the target and simplify the metal routing. Putting the anode of proposed P-type ESD device in the center can minimize the P+/N-well junction, and putting the cathode of proposed N-type ESD device in the center can minimize the N+/P-well junction. Besides, putting the trigger junction along the P-well/N-well junction can simplify the metal routing and also reduce the parasitic capacitance. The silicide is a procedure of the standard CMOS process without additional mask. The proposed devices are fabricated in a triple well process which is used to implement the high-speed circuits. In the testing of ESD stress, ESD current will flow through the silicide and turn ON the stacked diodes, and then the path of SCR will be triggered and take over to discharge the primary ESD current. The triggered current path and main ESD discharge current path are shown in Fig. 6. Fig. 7 shows the layout top view of both types of proposed ESD protection devices.

III. Experimental Results of Test Devices

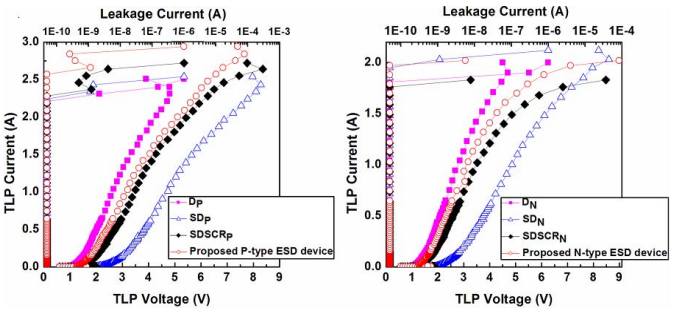
Each ESD protection device has been arranged with ground-signal-ground pads for test. For the purpose of reducing parasitic capacitance, the top metal is used to route to I/O pad, and the lower metal is used to route to V_{DD} and V_{SS}. The lengths of the centered junction ($L = 1.3\ \mu$m) and the outer junction ($D = 0.8\ \mu$m) for all test devices (diodes, stacked diodes, SDSCR, and proposed device) are the same. The width of centered junction (W) is designed as 30 μm. The trigger junction (T) is formed by P+ and N+ of SDSCR and proposed device. According to the previous research results of stacked diodes with embedded SCR [9], the trigger junction is the smaller the better, because the SCR path is wished to discharge the primary ESD current. Therefore, the width of the trigger junction size is selected as 1 μm.

A. Parasitic Capacitance

With the on-wafer and two-port S-parameter measurement, the parasitic effects of test devices are captured. In order to extract the exact parasitic capacitance of the stand-alone device at high frequency, the parasitic effects of the pads and the metal routing have been removed [14]. Fig. 8(a) and (b) shows the extracted parasitic capacitances of the test devices from 1 to 7.5 GHz. In Fig. 8(a), the conventional P-type diode has the largest parasitic capacitance. Using the stacked diodes can reduce capacitance at the rate of only 10% at 5 GHz. The parasitic capacitance of stacked diode is influenced by its local connection metal, because it is an inherent part of the device which should be retained and not be de-embedding [14]. The parasitic capacitances of SDSCR and proposed device are lower than conventional diode at the rate of about 25% at 5 GHz. Fig. 8(b) shows the similar results as described above. The conventional N-type diode has the largest parasitic capacitance, and the proposed device has the lowest one.

B. Transmission-Line Pulsing Measurement

In order to investigate the device behavior during ESD zapping stress, a transmission-line-pulsing (TLP) generator gave an ESD-like waveform which pulsewidth is 100 ns and rising time is about 10 ns. Analyzing the trigger voltage (V_{t1}), turn-ON resistance (R_{on}), and second breakdown current (I_{t2}) from TLP I–V characteristics can associate with the ESD robustness. Fig. 9(a) shows the comparison of TLP I–V curves of P-type test devices. The single diode has lowest trigger



(a) (b)

Fig. 9. TLP measured *I–V* characteristics of (a) P-type devices and (b) N-type devices. The leakage current is detected at reverse bias 1.2 V.

TABLE I
MEASURED RESULTS OF P-TYPE DEVICES

P-type	D_P	SD_P	$SDSCR_P$	Proposed device
Size of Device (μm)	W=30 D=0.8 L=1.3	W=30 D=0.8 L=1.3	W=30 D=0.8 L=1.3 T=1	W=30 D=0.8 L=1.3 T=1
V_{t1}(V)	1.03	2.1	2.00	1.63
R_{on} (Ω)	1.51	2.32	2.08	1.96
I_{t2} (A)	2.31	2.43	2.64	2.84
VF-I_{t2} (A)	6.18	6.4	4.95	7
HBM (kV)	4	4.2	4.5	5
HMM (kV)	1.4	1.1	1.4	1.7
Overshoot (V)	22.0	28.6	32.4	25.4
$C_{parasitic}$ (at 5 GHz)	46.4	42.2	34.0	33.7
R_{on}*$C_{parasitic}$ (Ω-fF)	70.06	97.90	70.72	66.05
$I_{t2}/C_{parasitic}$ (mA/fF)	49.78	57.58	77.65	84.27
HBM/$C_{parasitic}$ (V/fF)	86.21	99.53	132.35	148.37
HMM/$C_{parasitic}$ (V/fF)	30.17	26.07	41.18	50.44
VF-I_{t2}/ Overshoot*$C_{parasitic}$ (mA/V*fF)	6.05	5.30	4.49	8.18

voltage and clamping voltage. The stacked diodes have the highest trigger voltage, clamping voltage, and turn-ON resistance, which is not suitable for ESD protection due to the gate oxide of internal circuits may be damaged. Compared with SDSCR, the proposed ESD device has the lower trigger voltage, lower turn-ON resistance, and higher second breakdown current. Fig. 9(b) shows the similar results as described above. The conventional N-type diode has lowest trigger voltage and clamping voltage. The characteristics of the proposed device for ESD protection have been effectively improved, compared to those of SDSCR. All these measurement results are listed in Tables I and II.

C. ESD Robustness of Devices

The component-level HBM ESD robustness of the fabricated devices is tested. The failure criterion is defined as

TABLE II
MEASURED RESULTS OF N-TYPE DEVICES

N-type	D_N	SD_N	$SDSCR_N$	Proposed device
Size of Device (μm)	W=30 D=0.8 L=1.3	W=30 D=0.8 L=1.3	W=30 D=0.8 L=1.3 T=1	W=30 D=0.8 L=1.3 T=1
V_{t1}(V)	1.02	1.98	1.86	1.73
R_{on} (Ω)	1.69	2.7	2.5	2.27
I_{t2} (A)	1.9	1.95	*1.76	*1.97
VF-I_{t2} (A)	6.76	6.75	5.62	7.12
HBM (kV)	4	4	3.5	4.2
HMM (kV)	1.3	1.1	1.3	1.5
Overshoot (V)	22.8	26.5	33.7	26.3
$C_{parasitic}$ (at 5 GHz)	52.5	46.6	30.5	29.4
R_{on}*$C_{parasitic}$ (Ω-fF)	88.72	125.82	76.25	66.74
$I_{t2}/C_{parasitic}$ (mA/fF)	36.19	41.84	57.70	67.01
HBM/ $C_{parasitic}$ (V/fF)	76.19	85.84	114.75	142.86
HMM/ $C_{parasitic}$ (V/fF)	24.76	23.60	42.62	51.02
VF-I_{t2}/ Overshoot*$C_{parasitic}$ (mA/V*fF)	5.65	5.47	5.46	9.21

*limited by metal width

the *I–V* characteristics of the device shifting more than 20% from its initial curve or the reverse bias leakage current more than 1 μA after ESD stressed. The ESD test results of all devices are listed in Tables I and II. The HBM ESD robustness of D_P, SD_P, $SDSCR_P$, and proposed P-type device are 4, 4.2, 4.5, and 5 kV, respectively. The ESD robustness of D_N, SD_N, $SDSCR_N$, and proposed N-type device are 4, 4, 3.5, and 4.2 kV, respectively. According to measurement results, the proposed device has the highest ESD robustness.

In addition to component-level ESD test, the HMM robustness is tested. The HMM ESD robustness of D_P, SD_P, $SDSCR_P$, and proposed P-type device are 1.4, 1.1, 1.4, and 1.7 kV, respectively. The HMM robustness of N-type devices are 1.3, 1.1, 1.3, and 1.5 kV, respectively. The proposed device has the highest HMM robustness.

D. FOM Comparison and Discussion

The important factors of ESD protection devices for high-speed I/O applications include parasitic capacitance and ESD robustness. The higher ESD level and lower parasitic effect are needed. Besides, the device turn-ON behavior and the loading effect impact whether devices are suitable for high-speed applications or not. These Figures of Merit (FOMs) are compared in Tables I and II. The HBM means the maximum sustaining voltage level under HBM ESD test, and $C_{parasitic}$ is the parasitic capacitance of the devices. The value of HBM/$C_{parasitic}$ indicates the ESD robustness of per

unit parasitic capacitance. The higher value of HBM/$C_{\text{parasitic}}$ will be better. Furthermore, using turn-ON resistance (R_{on}) multiplies parasitic capacitance display suitability for high-speed circuit applications which represents the device turn-ON behavior and loading effect. The lower turn-ON resistance and parasitic effect are needed. Therefore, the lower value of $R_{\text{on}}{}^{*}C_{\text{parasitic}}$ will be better. $I_{t2}/C_{\text{parasitic}}$ means that the current handling ability per unit parasitic capacitance of the device. The HMM means the maximum sustaining voltage level under the HMM ESD test. The value of HMM/$C_{\text{parasitic}}$ denotes the robustness of per unit parasitic capacitance under system-level ESD test.

For the P-type ESD protection diode and stacked diode of $R_{\text{on}}{}^{*}C_{\text{parasitic}}$ are 70.06 and 97.90 $\Omega \cdot$ fF. For the P-type SDSCR and proposed device whose $R_{\text{on}}{}^{*}C_{\text{parasitic}}$ are 70.72 and 66.05 $\Omega \cdot$ fF. The test results of HBM/$C_{\text{parasitic}}$ for all P-type test devices that is from diode to proposed device are 86.21, 99.53, 132.35, and 148.37 V/fF, respectively. The $I_{t2}/C_{\text{parasitic}}$ of D_P, SD_P, SDSCR_P, and proposed P-type device are 49.78, 57.58, 77.65, and 84.27 mA/fF, respectively. The HMM/$C_{\text{parasitic}}$ of P-type devices are 30.17, 26.07, 41.18, and 50.44 V/fF, respectively. The N-type devices show the similar trend as described above. The $R_{\text{on}}{}^{*}C_{\text{parasitic}}$ of N-type devices that is from diode to proposed device are 88.72, 125.82, 76.25, and 66.74 $\Omega \cdot$ fF, respectively. The values of HBM/$C_{\text{parasitic}}$ for all N-type devices are 76.19, 85.84, 114.75, and 142.86 V/fF, respectively. The $I_{t2}/C_{\text{parasitic}}$ of D_N, SD_N, SDSCR_N, and proposed N-type device are 36.19, 41.84, 57.70, and 67.01 mA/fF, and the HMM/$C_{\text{parasitic}}$ of N-type devices are 24.76, 23.60, 42.62, and 51.02 V/fF, respectively.

According to the experimental results, the diode has the lowest turn-ON resistance because the shortest ESD current path, but only p-n-junction has the highest parasitic capacitance. The higher parasitic capacitance will cause higher signal loss. Using stacked diode can reduce parasitic capacitance, but it has the largest turn-ON resistance. The proposed ESD device improves parasitic capacitance, trigger voltage, and turn-ON resistance. The trend for FOMs of both type devices shows that proposed ESD devices are better for high-speed ESD protection. Therefore, the proposed ESD protection design can achieve better performance for high-speed circuit applications.

E. VF-TLP and Transient Overshoot Measurement

In order to investigate the turn-ON speed of the ESD protection devices during the ESD stress, very fast TLP (VF-TLP) is an important measurement method that is utilized to verify the performance of the ESD protection devices turn-ON behavior. The pulsewidth of VF-TLP in this paper is 5 ns and the rise time is 200 ps. Fig. 10(a) shows the comparison of VF-TLP I–V curves of P-type test devices. The single diode has the lowest trigger voltage and clamping voltage. The stacked diodes and SDSCR have the higher clamping voltage and turn-ON resistance. Compared with stacked diodes and SDSCR, the proposed ESD device has the lower clamping voltage, lower turn-ON resistance, and higher second breakdown current. Fig. 10(b) shows the similar results as described above. The conventional N-type diode has the lowest

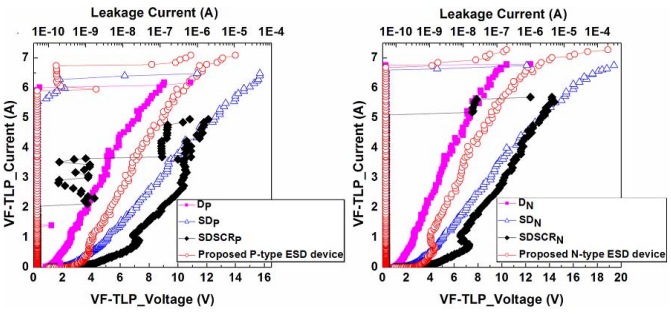


Fig. 10. VF-TLP measured I–V characteristics of (a) P-type devices and (b) N-type devices.

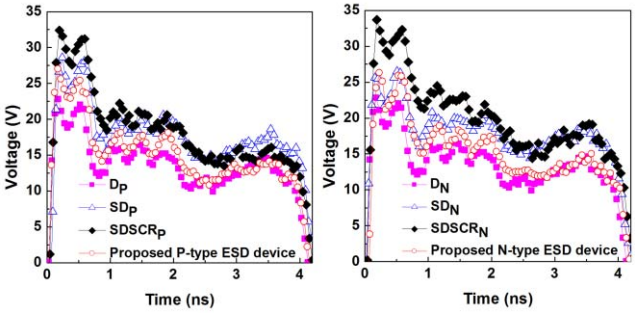


Fig. 11. VF-TLP measured voltage waveform of (a) P-type devices and (b) N-type devices under 4.8 A condition.

trigger voltage and clamping voltage. The N-type proposed device has the better ESD performance than stacked diodes and SDSCR.

In order to observe the turn-ON behavior during the high current of very-fast ESD transient, the overshoot waveform has been shown in Fig. 11. The voltage waveform is chosen under 4.8 A condition of VF-TLP current, and the value of overshoot is defined as the peak voltage. As shown in Fig. 11, the single diode has the lowest overshoot voltage and clamp voltage. The overshoot voltage and clamping voltage of the proposed ESD protection device are the second lowest. The stacked diodes and SDSCR have higher overshoot voltage and clamping voltage. If the FOM of the device during the VF-TLP testing is defined as VF-I_{t2}/(Overshoot * $C_{\text{parasitic}}$), where the VF-I_{t2} means the maximum sustaining current under the VF-TLP testing and Overshoot * $C_{\text{parasitic}}$ denotes the impact of overshoot voltage and parasitic capacitance, the FOM values of D_P, SD_P, SDSCR_P, and proposed P-type device are 6.05, 5.30, 4.49, and 8.18 mA/V * fF, respectively. The FOM values of D_N, SD_N, SDSCR_N, and proposed N-type device are 5.65, 5.47, 5.46, and 9.21 mA/V * fF, respectively. Based on the value of FOM, the proposed devices are more suitable for high-speed ESD protection applications.

The charge-device model (CDM) is another important ESD issue for high-speed circuits. The testing results of the field-induced CDM are influenced by the package type of chip [15]. In order to characterize the CDM robustness of test device, using the VF-TLP test method has been reported [16], [17]. The second breakdown current of VF-TLP means the maximum sustaining current during CDM testing, and it can be related to the CDM level. According to the JEDEC

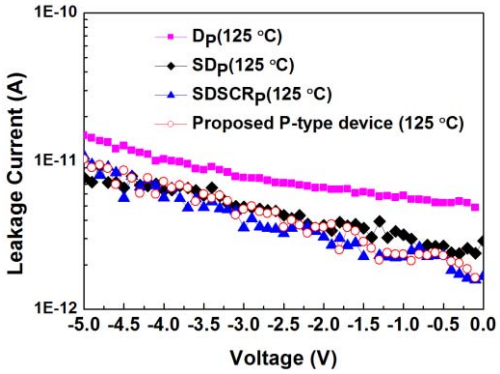


Fig. 12. Measured leakage currents of (a) P-type devices and (b) N-type devices under high-temperature (125 °C) condition.

JESD22-C101F standard of CDM test method, the peak current of the small and large module under CDM 500 V testing are 5.75 and 11.5 A, respectively. If the VF-TLP second breakdown current is higher than 5.75 A, it means the device can sustain the 500-V CDM zapping in the small package type [18]. Based on the above VF-TLP measurement results, the second breakdown current of the proposed ESD protection device is about 7 A that can against 500-V CDM testing under the small test module. Besides, the test circuit can be enlarged to have higher ESD robustness.

F. DC I–V Curve of ESD Devices

Fig. 12 shows the dc I–V curves of the protection device at high temperature (125 °C). In this paper, the operational voltage is selected as 1.2 V, so the leakage current at −1.2 V should be noticed. The leakage currents of D_P, SD_P, $SDSCR_P$, and proposed P-type device at −1.2 V are 5.8, 3, 2.3, and 2.4 pA, respectively. For the N-type devices, the leakage current of D_N, SD_N, $SDSCR_N$, and proposed N-type device at −1.2 V are 4.5, 1.9, 1.8, and 1.5 pA, respectively. For the proposed P-type and N-type devices, the leakage currents are sufficiently low under normal operating condition.

IV. Discussion

With the development of high-speed integrated circuits, the circuits operated at higher frequencies and fabricated in advanced technologies is the trend of industry. The most common devices for ESD protection in advanced technologies are the diode and SCR [14], [19]–[21]. In order to sustain enough ESD robustness, the large parasitic capacitance of the large-size diode not only causes large signal losses, but also increases the difficulty of circuit matching at high frequency [22], [23]. The most widely known problems of the SCR are turn-ON speed and holding voltage even though it has low parasitic capacitance and high ESD robustness. According to above measurement results, the proposed ESD protection device can achieve higher ESD robustness, lower parasitic capacitance, lower turn-ON resistance, and fast turn-ON response. The proposed ESD protection devices have been fabricated in the standardization process. It can implement in any nanoscale CMOS process easily, smaller footprint, and simpler metal routing. Therefore, the proposed ESD protection design can achieve better performance for high-speed circuit applications.

V. Conclusion

The proposed ESD protection device has been verified in a 130-nm CMOS process for high-speed I/O applications. The proposed ESD device uses a P+ and N+ junction contact with silicide to shorten the path of SCR, which can reduce the trigger voltage and turn-ON resistance to get higher ESD robustness. As compared to the prior ESD protection devices, the experimental results showed that the proposed device has the better FOMs. The two major FOMs are defined as HBM/$C_{\text{parasitic}}$ and VF-I_{t2}/(Overshoot * $C_{\text{parasitic}}$). The FOM values of the proposed P-type device are 148.37 and 8.18, respectively, which have been improved more than 30% compared with those of the traditional diode. Therefore, the proposed device verified in this paper will be a useful ESD protection solution for the high-speed I/O applications in the nanoscale CMOS technology.

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