A Digitally Dynamic Power Supply Technique for 16-Channel 12 V-Tolerant Stimulator Realized in a 0.18-μm 1.8-V/3.3-V Low-Voltage CMOS Process

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***Abstract*—A new digitally dynamic power supply technique for 16-channel 12-V-tolerant stimulator is proposed and realized in a 0.18-μm 1.8-V/3.3-V CMOS process. The proposed stimulator uses four stacked transistors as the pull-down switch and pull-up switch to withstand 4 times the nominal supply voltage ($4 \times V_{DD}$). With the dc input voltage of 3.3 V, the regulated three-stage charge pump, which is capable of providing 11.3-V voltage at 3-mA loading current, achieves dc conversion efficiency of up to 69% with 400-pF integrated capacitance. Power consumption is reduced by implementing the regulated charge pump to provide a dynamic dc output voltage with a 0.5-V step. The proposed digitally dynamic power supply technique, which is implemented by using a p-type metal oxide semiconductor (PMOS) inverter with pull-down current source and digital controller, greatly improves the power efficiency of a system. The silicon area of the stimulator is approximately 3.5 mm^2 for a 16-channel implementation. The functionalities of the proposed stimulator have been successfully verified through animal test.**

***Index Terms*—Dynamic power supply technique, high-voltage-tolerant, power efficiency, regulated charge pump, stimulator.**

I. Introduction

NEURO-STIMULATORS have been widely used in cardiac pacemaker, cochlear implant, bladder stimulation, neuromuscular electrical stimulation, deep brain stimulation, implantable visual prosthesis, etc. [1]–[15]. Those stimulators are capable of delivering charges into the tissue via electrodes. If sufficient charges are injected into the working electrodes, it can artificially depolarize some portion of the axon membrane to the threshold, and trigger the action potentials in axons [5]. In order to achieve a more effective electrical stimulation, a multi-channel stimulator is necessary. For example, cochlear implants with multiple channels can stimulate different positions to select the different audio frequencies. Using multi-channel stimulation to suppress epileptic seizure can stimulate more accurately the position of the source of abnormal discharge to get better therapy result. There are many challenges for designing a stimulator. Issues such as realization of high level of integration to reduce the size of the implant devices, efficient power delivery to the stimulators, delivery of the safe electrical stimulation to avoid damaging the tissue and electrode, and reducing of the medical costs, are some of the challenges faced by the circuit designers [6].

The required supply of a stimulator varies from a few volts to tens of volts in various applications [7]. For instance, the supply voltage of stimulator for suppressing epileptic seizure can be up to 12 V. There are two approaches to realize a high-voltage-tolerant stimulator in the prior literatures [1]–[10]. One approach is to use high voltage (HV) devices, and the other approach is to use the concept of stacked low voltage (LV) devices [8], [9]. The HV devices should be manufactured using the standard CMOS process with HV layers and some special layout techniques. Using LV devices in low voltage CMOS process to realize stimulator can reduce the size and the cost of the implantable medical devices because the stimulator can be fully integrated with the microcontroller or the biomedical signal processor into an SoC.

For implantable stimulators, power consumption is often the limiting factor in determining the size of power coil or battery. Improvements in power efficiency lead to the reductions in coil or battery size and the increases in battery lifetime. If the size of implantable stimulators can be decreased, the safety and comfort of patient are increased. Thus, there is a strong motivation to improve the power efficiency of implantable stimulators.

In this work, a novel digitally dynamic power supply technique for 16-channel 12V-tolerant stimulator is proposed and realized in a 0.18-μm 1.8-V/3.3-V CMOS process. Unlike the traditional dynamic power supply techniques which consisted of many analogue circuits (e.g. ADC, amplifier, comparator, and reference), the proposed power control system is designed and realized by using digital circuits. Experimental results show that the power efficiency of the stimulator has been greatly improved.

II. Dynamic Power Supply Techniques for Stimulator

Fig. 1 shows a typical current-controlled stimulator (CCS) with $n \times V_{DD}$ supply realized in LV CMOS process. The

Manuscript received January 31, 2017; revised March 27, 2017 and May 31, 2017; accepted June 5, 2017. Date of publication July 18, 2017; date of current version September 25, 2017. This work was supported in part by the Ministry of Science and Technology (MOST), Taiwan, under Contracts of MOST 104-2220-E-009-004, MOST 105-2221-E-009-166, and MOST 106-3114-8-009-001. This paper was recommended by Associate Editor A. Demosthenous. *(Corresponding author: Ming-Dou Ker.)*

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Digital Object Identifier 10.1109/TBCAS.2017.2713122

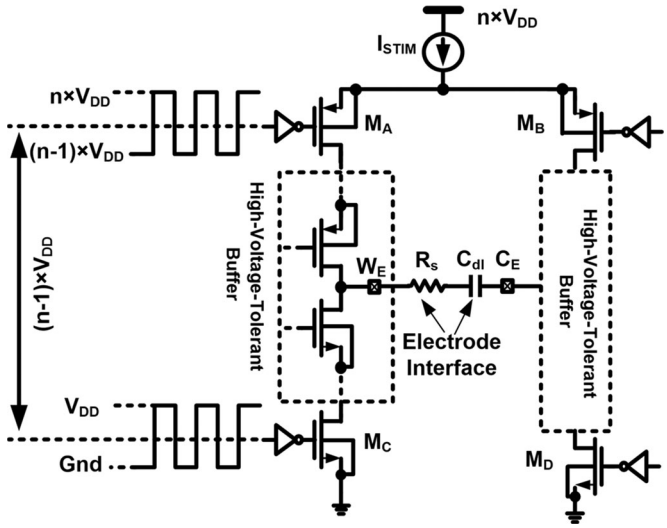

Fig. 1. Schematic of a typical current-controlled stimulator, where the output is connected to an equivalent electrode model.

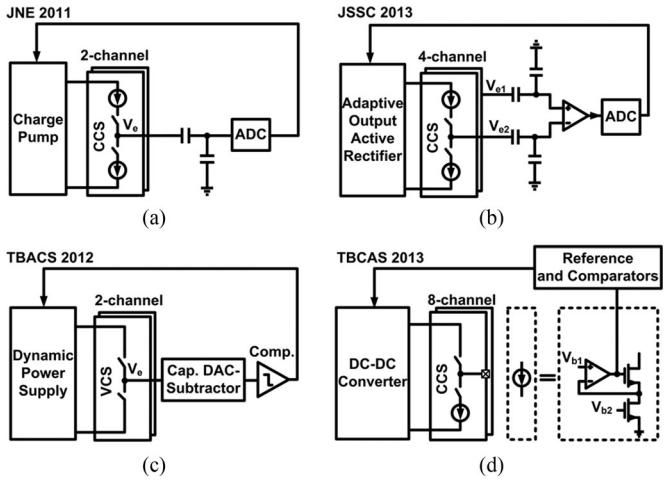

Fig. 2. Various dynamic power supply techniques for stimulator. (a) The dynamic power supply technique, realized in an HV CMOS process, in [7]. (b) The dynamic power supply technique in [10]. (c) The dynamic power supply technique in [11]. (d) The dynamic power supply technique for CCS, realized in an HV CMOS process, in [12].

outer transistors ($\mathrm{M_A}$, $\mathrm{M_B}$, $\mathrm{M_C}$, and $\mathrm{M_D}$) are controlled by the level shifter which converts the low-level voltage to the high-level voltage with an DC offset of $(\mathrm{n}-1) \times \mathrm{V_{DD}}$. When the transistors ($\mathrm{M_A}$ and $\mathrm{M_D}$) are turned on, and the transistors ($\mathrm{M_B}$ and $\mathrm{M_C}$) are turned off, cathodic electrode $\mathrm{C_E}$ is pulled down to ground. The stimulus current $\mathrm{I_{STIM}}$ flows into the tissue through the anodic electrode $\mathrm{W_E}$. The voltage on electrode $\mathrm{W_E}$ can be expressed as

$$V_{elec}(t) = V_s + V_{dl}(t) = |I_{\mathrm{STIM}}| \cdot \left(R_S + \frac{t}{C_{dl}}\right) \quad (1)$$

where V_s is the voltage drop across the solution resistance R_S, $V_{dl}(t)$ is the instantaneous voltage across the double layer capacitor C_{dl}. In (1), $V_{elec}(t)$ rises to $|I_{\mathrm{STIM}}| \cdot R_S$ instantaneously once the stimulus current is applied. Power loss of the stimulator can be calculated as

$$P_{loss} = \left[V_{Supply} - |I_{\mathrm{STIM}}| \cdot \left(R_S + \frac{t}{C_{dl}}\right)\right] \cdot |I_{\mathrm{STIM}}| \quad (2)$$

where V_{Supply} is the supply voltage. The first item in (2) is the voltage drop across the current source and switches. In order to maximize the overall efficiency of the stimulator, dynamic power supply techniques are required to minimize the voltage drop across the current generator, and also to ensure the current generator operates in saturation region, while complex monitoring circuits are required for instantaneous adjustment of the supply voltage during the stimulation [3].

The existing dynamic power supply techniques can be divided into two classes: pseudo-closed-loop dynamic power supply technique and closed-loop dynamic power supply technique. The pseudo-closed-loop dynamic power supply technique just adjusts the power supply as programmed, and the program does not continuous. On the contrary, the closed-loop dynamic power supply technique continuously monitors the operating state of the stimulator and automatically adjusts the power supply when it is needed.

A. *Pseudo-Closed-Loop Dynamic Power Supply Techniques*

Fig. 2 compares various dynamic power supply techniques. The conventional dynamic power supply technique in Fig. 2(a) utilized a capacitive attenuator and ADC to attenuate and digitize the maximum electrode voltage of the CCS, respectively. Then, the charge pump was controlled by ADC to provide a dynamic voltage [7]. H. Lee designed another highly efficient CCS with a pseudo-closed loop [10], which is shown in Fig. 2(b). The difference voltage between the electrodes was attenuated, single-ended, and digitized by the capacitive attenuator, differential amplifier, and ADC, respectively. Finally, the active rectifier was controlled to provide a dynamic supply. In addition, the gate voltage of the transistor in the current generator circuit [2] and the maximum electrode voltage [3] were monitored to provide an adjustable supply voltage. The dynamic power supply techniques described in this section just adjust the power supply as programmed.

B. *Closed-Loop Dynamic Power Supply Techniques*

The voltage-controlled stimulator in [11] utilized another dynamic power supply technique, as shown in Fig. 2(c), to maximize the power efficiency. The electrode voltage was sampled periodically by the DAC-subtractor with a comparator to decide whether the electrode voltage was greater or less than the predefined voltage. If the electrode voltage was greater than the predefined voltage, the dynamic power supply would be increased continuously. For current-controlled stimulator, the stimulus current is related to the operating region of the stimulus current generators. If the stimulus current generators are operating the saturation region, the performance of charge balance will be well enough. In [12], a dynamic power supply technique, through monitoring the gate voltage of the transistor in the regulated cascode current sink, has been proposed. As shown in Fig. 2(d), the gate voltage of the outer transistor was monitored by comparators and a reference. A switched capacitor

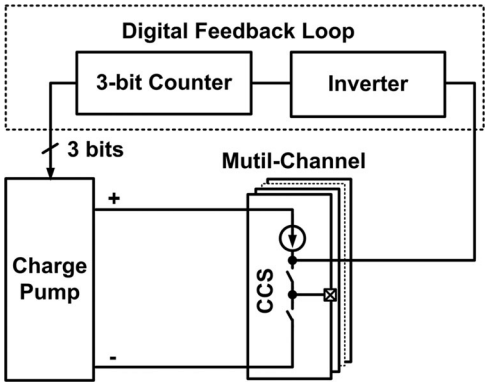

Fig. 3. The new proposed digitally dynamic power supply technique for 16-channel CCS with current source. It is realized in an LV CMOS process.

DC-DC converter with 1000-pF integrated capacitance is used to provide a continuous voltage at 3-V step. The dynamic power supply technique in Fig. 2(d) was realized in a 0.18-μm 1.8-V/20-V CMOS process. In addition, the voltage compliance of cascode current source was monitored by a comparator and a reference to provide a continuous adjusting voltage [13]. The existing stimulators with dynamic power supplies use complex monitoring circuits, such as attenuator, ADC, amplifier, comparator, which lead to large layout area and power dissipation.

The novel proposed closed-loop dynamic power supply technique for 16-channel 12V-tolerant stimulator, realized in a 0.18-μm 1.8-V/3.3-V CMOS process, is shown in Fig. 3. In the proposed CCS, the monitoring circuit examines the operating region (triode vs. saturation) of the current source by a simple inverter. The output of the regulated charge pump is driven by a digital input, eliminating the need of the decision-making analogue circuits. The experimental results have shown that the proposed new digital dynamic power supply technique can greatly improve the power efficiency.

III. Circuit Implementation

The proposed stimulator uses the stacked transistors configuration to prevent the low voltage transistors from the electrical overstress and the gate-oxide reliability issues. The $\mathrm{n} \times \mathrm{V_{DD}}$ high-voltage-tolerant buffers or stimulators have been reported and verified successfully in LV CMOS process [8], [9], [14]–[19].

A. Overall Architecture of the Proposed 16-Channel Stimulator

The overall architecture of the proposed 16-channel stimulator is shown in Fig. 4. The stimulus drivers are grouped into 4 regions, and each region consists of 4 stimulus drivers. The decoder decides which two of the stimulus drivers are activated, and also decides the interval of stimulus current pulse, stimulation width, and the interphase delay. The stimulus current amplitude is decided by the 3-bit current DAC. Mode controller is used to control the operation mode of the stimulator, which includes the stimulation mode and the detection mode. The adaptive regulated charge pump is turned on in the stimulation mode. Correspondingly, it will be turned off, and discharged to the ground by the quick-discharge circuit in the detection mode. The current DAC is composed of the cascode current source. The triode indicator is used to monitor the drain-source voltage of the cascode transistor in the current generator. Once the cascode transistors leave the saturation, digital controller will be activated to control the regulated charge pump to generate a higher voltage.

B. High-Voltage-Tolerant Stimulator Buffer with Triode Indicator

Fig. 5 shows the detailed schematic of the proposed CCS. It consists of a high-voltage-tolerant buffer [9], self-adaption bias circuit, nth $\mathrm{V_{DD}}$ bias circuit, quick-discharge circuit, and the triode indicator. nth $\mathrm{V_{DD}}$ bias circuit is used to provide $3 \times \mathrm{V_{DD}}$, $2 \times \mathrm{V_{DD}}$, and $1 \times \mathrm{V_{DD}}$ bias voltages with outputting current capability at nodes b1, b2, and b3, respectively. Decoupling capacitors need to be added to the nodes (b1, b2, and b3). Transistors ($\mathrm{M_1}$ to $\mathrm{M_4}$) and transistors ($\mathrm{M_5}$ to $\mathrm{M_8}$) act as the pull-up switch and pull-down switch, respectively, to withstand 4 times nominal supply voltage $(4 \times \mathrm{V_{DD}})$ without degrading the transistor reliability. The outer transistors ($\mathrm{M_1}$ and $\mathrm{M_8}$) are drived by the taper inverters for reducing the peak transient drain-source voltages of the transistors ($\mathrm{M_4}$ and $\mathrm{M_5}$), during the switching operation. Transistors ($\mathrm{M_{B1}}$ to $\mathrm{M_{B6}}$) act as a self-adaption bias circuit, which is designed to keep the voltages across the terminals of the stacked transistors within the safe voltage range of $1 \times \mathrm{V_{DD}}$ during the operation.

Triode indicator, which is a p-type metal oxide semiconductor (PMOS) inverter with pull-down current source, is used to monitor the operating region of the cascode current mirror. Transistors ($\mathrm{M_{C1}}$ to $\mathrm{M_{C4}}$) act as a wide-swing cascode current mirror. The overdrive voltages of those transistors are $\sim$ 200 mV when the drain current is 3 mA. If those transistors are operating in the saturation region, the drain current (stimulus current) of $\mathrm{M_{C4}}$ can be matched accurately to the output current of a 3-bit current DAC. Triode indicator, biased with 5 μA, monitors the operating region of the transistors in the cascode current mirror all the time. In consideration of the voltage ripple in the power line, the process-voltage-temperature (PVT) variation, the delay time in the feedback circuit, and the rising speed of electrode voltage, the triode indicator will output an "error" signal when the voltage drop across $\mathrm{M_{C3}}$ and $\mathrm{M_{C4}}$ reaches the threshold voltage $(\mathrm{V_{THP}})$ of a PMOS transistor. The rising edge of this "error" will enable the digital controller to increase the supply voltage of stimulator. In general, the rising speed of the supply voltage, which is provided by the regulated charge pump, is much faster than that of the electrode voltages. As described in (1), when $\mathrm{I_{STIM}}$ is 3 mA and $\mathrm{C_{DL}}$ is 100 nF, the rising time, where the electrode voltage increases by 400 mV (the source-gate voltage of $\mathrm{M_{C5}}$ minus the overdrive voltages of transistors $\mathrm{M_{C3}}$ and $\mathrm{M_{C4}}$), is 13.3 μs. If the digital controller can deal with these rising edges promptly, the wide-swing cascode current mirror can operate in the saturation region all the time. In addition, the power efficiency of the stimulator could be optimal if the voltage $(\mathrm{V_{BP}})$ at the gate of $\mathrm{M_{C3}}$ varies with the stimulation

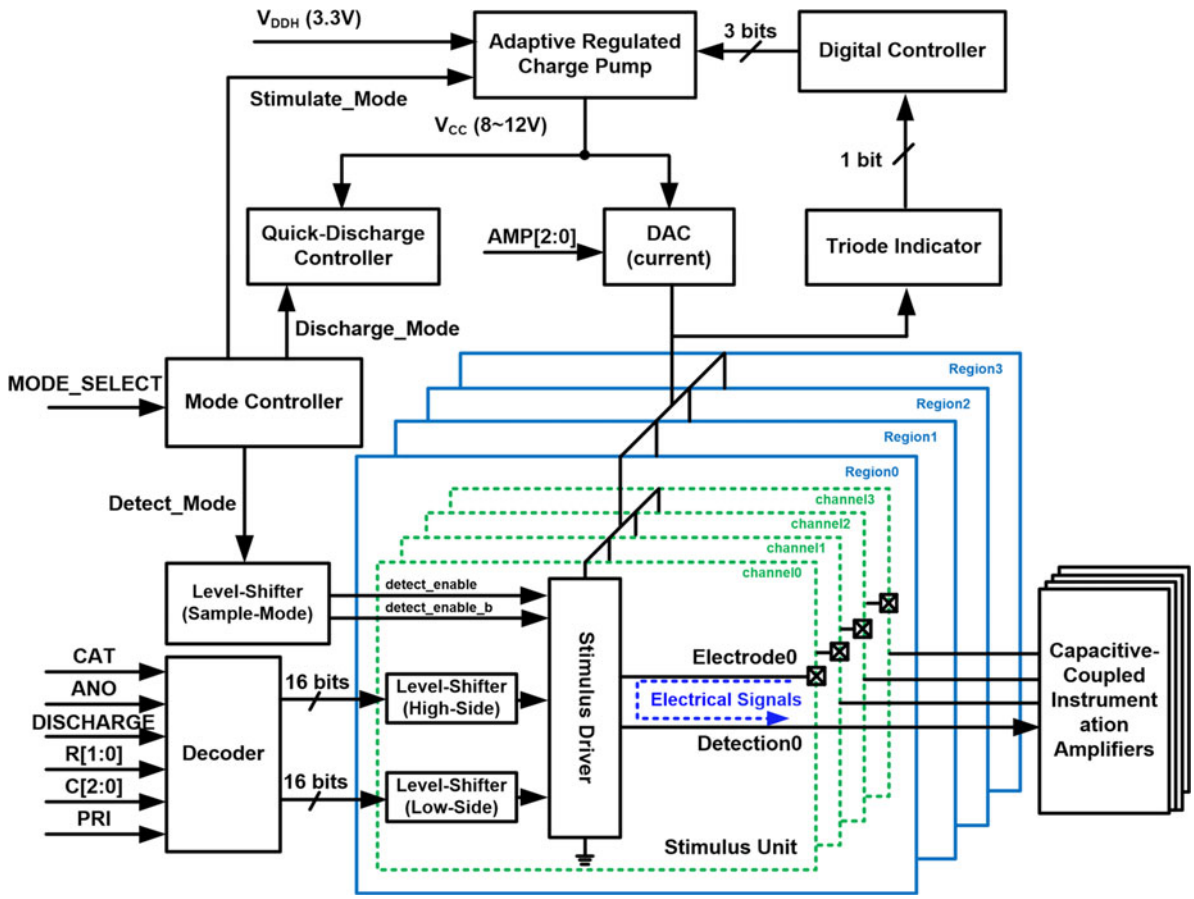

Fig. 4. The overall architecture of the proposed 16-channel 12V-tolerant stimulator with adaptive power supply.

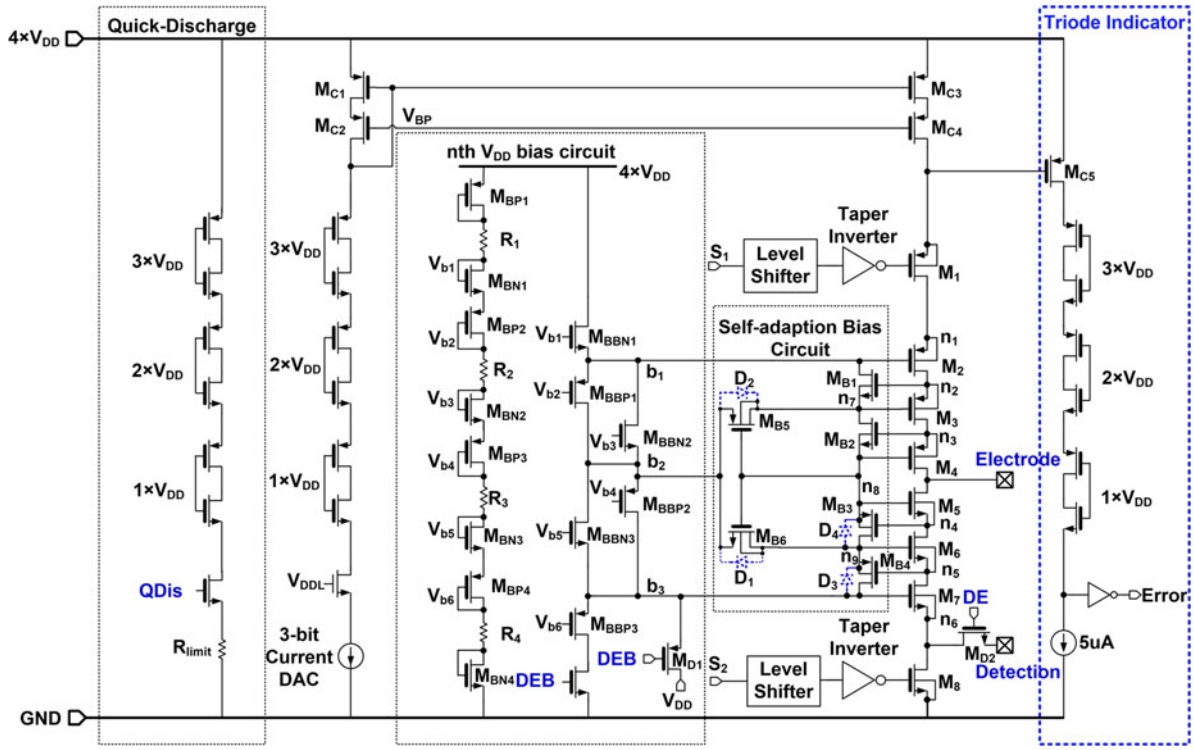

Fig. 5. The detailed circuit of the proposed high-voltage-tolerant buffer with triode indicator and quick-discharge circuits. Transistors M_1 to M_8 in output buffer, transistors M_{B1} to M_{B6} in self-adaption bias circuit, transistors M_{D1} and M_{D2}, level shifters, and taper inverters need to be replicated for each channel. The dimensions of the transistors $\mathrm{M}_{\mathrm{BN1}}$ to $\mathrm{M}_{\mathrm{BN4}}$, $\mathrm{M}_{\mathrm{BP1}}$ to $\mathrm{M}_{\mathrm{BP4}}$, $\mathrm{M}_{\mathrm{BBN1}}$ to $\mathrm{M}_{\mathrm{BBN3}}$, $\mathrm{M}_{\mathrm{BBP1}}$ to $\mathrm{M}_{\mathrm{BBP3}}$, M_{B1} and M_{B2}, M_{B3} and M_{B4}, M_{B5} and M_{B6}, M_{C5}, and resistors R_1 to R_4 are 1 μm/0.35 μm, 4 μm/0.35 μm, 2 μm/0.35 μm, 8 μm/0.35 μm, 1 μm/5 μm, 3 μm/0.35 μm, 50 μm/0.35 μm, 40 μm/0.3 μm, and 50 kΩ, respectively, realized in a 0.18-μm CMOS process.

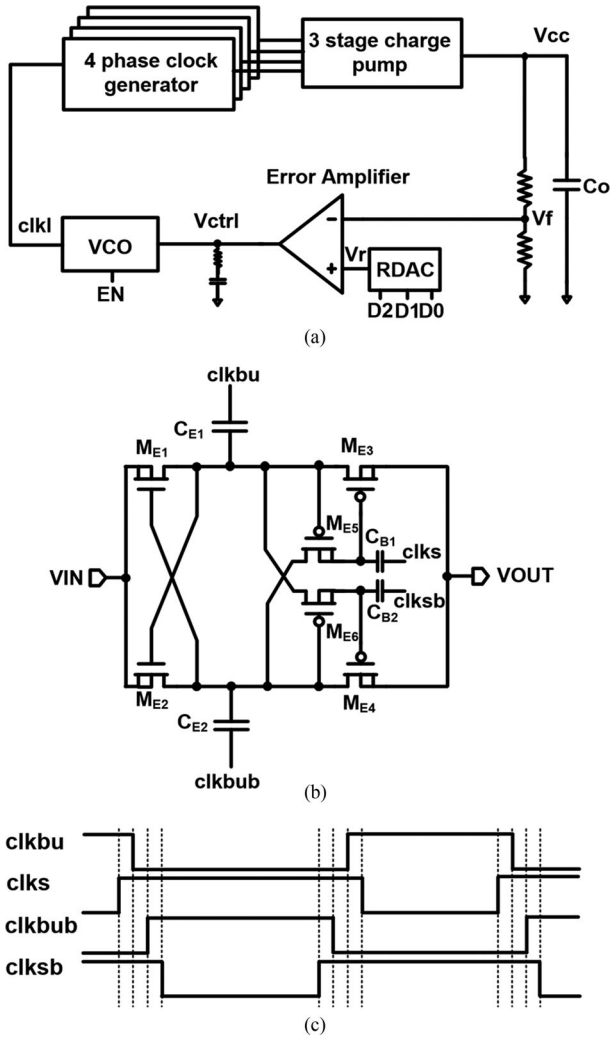

Fig. 6. (a) The overall architecture of the proposed the system of regulated charge pump. (b) The detailed schematic of one stage in the charge pump. (c) The timing diagram for the 3-stage charge pump.

current. Three stacked inverters are used to withstand a higher operation voltage.

The capacitive-coupled instrumentation amplifiers [8], which are the first stage in the action potential recording channels, are used to amplify the electrical signals from neurons. During stimulation period, the stimulus voltages on the electrode may be up to $4 \times \mathrm{V_{DD}}$. Thus, the amplifiers should be disconnected from the electrodes in the stimulation phase to prevent the transistors in amplifiers from electrical overstress, and be reconnected after the stimulation artifact vanishes. When transistors (M_{D1} and M_{D2}) and the parasitic diodes (D_3 and D_4) are turned on, the voltages on nodes n_9 and n_8 are $(V_{DD} - V_{TH})$ and $(V_{DD} - 2 \cdot V_{TH})$, respectively. In this way, transistors (M_5, M_6, and M_7) are turned on, and the electrode can be reconnected to the action potential recording channel.

Quick-discharge circuit is activated to discharge the charges on the supply line within a small time-window before and after the stimulus pulses is applied. Once the control signal QDis goes from low to high, the charges on the supply line will be discharged to the ground.

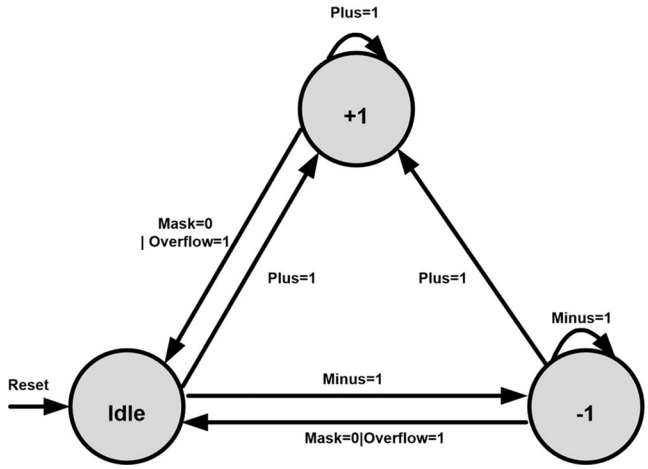

Fig. 7. State diagram of the counter which controls the 3-bit RDAC.

C. Adaptive Regulated Charge Pump

The overall architecture of the regulated charge pump system is shown in Fig. 6(a) [20]–[22]. It consists of voltage divider, error amplifier, voltage control oscillator (VCO), level shifter, 4-phase clock generator, and 3-stage charge pump. Pulse frequency modulation (PFM) feedback network is used to generate the regulated output voltage $\mathrm{V_{CC}}$. When $\mathrm{V_{CC}}$ is lower than the predefined voltage, Vctrl, which is the output of the error amplifier and the input control signal of VCO, becomes higher. Thus, the frequency of VCO arises until $\mathrm{V_{CC}}$ equals to the predefined voltage. In contrast, the frequency of VCO becomes slower, when $\mathrm{V_{CC}}$ is greater than the predefined voltage. The regulated output voltage is programed by the 3-bit resistor DAC and the digital controller. Voltage-controlled oscillator (VCO), in Fig. 6(a), is a current starved ring oscillator. Five inverters are attached in a chain, and the output of the last inverter is fed back into the input of the first inverter. Error amplifier, in Fig. 6(a), is a single stage op-amp.

The detailed schematic of one stage in the charge pump and the corresponding timing diagram are shown in Fig. 6(b) and Fig. 6(c), respectively. Each stage of the charge pump is implemented as a 4-phase voltage doubler (FPVD). The separated capacitor pairs (C_{E1} and C_{E2}) for voltage pumping and (C_{B1} and C_{B2}) for clock boosting are used to achieve smaller voltage drops, and reduce the conduction loss. A voltage doubler cell is used to separate the gate driving of the NMOS switches (M_{E1} and M_{E2}) from that of the PMOS switches (M_{E3} and M_{E4}). In this way, the reverse currents can be eliminated. The bulk terminals of the devices are connected to their respective sources terminals.

D. Digital Controller for Dynamic Power Supply

Power efficiency is critically important for implantable biomedical devices. Current-controlled stimulator can achieve high power efficiency when its supply voltage adapts to the electrode voltage.

Fig. 7 shows the finite state machine made up of a 3-bit counter to control the 3-bit resistor DAC in the adaptive

TABLE I
COUNTER STATE DESCRIPTIONS

State	Action
Idle	The counter value defaults to 7 after the reset action. In other case, it equals to the value in previous state. And signal "overflow" is reset to 0.
+1	The output value of counter increases by 1. Correspondingly, supply voltage steps up at 0.5 V immediately.
−1	The output value of counter decreases by 1. Correspondingly, supply voltage steps down at 0.5 V immediately.
Mask	Mask = 1 during the phase of cathodic or anodic stimulation. In other case, mask = 0.
Error	Output signal of triode indicator.
Plus and Minus	When mask = 1, signal "error" will be sampled periodically by a D-flip flop with output signals "plus" and "minus". If error = 1, plus = 1 and minus = 0. If error = 0, plus = 0 and minus = 1. After the counter has been increased or decreased by 1, "plus" and "minus" will be reset to 0. In addition, the rising edge of "error" can also set "plus" and "minus" to 1 and 0, respectively. In other case, signals "plus" and "minus" are reset to 0.
Overflow	If the counter reaches the value 0 or 7, overflow = 1. In other case, overflow = 0.

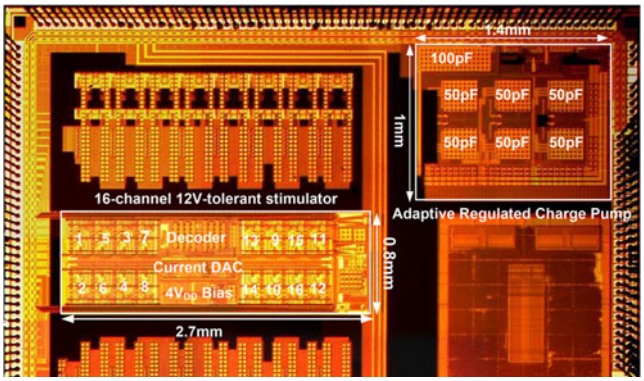

Fig. 8. Die photo of the fabricated fully integrated stimulator with dynamic power supply.

regulated charge pump. The counter runs on a fixed 50 MHz clock and steps through the various states indicated in Fig. 7 to provide an adaptive supply voltage for reducing the power consumption of stimulator as described in Table I. For example, once the voltage drop across M_{C3} and M_{C4} is lower than the source-gate voltage (about one threshold voltage) of M_{C5}, the triode indicator will output a positive pulse as described in Section B. Moreover, the digital controller will be activated by those positive pulses to enable the counter to increment by one immediately. Correspondingly, the supply voltage increases by 0.5-V step voltage.

IV. EXPERIMENTAL RESULTS

The stimulator chip has been fabricated in a 0.18-μm 1.8-V/3.3-V CMOS process. The die photo is shown in Fig. 8. The pumping capacitors (C_E) of the charge pump are 50 pF, and the output capacitor (C_O) is 100 pF. All of the capacitors are implemented by using the metal-insulator-metal capacitor and are fully integrated on the chip. The silicon area of the 16-channel 12V-tolerant stimulator and regulated charge pump are 2.1 mm^2 and 1.4 mm^2, respectively. The supply voltage for VCO, error amplifier, and the other digital controller is 1.8 V, and the supply voltage for regulated charge pump is 3.3V.

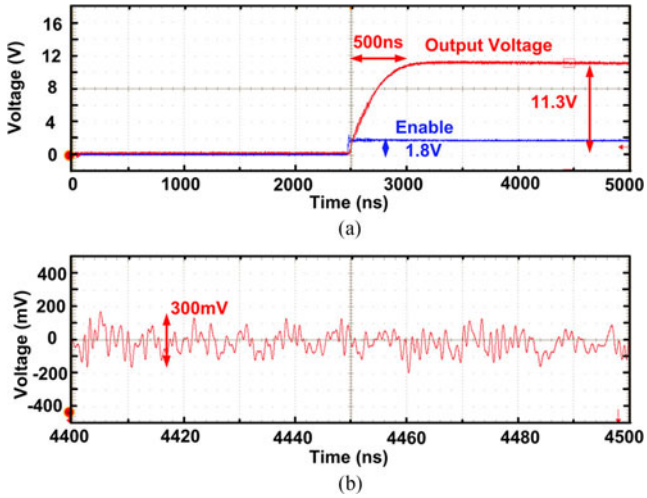

Fig. 9. When $D_0D_1D_2 = 111$ and loading current is 3 mA, (a) the measurement result of power on, (b) the voltage ripple at the output of charge pump.

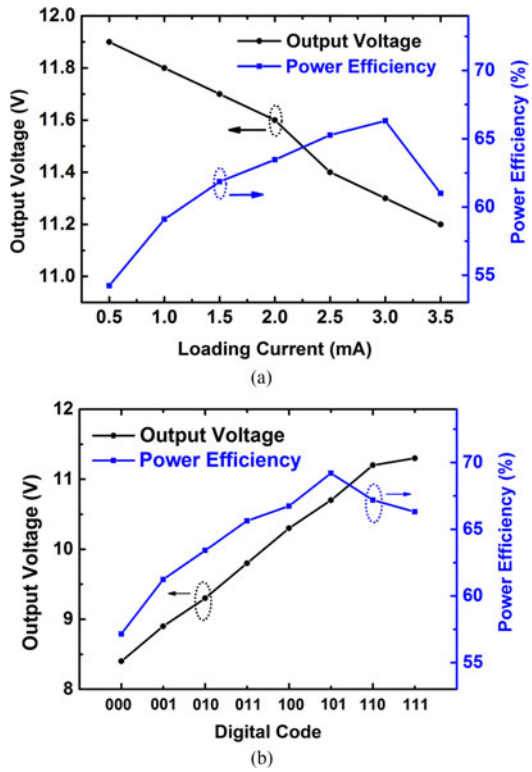

Fig. 10. (a) The output voltage and power efficiency of charge pump vs. the loading current when $D_0D_1D_2 = 111$. (b) The output voltage and power efficiency of charge pump when the loading current is 3 mA and digital code $(D_0D_1D_2)$ varies from 000 to 111.

A. Adaptive Dynamic Power Supply Measurement Results

The settling time, voltage ripple, and power efficiency of the regulated charge pump are evaluated under a variety of ideal current loads. Fig. 9 shows that the settling time and voltage ripple are ~500 ns and ~300 mV, respectively, when the loading current is 3 mA and $D_0D_1D_2 = 111$. Fig. 10(a) shows the output voltage and power efficiency of charge pump vs. the loading current when $D_0D_1D_2 = 111$. It shows that the power

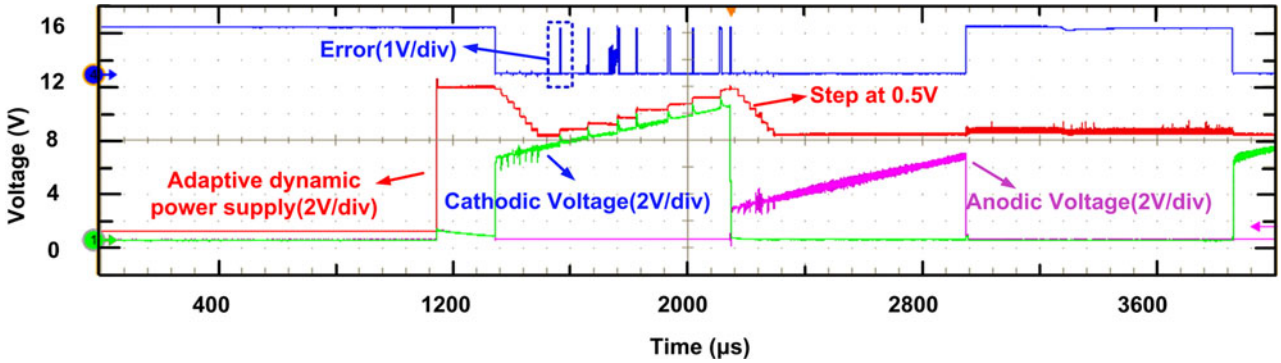

Fig. 11. The power supply self-adjusting procedure during stimulation when the stimulus current is 1.5 mA, R_S is 4 kΩ, and C_{DL} is 300 nF.

efficiency of the charge pump can be up to 67% under 3-mA loading current. Fig. 10(b) shows the output voltage and power efficiency of the charge pump when the loading current is 3 mA and digital code $(D_0D_1D_2)$ varies from 000 to 111.

Fig. 11 shows the power supply self-adjusting procedure during the stimulation. When the voltage drop across transistors M_{C3} and M_{C4} is less than 0.8 V, triode indicator outputs an "error" signal, and then the supply voltage steps up at 0.5 V promptly.

As described in (1), $V_{elec}(t)$ rises to $|I_{STIM}| \cdot R_S$ instantaneously once the stimulus current is applied. In order to keep up with the rising speed of electrode voltage at the very beginning of cathodic stimulation, the supply voltage is initially programmed to 12 V. And then, the supply voltage of the stimulator steps down one by one at 0.5 V in a defined interval until the "error" signal is detected. Once the "error" is detected, the supply voltage will step up with 0.5 V immediately until the "error" disappears. During stimulation, the operating region of the transistors in the cascode current mirror is continually monitored by the triode indicator and the digital controller. During the anodic stimulation phase, the power supply self-adjusting procedure is the same as that of the cathodic stimulation phase.

The overall power efficiency (η_{eff}) from the power source unit (Agilent B2902A) to the load is calculated as

$$\eta_{eff} = \frac{I_{\text{STIM}} \times V_{\text{supply,adap}}}{P_{total}} \tag{3}$$

where I_{STIM} is the stimulus current, $V_{supply,adap}$ is the supply voltage of the stimulator under the adaptive supply, and P_{total} is the overall average power consumed by stimulator under the fixed or adaptive supply, which is measured by Agilent B2902A at a 50 kS/s sample rate for a period of 2 seconds. For example, the consumed power of stimulator is 30.1 mW and 20.2 mW in the fixed and adaptive supply, respectively, under 2.5-mA stimulus current amplitude, 320-μs current pulse width, 640-μs current pulse period, 1–kΩ R_S, and 100-nF C_{DL}. It shows that the power consumption of stimulator can be greatly reduced by using adaptive supply. Fig. 12 compares the power efficiencies of the stimulator vs. the stimulus current between the fixed and adaptive mechanisms. The results show that the stimulator power efficiency with the adaptive supply control (49% ∼ 54%) is higher than that of the fixed supply (34% ∼ 37%).

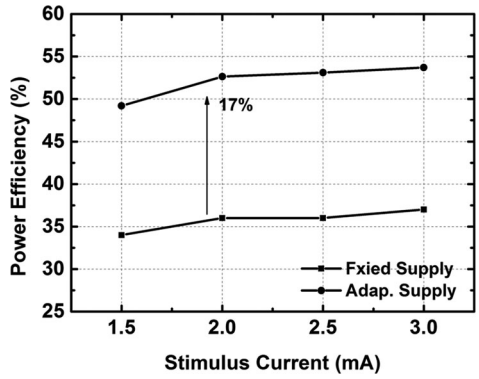

Fig. 12. The power efficiency of stimulator vs. stimulus currents between adaptive and fixed supplies when R_S is 1 kΩ and C_{DL} is 100 nF.

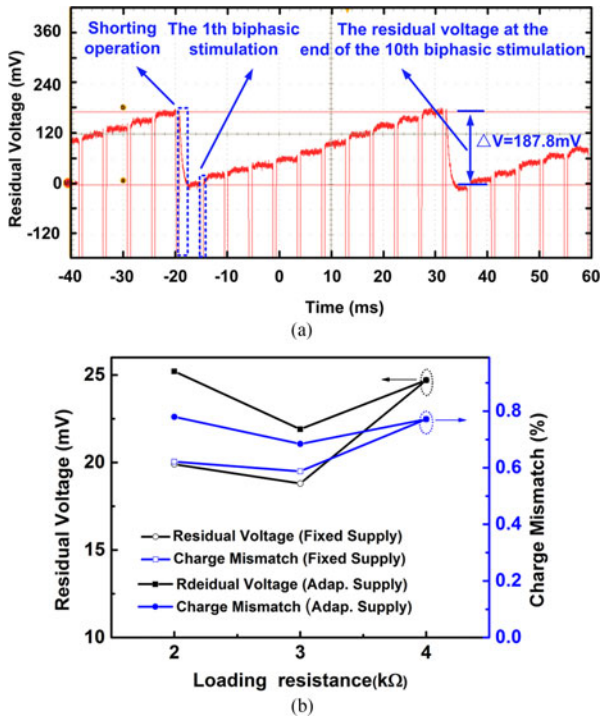

Fig. 13. (a) An oscilloscope capture of the residual voltage on the 100-nF Teflon capacitor at 2-mA stimulus current, which allows the measurements of the accumulated residual voltage at the end of the 10th biphasic stimulation. (b) Residual voltage and charge mismatch factor in one-cycle biphasic stimulus stimulation as the function of loading resistance at 2-mA stimulus current.

TABLE II
PERFORMANCE COMPARISON WITH THE PRIOR WORKS WITH DYNAMIC POWER SUPPLY TECHNIQUES

	TBioCAS 2012 [11]	TBioCAS 2011 [4]	JSSC 2013 [10]	TBioCAS 2013 [12]	This work
Technology	0.35-μm CMOS	1.5-μm CMOS	0.5-μm CMOS	0.18-μm 1.8-V/20-V CMOS	0.18-μm 1.8-V/3.3-V CMOS
Dynamic Range	0–450 μA	0–136 μA	0–2800 μA	0–504 μA	0–3000 μA
Voltage Compliance	3 V	1.75 V	4.6 V	11.5 V (6 V input voltage)	12 V (3.3 V input voltage)
Integrated Capacitance	n/A	n/A	n/A	1000 pF	400 pF
Monitoring Circuits	DAC-subtractor and Comparators	Reference and Comparators	Attenuator, Voltage Detector, and ADC	Reference and Four Comparators	PMOS Inverter
Ext. Components	Yes	Yes	Yes	No	No
Channels	1	15	4	8	16
Area	n/A	4.76 mm^2	2.25 mm^2	2.8 mm^2	3.5 mm^2

TABLE III
PERFORMANCE COMPARISON WITH THE EXISTING CHARGE PUMPS

	JSSC 2006 [21]	ISSCC 2014 [25]	JSSC 2015 [26]	JSSC 2003 [27]	This work
Technology	0.13-μm CMOS	0.16-μm CMOS	0.18-μm CMOS	0.18-μm CMOS	0.18-μm CMOS
Vin	3.3 V	3.3 V	1 V	1.8 V	3.3 V
Vout	4.5 V@30 mA	16 V@7 mA	3 V $\sim$ 6 V	5 V $\sim$ 6 V	11.3 V@3 mA
Output Current	1 $\sim$ 30 mA	0.1 $\sim$ 7 mA	0.03 $\sim$ 0.24 mA	0.2 $\sim$ 0.4 mA	0.5 $\sim$ 3.5 mA
Switching Frequency	400 kHz $\sim$ 600 kHz	6.67 MHz	10 kHz $\sim$ 20 MHz	100 MHz	7 MHz $\sim$ 50 MHz
Flying Cap	SMD Ext. 2 μF +330 nF $\times$ 2	SMD Ext. 1 μF $\times$ 2 +100 nF+220 nF	MIMCAP +MOSCAP	MIMCAP	MIMCAP Integrated 400 pF
Peak Efficiency	70% $\sim$ 75%	70%	48% $\sim$ 58%	46% $\sim$ 56%	69%
Output Ripple (Relative to the output voltage)	0.75% (with 2000-nF load capacitor)	1% (with 100-nF load capacitor)	1.3% @ 3 V, 0.6%@6 V	n/A	2.6% (with 0.1-nF load capacitor)

B. Residual Voltage and Charge Mismatch

The stimulus current is programmed by the 3-bit current DAC. The size of LSB of the 3-bit current DAC is set to 500 μA. Fig. 13(a) shows an oscilloscope capture of the residual voltage on the 100-nF Teflon capacitor at 2-mA stimulus current. The electrodes are both short-circuited to the ground once every 10 cycles of the biphasic stimulation for the purpose of precise measurement. The accumulated residual voltage at the end of the 10th biphasic stimulation under the fixed power supply is 187.8 mV. It means that the injected charge in one-cycle biphasic stimulation is $2000\,\mu\text{A} \times 160\,\mu\text{s} = 320\,\text{nC}$, and results in charge error of $18.78\,\text{mV} \times 100\,\text{nF} = 1.88\,\text{nC}$. Thus, the charge mismatch is $1.88\,\text{nC}/320\,\text{nC} = 0.58\%$. Fig. 13(b) compares the residual voltage on the loading capacitor C_{DL} and the charge mismatch vs. the loading resistance between the fixed and the adaptive mechanisms. The performance of charge balance degrades slightly under the adaptive power supply. The maximal accumulated residual voltage in one-cycle biphasic stimulation is $\sim$25 mV. In [9], an additional reduction of the residual charge at least 1/180 can be achieved by following the biphasic stimulation with shorting operation. The residual average dc current is the residual charge after shorting operation and divided by the pulse interval, which is calculated as $2.5\,\text{nC}/180/1\,\text{ms} = 14\,\text{nA}$.

C. Performance Comparison with Prior Works

Table II summarizes the performances of the proposed stimulator relative to the prior works. The experimental results show that the new proposed dynamic power supply technique employed on a multi-channel CCS can greatly improve the power efficiency of stimulator. The silicon area of the 12V-tolerant stimulator with adaptive regulated charge pump, realized in a 0.18-μm 1.8-V/3.3-V CMOS process, is 3.5 mm^2. Table III summarizes the key specifications of the proposed charge pump relative to the existing charge pumps. The proposed regulated charge pump, without any external components, can achieve an output current of up to 3.5 mA. The peak power efficiency of charge pump is 69%.

D. Animal Test

Animal trials have been performed, and all experimental procedures have been reviewed and approved by the Department of Mechanical Engineering College of Engineering of National Taiwan University, Taiwan. Fig. 14(a) shows the guinea-pig with the electrodes for detection and stimulation, and Fig. 14(b) shows the measurement setup for animal test [23], [24]. The stimulus current of the pulse train with $\pm$1.5-mA amplitude, 100-μs pulse width, 40-ms period, and 1-s duration is used to elicit the corresponding neural response of the guinea-pig. Fig. 15 shows the measured ABR (auditory brainstem evoked response) result. The stimulus driver can successfully elicit the corresponding neural response with the waveform transition marked as I $\sim$ V in Fig. 15.

Based on the experiment results, the functionalities of the proposed stimulator have been successfully verified.

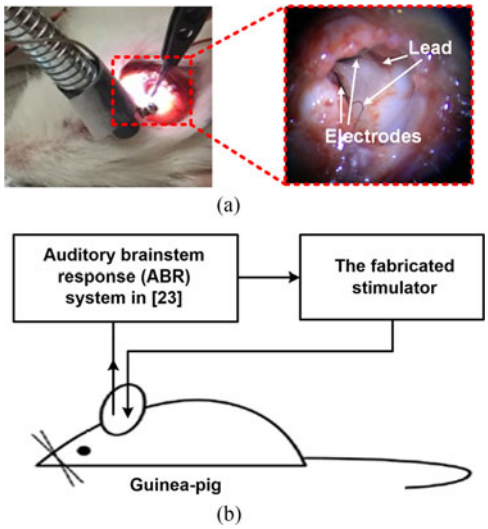

Fig. 14. (a) The guinea-pig with electrodes for detection and stimulation. (b) Measurement setup for animal test [23].

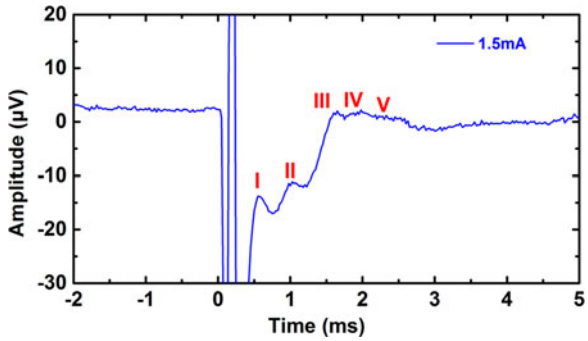

Fig. 15. The measured ABR (auditory brainstem evoked response) result.

V. Conclusion

A 16-channel 12V-tolerant stimulator has been designed and successfully verified in a 0.18-μm 1.8-V/3.3-V CMOS process. It can be fully integrated with the microcontroller or the biomedical signal processor into an SoC chip fabricated in a low-voltage CMOS technology. The experimental results have shown that the proposed new digitally dynamic power supply technique for multi-channel CCS can greatly improve the power efficiency. The charge mismatch is less than 0.8%, and the residual dc current is less than 14 nA with shorting operation. The reliability measurement of up to hundreds of millions biphasic stimulus cycles in 30 days has been done. It has been successfully verified that the proposed high-voltage-tolerant stimulator is robust, and the performance of charge balance does not degrade.

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