Regulated Charge Pump With New Clocking Scheme for Smoothing the Charging Current in Low Voltage CMOS Process

Zhicong Luo, *Student Member, IEEE*, Ming-Dou Ker, *Fellow, IEEE*, Wan-Hsueh Cheng, and Ting-Yang Yen

***Abstract*— A regulated cross-couple charge pump with new charging current smoothing technique is proposed and verified in a 0.18-μm 1.8-V/3.3-V CMOS process. The transient behaviors of 3-stage cross-couple charge pump and the expressions for the charging current are described in detail. The experiment results show that the charging current ripples are reduced by a factor of three through using the proposed new clocking scheme. The voltage ripples in the power supply line, which is connected with the charge pump input, are also smoothed greatly as the filter circuit does. The proposed scheme is used to decrease the smoothing capacitance in the power line of charge pump for reducing the size of implantable devices in biomedical application. In addition, the power efficiency is improved. The proposed cross-couple charge pump can provide 10.5-V output voltage with 3.5-mA output current, and the power efficiency of the charge pump can be up to 69%.**

***Index Terms*— Charge pump, charging current ripples, high-voltage-tolerant, peak current, power efficiency, transient behaviors.**

I. Introduction

ELECTRICAL stimulation had been generally used to recover some physical functions of human beings, such as epileptic-suppression prosthesis [1], [2], proprioceptive prosthesis [3], and retinal prosthesis [4], [5]. The required supply for the electrical stimulation varies from a few volts to tens volts in various applications, e.g. the high voltage generator for epileptic-suppression prosthesis should provide at least 12-V voltage supply [6]. In addition, the off-chip devices of the implantable devices should be eliminated as possible for reducing the size of device.

The issues in the conventional charge pump circuits, such as body effect, gate-reliability issues [7], threshold voltage drop, and return-back leakage current [8], had been widely studied. But, the charging current of the conventional charge pump is the power exponent function of time. A filter or smoothing circuit is needed in the power line to smooth the charging current. In the simplest form, this can be a capacitor placed across power supply line. Therefore, the size of the implantable device is disadvantageously increased. The problem is worsen for wireless powered implantable devices, because the energy from wireless power system is limited [9], [10]. In order to produce a steady DC voltage for charge pump, a large smoothing capacitance in the power line is needed. If the peak charging current of charge pump is reduced, the smoothing capacitance in the power line can be decreased. Therefore, the size of the implantable device decreases. In addition, reducing the charging current peaks can enhance the transient response of the front power source (e.g., LDOs), reduce the transient noise in the power supply line, and improve the electromagnetic emission (EME) behavior of the implantable devices. In [11], the EME can be reduced up to 20 dB by reducing the charging current peaks by a factor of three.

This work proposed a new charge pump with phase-shifted clocks. Compare to the conventional high-voltage charge pump system, this high-voltage-tolerant charge pump can smooth the charging current by using new clocking scheme, instead of using the filter capacitor. The experimental results show that the proposed new phase-shifted clocks for charge pump can smooth the charging current ripple with a factor of three. More still, the power efficiency is improved.

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II. Transient Behaviors Analysis for Cross-Couple Charge Pump

A. Expressions for Charging Current of Cross-Couple Charge Pump Without Phase-Shifted Clocks

Fig. 1(a) shows the proposed 3-stage cross-couple charge pump, which can generate the high voltage without the electrical overstress and gate-oxide reliability issues [12], [13]. The conventional clock scheme for charge pump is shown in Fig. 1(b). When the clock signals (clkbu_1, clkbu_2, clkbu_3, and clkbu_4) are logic 0, transistors (M_{E1} to M_{E9}) are turned on, and the other transistors in the circuit are turned off. There are four charging current paths flowing out from the power source to the charge pump, which are indicated by the dotted line in Fig. 1(a). In order to analyze and calculate those charging currents for simplicity, the following assumptions are made.

1) Each pumping capacitor and transistor has the same value of C_E and on-resistance R_{on}, respectively.
2) Each stage charge pump is driven by 2-phase clock with the cycle of T seconds.

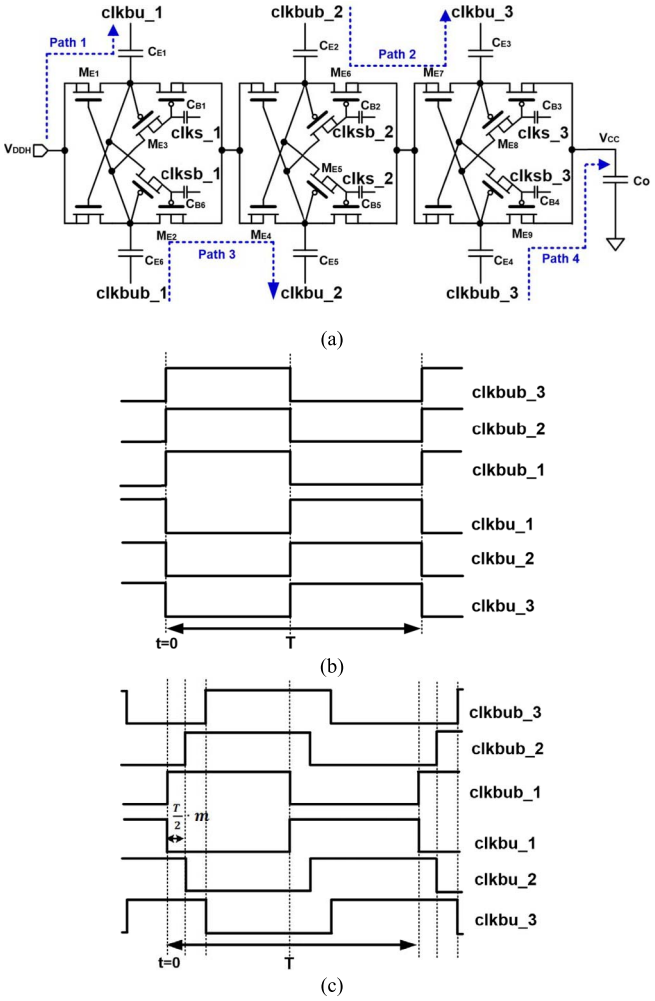

Fig. 1. (a) Detailed schematic of the 3-stage charge pump. (b) Clocking schemes for charge pump without phase-shifted clocks. (c) Clocking schemes for charge pump with phase-shifted clocks.

3) The parasitic capacitance of the pumping capacitor is negligibly small compared with the pumping capacitance, and the pumping inverters have negligibly small on-resistance.
4) The various sources of power loss in the charge pump, such as the conduction loss, the switching loss, and the reversion loss, are negligibly small.
5) Defining $t = 0$ at one of the falling edges of the clock signal clkbu_1, this is indicated in Fig. 1(b).

The equivalent circuit for path 1 is shown in Fig. 2(a), which is a type first-order RC circuit in the textbooks, the charging current $i_1(t)$ in path 1, during $0 \le t < T/2$, can be expressed as

$$i_1(\mathrm{t}) = \mathrm{C}_{E1} \cdot \left(V_{DDH} - V_{C_{E1}}\left(0^-\right)\right)\left(\frac{1}{R_{on} \cdot \mathrm{C}_{E1}}\right) \cdot e^{-\frac{t}{R_{on} \cdot C_{E1}}}, \tag{1}$$

where $V_{C_{E1}}(0^-)$ is the voltage on capacitor C_{E1} in the ending of the latest half pumping cycle before $t = 0$. Referring to [11], the output voltage (V_{out}) of a n-stages positive charge

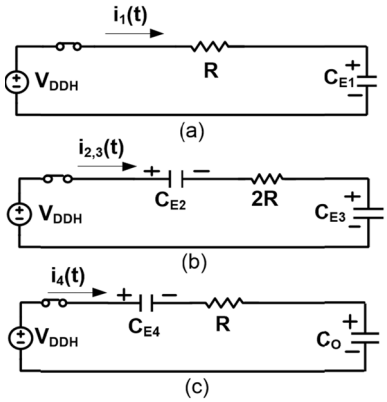

Fig. 2. Simplified equivalent circuits for (a) path 1, (b) path 2 and path 3, and (c) path 4, at the falling edge (t = 0) of the clock signals (clkbu_1, clkbu_2, clkbu_3, and clkbu_4), respectively.

can be approximately expressed as

$$V_{out} = V_{DDH} + n \cdot \left(\frac{V_{DDH} \cdot C_E}{C_{E+C_B+C_{par}}} - \frac{T \cdot I_{out}}{2 \cdot C_E} - R_{on} \cdot I_{out}\right) \tag{2}$$

where $\mathrm{V_{DDH}}$ is supply voltage used as the input voltage at the charge pump input. C_E, C_B, and C_{par} are the pump capacitance, the boost capacitance, and the parasitic capacitances of the pump capacitor in circuit, respectively. I_{out} is the output current. In the ending of the latest half pumping cycle before $t = 0$, the clock clkbu_1 switches from the logic high level to the logic low level. Thus

$$V_{C_{E1}}\left(0^-\right) = \left[V_{DDH} + \left(V_{DDH} \cdot \frac{C_{E1}}{C_{E1+C_{B1}+C_{par}}} - \frac{T \cdot I_{out}}{2 \cdot C_{E1}} - R_{on} \cdot I_{out}\right)\right] - V_{DDH}. \tag{3}$$

In (3), the first item represents the output voltage of one-stage (the first stage) of charge pump, and the second item represents the effects which are resulted from the switching (from V_{DDH} to 0) of clock clkbu_1. C_{par} and C_{B1} are negligibly smaller than C_{E1}, and the effect of $R_{on} \cdot I_{out}$ is neglected for simplicity, $V_{C_{E1}}(0^-)$ is approximately expressed as

$$V_{C_{E1}}\left(0^-\right) = V_{DDH} - \frac{T \cdot I_{out}}{2 \cdot C_E}. \tag{4}$$

Define $a(t)$ and ε as

$$a\,(t) = e^{-t/R_{on} \cdot \mathrm{C}_E} \tag{5}$$

$$\varepsilon = \frac{T \cdot I_{out}}{2 \cdot R_{on} \cdot \mathrm{C}_E}. \tag{6}$$

Substituting (4), (5), and (6) into (1), the charging current $i_1(\mathrm{t})$ in path 1 can be expressed as

$$i_1\,(\mathrm{t}) = \varepsilon \cdot a\,(t)\,. \tag{7}$$

The equivalent circuits for path 2 and 3 are shown in Fig. 2(b). Kirchhoff's voltage law for this RC circuit, during $0 \le t <$ T/2, can be expressed as

$$V_{DDH} - V_{C_{E2}}\,(t) - V_{C_{E3}}\,(t) - i_2\,(t) \cdot 2 \cdot R_{on} = 0 \tag{8}$$

where $i_2(t)$ is the charging current in path 2, $V_{C_{E2}}(t)$ and $V_{C_{E3}}(t)$ are the transient voltages on the capacitors C_{E2} and C_{E3}, respectively. Charge conservation equation for the capacitors (C_{E2} and C_{E3}) in the circuit can be expressed as

$$C_{E2}\cdot V_{C_{E2}}(t) - C_{E3}\cdot V_{C_{E3}}(t) = C_{E2}\cdot V_{C_{E2}}\left(0^-\right) - C_{E3}\cdot V_{C_{E3}}\left(0^-\right). \quad (9)$$

The current through the capacitors (C_{E2} and C_{E3}) can be expressed as

$$i_2(\mathrm{t}) = C_{E2}\cdot\frac{dV_{C_{E2}}(t)}{dt} = C_{E3}\cdot\frac{dV_{C_{E3}}(t)}{dt}. \quad (10)$$

With (8), (9), and (10), the solutions for $i_2(t)$, $V_{C_{E2}}(t)$, and $V_{C_{E3}}(t)$, during $0 \le t < \mathrm{T}/2$, can be expressed as

$$i_2(\mathrm{t}) = b(t)\cdot C_{E3}\cdot\left[V_{DDH} - V_{C_{E3}}\left(0^-\right) - V_{C_{E2}}\left(0^-\right)\right] \quad (11)$$

$$V_{C_{E2}}(t) = c(t)\cdot\left[V_{DDH} - V_{C_{E3}}\left(0^-\right) - V_{C_{E2}}\left(0^-\right)\right] + V_{C_{E2}}\left(0^-\right), \quad (12)$$

$$V_{C_{E3}}(t) = d(t)\cdot\left[V_{DDH} - V_{C_{E3}}\left(0^-\right) - V_{C_{E2}}\left(0^-\right)\right] + V_{C_{E3}}\left(0^-\right) \quad (13)$$

where

$$b(t) = \frac{1}{2}\cdot\frac{1}{R_{on}\cdot \mathrm{C}_E}\cdot e^{-\frac{t}{\tau}} \quad (14)$$

$$c(t) = \frac{\mathrm{C}_{E2}}{\mathrm{C}_{E2}+\mathrm{C}_{E3}}\cdot\left(1-e^{-\frac{t}{\tau}}\right) = \frac{1}{2}\cdot\left(1-e^{-\frac{t}{\tau}}\right) \quad (15)$$

$$d(t) = \frac{\mathrm{C}_{E3}}{\mathrm{C}_{E2}+\mathrm{C}_{E3}}\cdot\left(1-e^{-\frac{t}{\tau}}\right) = \frac{1}{2}\cdot\left(1-e^{-\frac{t}{\tau}}\right) \quad (16)$$

$$\tau = 2\cdot R_{on}\cdot\frac{C_{E2}\cdot C_{E3}}{C_{E2}+C_{E3}} = R_{on}\cdot C_E. \quad (17)$$

And $V_{C_{E2}}(0^-)$ and $V_{C_{E3}}(0^-)$ are the initial voltages on capacitor C_{E2} and C_{E3} at $t = 0$, respectively. Referring to (2), $V_{C_{E2}}(0^-)$ can be approximately expressed as

$$V_{C_{E2}}\left(0^-\right) = -\left(2\cdot V_{DDH} - \frac{T\cdot I_{out}}{2\cdot C_E}\right). \quad (18)$$

Referring to (3), $V_{C_{E3}}(0^-)$ can be approximately expressed as

$$V_{C_{E3}}\left(0^-\right) = 3\cdot V_{DDH} - \frac{3\cdot T\cdot I_{out}}{2\cdot C_E}. \quad (19)$$

Substituting (14), (17), (18), and (19) into (11), i_2(t) can be rewritten as

$$i_2(\mathrm{t}) = T\cdot I_{out}\cdot b(t) = \varepsilon\cdot a(t). \quad (20)$$

On the same principle, i_3(t) in path 3 and i_4(t) in path 4, during $0 \le t < \mathrm{T}/2$, can be expressed as

$$i_3(\mathrm{t}) = \varepsilon\cdot a(t) \quad (21)$$

$$i_4(\mathrm{t}) = \varepsilon\cdot e(t). \quad (22)$$

where

$$e(t) = e^{-\frac{t}{\tau 1}}, \quad (23)$$

$$\tau 1 = R_{on}\cdot\frac{C_{E4}\cdot C_O}{C_{E4}+C_O} = R_{on}\cdot\frac{C_E\cdot C_O}{C_E+C_O}. \quad (24)$$

With (7), (20), (21), and (22), the total charging current, during $0 \le t < \mathrm{T}/2$, can be expressed as

$$i_{total,conv}(\mathrm{t}) = \varepsilon\cdot[3\cdot a(t) + e(t)]. \quad (25)$$

The total charging current $i_{total,conv}(t)$ in (25) can be periodically extended to the whole operating range by defining $a(t)$ and $e(t)$ as

$$a(t) = a\left(t + n\cdot\frac{T}{2}\right). \quad (26)$$

$$e(t) = e\left(t + n\cdot\frac{T}{2}\right). \quad (27)$$

Equation (25) shows that the total charging current decreases exponentially with time, the maximum charging current appears at $t = 0$. The maximum charging current can be expressed as

$$i_{total,conv}(0) = 4\cdot\varepsilon. \quad (28)$$

B. Expressions for Charging Current of Cross-Couple Charge Pump with Phase-Shifted Clocks

The new clocking scheme with phase-shifted clocks for charge pump is shown in Fig. 1(c). In Fig. 1(c), the clock signals are separated to each other by a time delay of $(\frac{T}{2}\cdot m)$ seconds, which means that the charge pump stages are started up one stage by one stage with a delay, where $0 < m < \frac{1}{2}$. The total charging current can be expressed as

$$i_{total,new}(t) = i_{11}(t) + i_{12}(t) + i_{23}(t) + i_{44}(t), \quad (29)$$

where $i_{11}(t)$ is the charging current flowing from power supply (V_{DDH}) to the first-stage pumping capacitor (C_{E1} or C_{E6}). $i_{12}(t)$ is the charging current flowing from the first-stage pumping capacitor (C_{E1} or C_{E6}) to the second-stage pumping capacitor (C_{E2} or C_{E5}). $i_{23}(t)$ is the charging current flowing from the second-stage pumping capacitor (C_{E2} or C_{E5}) to the third-stage pumping capacitor (C_{E3} or C_{E4}). And $i_{44}(t)$ is the charging current flowing from the third-stage pumping capacitor (C_{E3} or C_{E4}) to the output capacitor (C_o). Referring to (11), $i_{12}(t)$, during $0 \le t < \mathrm{T}/2$, can be expressed as

$$i_{12}(t) = \begin{cases} \frac{\varepsilon\cdot a(t)}{2\left[1-c\left(\frac{T}{2}\cdot m\right)\right]}. & \left(\text{for } 0 \le t < \frac{T}{2}\cdot m\right) \\ \frac{\varepsilon\cdot a(t)\cdot\left[2-3\cdot c\left(\frac{T}{2}\cdot m\right)\right]}{2\cdot a\left(\frac{T}{2}\cdot m\right)\cdot\left[1-c\left(\frac{T}{2}\cdot m\right)\right]}. & \left(\text{for}\frac{T}{2}\cdot m \le t < \frac{T}{2}\right) \end{cases} \quad (30)$$

$i_{23}(t)$, during $0 \le t < \frac{T}{2}\cdot m$, can be expressed as

$$i_{23}(t) = \begin{cases} \frac{\varepsilon\cdot a(t)\cdot\left[2-3\cdot c\left(\frac{T}{2}\cdot m\right)\right]\cdot a\left(\frac{T}{2}(1-2\cdot m)\right)}{2\cdot\left(1-c\left(\frac{T}{2}\cdot m\right)\right)}. & \left(\text{for}0 \le t < \frac{T}{2}\cdot m\right) \\ \frac{\varepsilon\cdot a(t)}{2\cdot a\left(\frac{T}{2}\cdot m\right)\cdot\left[1-c\left(\frac{T}{2}\cdot m\right)\right]}. & \left(\text{for}\frac{T}{2}\cdot m \le t < \mathrm{T}\cdot m\right) \\ \frac{\varepsilon\cdot a(t)\cdot\left[2-3\cdot c\left(\frac{T}{2}\cdot m\right)\right]}{2\cdot a(\mathrm{T}\cdot m)\cdot\left[1-c\left(\frac{T}{2}\cdot m\right)\right]} & \left(\text{for } \mathrm{T}\cdot m \le t < \frac{T}{2}\right) \end{cases}. \quad (31)$$

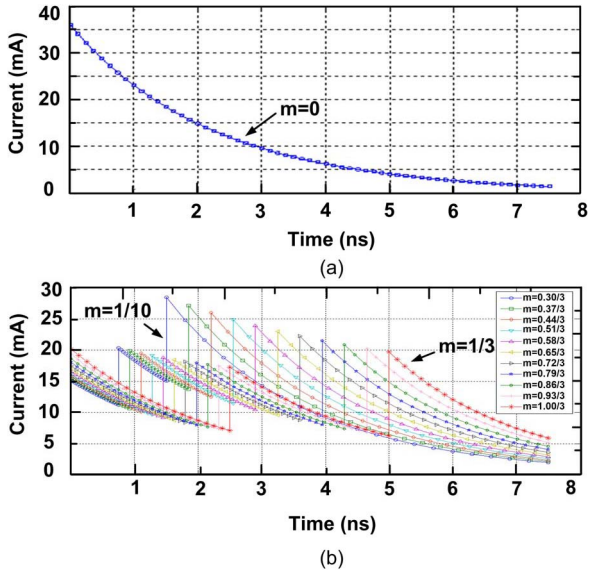

Fig. 3. Let $R_{on} = 50\Omega$, $C_E = 50$ pF, T =15 ns, and $C_o = 100$ pF. (a) Curve of $i_{total,conv}(t)$ when m = 0. (b) Curve of $i_{total,new}(t)$ when m varies from 1/10 to 1/3, m = 1/3 is the best case.

With (7) and (22), $i_{11}(t)$ and $i_{44}(t)$ can be approximately expressed as

$$i_{11}(t) = \varepsilon \cdot a(t). \quad \left(\text{for} 0 \le t < \frac{T}{2}\right) \tag{32}$$

$$i_{44}(t) = \begin{cases} \varepsilon \cdot e\left(t + \frac{T}{2}(1 - 2 \cdot m)\right). & (\text{for } 0 \le t < T \cdot m) \\ \varepsilon \cdot e\left(t - T \cdot m\right). & \left(\text{for } T \cdot m \le t < \frac{T}{2}\right). \end{cases} \tag{33}$$

Defining the current ripple attenuation factor g as

$$g = \frac{max\left(i_{total,conv}(t)\right) - min\left(i_{total,conv}(t)\right)}{max\left(i_{total,new}(t)\right) - min\left(i_{total,new}(t)\right)} \tag{34}$$

where $max(i_{total,conv}(t))$, $max(i_{total,new}(t))$, $min(i_{total,conv}(t))$, and $min(i_{total,new}(t))$ are the maximal charging currents and minimum charging currents in the whole operating range without and with phase-shifted clock, respectively. Substituting (25) and (29) into (34), g is the function of m, T, R_{on}, C_o, and C_E. In order to find the relationship between the factor g, phase-shifted factor m, pumping cycle T, τin (17), and $\tau 1$ in (24), defining h as

$$h = \frac{T}{\tau}. \tag{35}$$

Let $R_{on} = 50\,\Omega$, $C_E = 50$ pF, $T = 15$ ns, and $C_o = 100$ pF, The curves of $i_{total,conv}(t)$ and $i_{total,new}(t)$ are shown in Fig. 3, respectively. In Fig. 3(b), it can be found that the charging current is smoothed by a factor of two when m is 1/3. Fig. 4 is a 3-D graph that shows the variation of g as the factor m is swept from 0 to 1/2 and h is changed from 1 to 15. The maximum g is ~ 2.3 when m is 1/3 and h varies from 3 to 9. When $h \ge 10$, the analytic results indicate that m, where the maximum $g$can be obtained, becomes smaller as h becomes larger. For example, when $h = 15$, the maximum g is 2.17 as m is 0.21. Intuitively, m = 1/3 could be the best case, because the clock phases are distributed evenly. The peak of charging current with m = 0 is split averagely into three peaks with m = 1/3, as shown in Fig. 3.

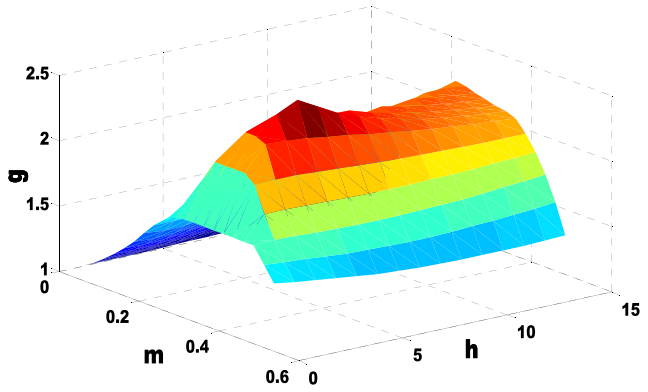

Fig. 4. When $R_{on} = 50\ \Omega$, $C_E = 50$ pF, and $C_o = 100$ pF. The variation of g as the factor m is swept from 0 to 1/2 and h is changed from 1 to 15.

III. Circuit Implementation and Experimental Results

A. Circuit Implementation

The proposed new regulated charge pump, shown in Fig. 5, consists of voltage divider, error amplifier, voltage control oscillator (VCO), phase-shifted clock generator, level shifter, 4-phase clock generator, and 3-stage charge pump. PFM feedback network is used to generate the regulated high output voltage V_{CC}. The output voltage (V_{ctrl}) of the error amplifier is decided by the difference voltage between V_{FB} and V_{REF}. The clock frequency of clkl is controlled by V_{ctrl}. When V_{CC} is lower than the predefined voltage, V_{ctrl} becomes higher and the frequency of clkl arises until V_{CC} equals to the predefined voltage. In contrast, the frequency of clkl becomes slower when V_{CC} is higher than the predefined voltage. The 3-stage charge pump, shown in Fig. 1(a), is driven by the 4-phase clock for eliminating the return-back leakage current. The circuit of voltage-controlled oscillator (VCO) is shown in Fig. 6(a). Five inverters are attached in a chain, and the output of the last inverter is fed back into the first inverter. The proposed phase-shifted clock generator is shown in Fig. 6(b). The output of VCO is firstly divided down by the frequency divider of six. Then, the clocks are separated to each other by the D flip-flops. The level shifters convert the clocks from low voltage to high voltage. When control signal V_{ctrlp} is logic 1, the output clock signals (clkd_1, clkd_2 and clkd_3) are separated to each other by a time delay of $\frac{T}{6}$ seconds ($m = 1/3$) as shown in Fig. 1(c). In this way, the maximum g in (34) can be obtained as described in the theoretical analysis. When control signal V_{ctrlp} is logic 0, the output clock signals (clkd_1, clkd_2 and clkd_3) will be not shifted as shown in Fig. 1(b). Fig. 7 shows the detailed schematic of the 4-phase clock generator for reducing the return-back leakage current.

B. Experimental Results

The proposed new charge pump with PFM feedback network has been fabricated in a 0.18-μm 1.8-V/3.3-V CMOS process. Charge pump, shown in Fig. 1(a), is realized with MIM capacitors, PMOS transistors, and NMOS transistors

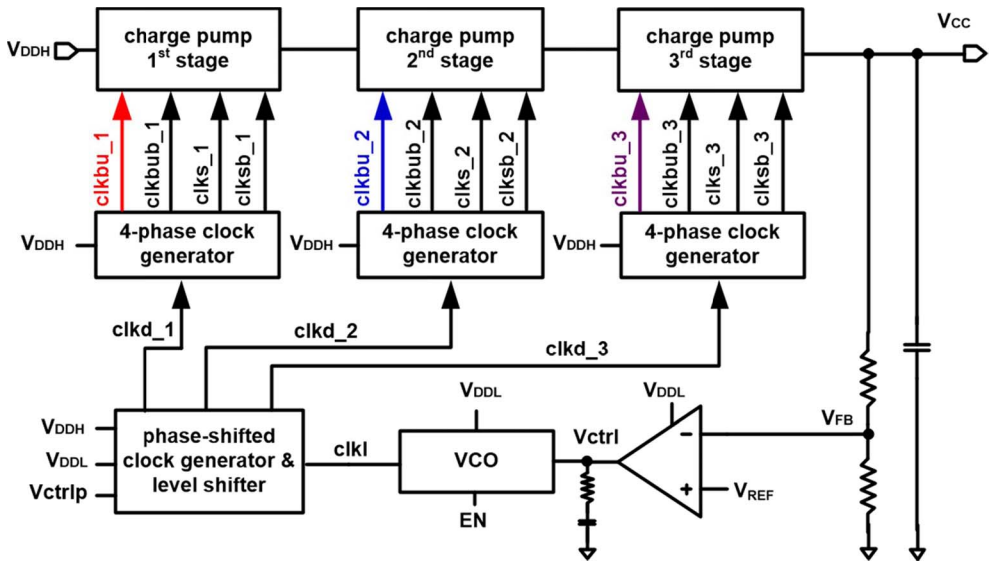

Fig. 5. The new regulated charge pump with phase-shifted clocks.

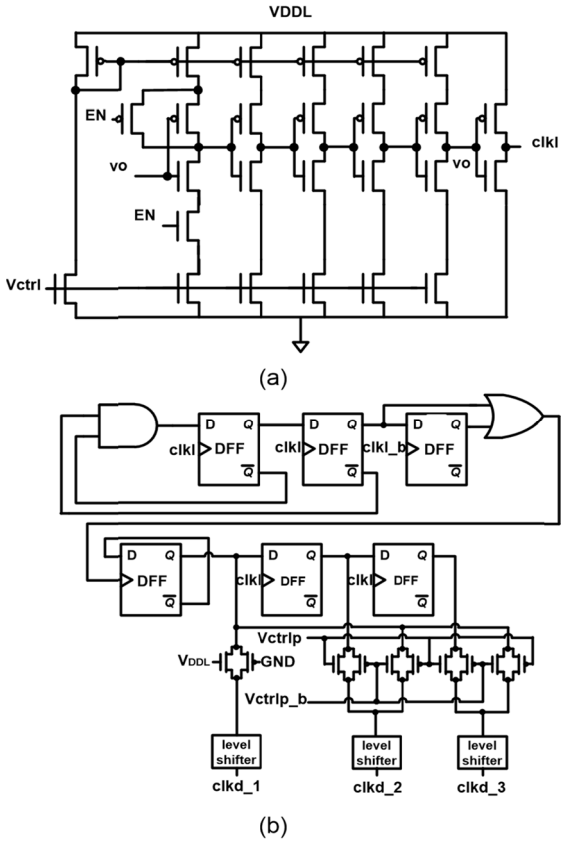

Fig. 6. (a) Detailed circuit of VCO. (b) Detailed circuit of the phase-shifted clock generator and level shifter, signal clkl is provided by VCO.

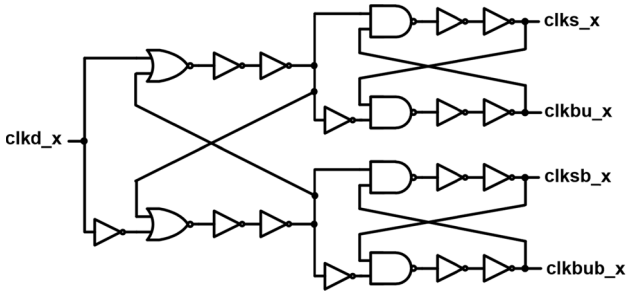

Fig. 7. Detailed schematic of the 4-phase clock generator, where x represents 1, 2, and 3, respectively.

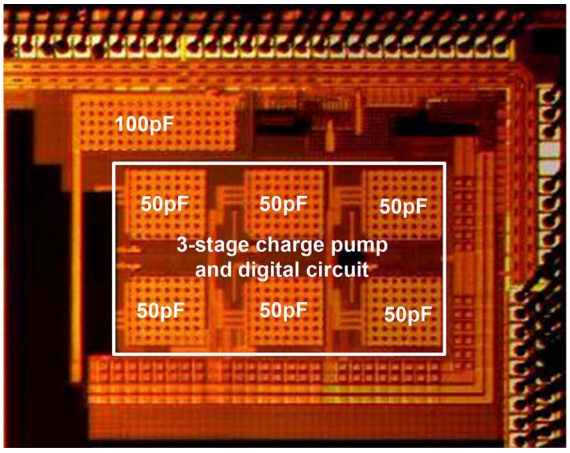

Fig. 8. Die photo of the fabricated charge pump.

with deep-nwell layer. The pumping capacitors (C_E) of the charge pump are 50 pF, and the output capacitor (C_O) is 100 pF. The die photo is shown in Fig. 8.

Fig. 9 shows the measurement result of power-on time at 3.5-mA loading current when V_{ctrlp} is logic 1, the power-on time is about 500 ns. Fig. 10 shows the setup for measuring the charging current (I_{VDDH}), where V_{DDL} is 1.8V, and V_{DDH2} is 3.3 V. The differential voltage across the 10-Ω resistor is measured by the oscilloscope (MSO5104) from Tektronix. Fig. 11 shows that the measured clock signals (clkd_1, clkd_2, and clkd_3) are separated to each other with a time delay (T/6) when V_{ctrlp} is logic 1. In addition, it can be clearly found that the operating clocks slow down when V_{ctrlp} changes from logic 0 to logic 1, which means that the power efficiency

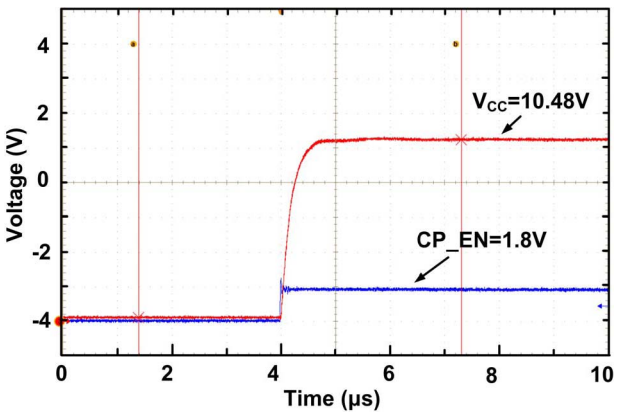

Fig. 9. Measurement result of power on at 3.5-mA loading current.

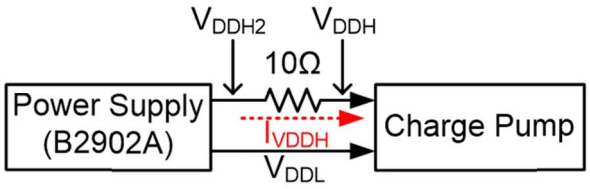

Fig. 10. Measurement setup for measuring I_{VDDH}.

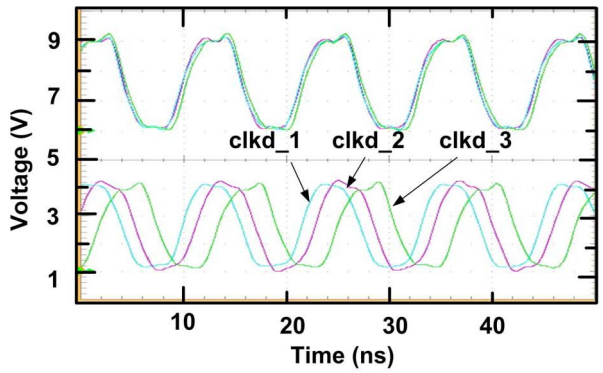

Fig. 11. Measured waveforms of clkd_1, clkd_2, and clkd_3 at 3.5-mA loading current. The upside of the figure shows the clocking scheme (87.1 MHz) when V_{ctrlp} is logic 0, and the downside of the figure shows the new clocking scheme (86.1 MHz) when V_{ctrlp} is logic 1. It can be found that the operating clocks slow down when V_{ctrlp} changes from logic 0 to logic 1.

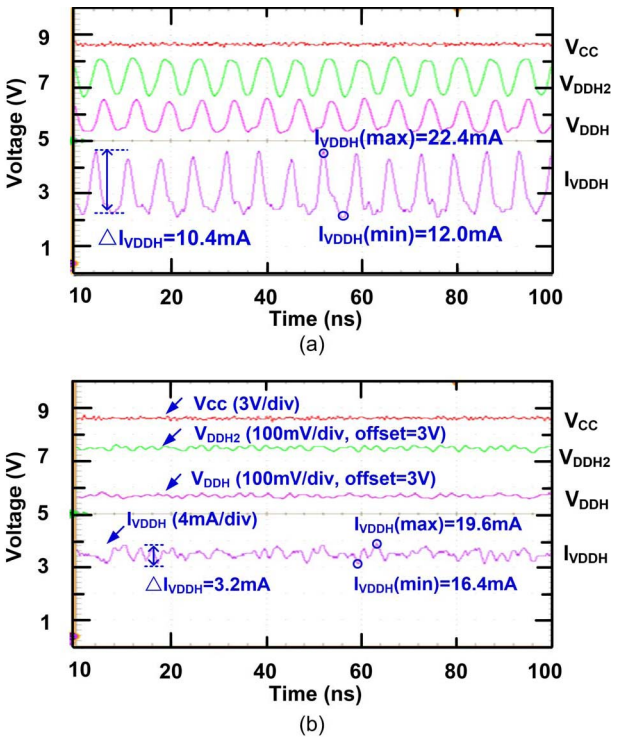

Fig. 12. Measured results of the charging current (I_{VDDH}) from V_{DDH} at 3-mA loading current. (a) V_{ctrlp} is logic 0. (b) V_{ctrlp} is logic 1. The voltage scale and offset of each voltage waveform in (a) are the same as that in (b).

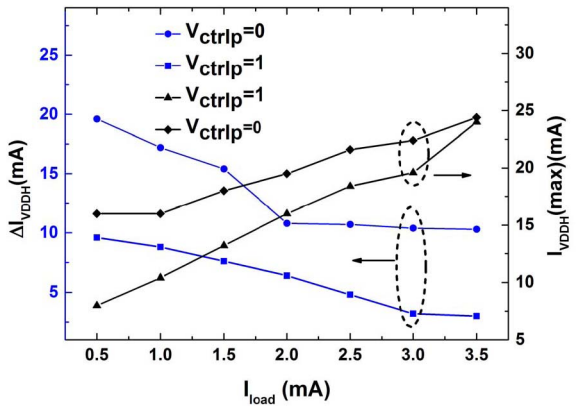

Fig. 13. The I_{VDDH}(max) and $\triangle I_{VDDH}$ versus the loading currents between the phase-shifted clocks ($V_{ctrlp} = 1$) and the fixed clocks ($V_{ctrlp} = 0$).

of charge pump is improved. Fig. 12 shows the measured charging current (I_{VDDH}) from power supply at 3-mA loading current. In Fig. 12(a), V_{ctrlp} is logic 0, the maximum charging current (I_{VDDH}(max)) and the minimum charging current (I_{VDDH}(min)) are 22.4 mA and 12.0 mA, respectively. In Fig. 12(b), V_{ctrlp} is logic 1, I_{VDDH}(max) and I_{VDDH}(min) are 19.6 mA and 16.4 mA, respectively. The charging current ripple ($\triangle I_{VDDH}$) is reduced by a factor of three by using the phase-shifted clocks. The ripple voltage at node V_{DDH}had been smoothed greatly by using the new clocking scheme. In other word, a virtual smoothing circuit has been placed at the power line.

Fig. 13 shows I_{VDDH}(max) and $\triangle I_{VDDH}$ vs. the loading currents between the phase-shifted clocks ($V_{ctrlp} = 1$) and fixed clocks ($V_{ctrlp} = 0$). It shows that the peak charging current and the ripples of the charging current are smoothed by the new clocking scheme.

The power efficiency of the charge pump is defined as

$$\eta_{eff} = \frac{P_{VCC}}{P_{VDDL} + P_{VDDH}} \tag{36}$$

where P_{VCC} is calculated as V_{CC} multiply by the loading current, and P_{VDDL} and P_{VDDH} are the overall average power measured by Agilent B2902A at a 50 kS/s sample rate in the period of 2 s.

Fig. 14 shows the measured power efficiency of the charge pump versus the loading currents between the phase-shifted clock ($V_{ctrlp} = 1$) and the fixed clock ($V_{ctrlp} = 0$). The

TABLE I
PERFORMANCE COMPARISON WITH THE PRIOR WORKS

	JSSC 2006 [13]	ISSCC 2014 [15]	ISSCC 2015 [14]	JSSC 2000 [11]	This work
Technology	0.13-μm CMOS	0.16-μm CMOS	0.5-μm CMOS	0.25-μm CMOS	0.18-μm CMOS
Conv. Ratios	1.4	4.8	1/2, 2/3, 3/4	3.5	3.2
Vin	3.3 V	3.3 V	1.6~2.2 V	2.5V	3.3V
Vout	4.5 V@30mA	16 V@7mA	0.6~1.2V	9V@40μA	10.5V@3.5mA
Output Current	1 ~ 30 mA	0.1 ~ 7 mA	n/A	1 ~ 40μA	0.5 ~ 3.5 mA
Flying Cap	SMD Ext. 2μF +330nF×2	SMD Ext. 1μF×2 +100nF+220nF	n/A	n/A	MIMCAP Integrated 400pF
Peak Efficiency	70%~75%	70%@7mA	78.3%	65%@40μA	69%@3mA
Smoothing Technology	No	No	Turn on Switches Slowly	Charge Sharing	Phase-Shifted Clocking Scheme
Smoothed Factor	No	No	n/A	3	3
Power Density	n/A	n/A	180 mW/mm^2	n/A	26 mW/mm^2
Output Ripple (Relative to the output voltage)	0.75% (with 2000-nF load capacitor)	1% (with 100-nF load capacitor)	n/A	n/A	2.7% (with 0.1-nF load capacitor)

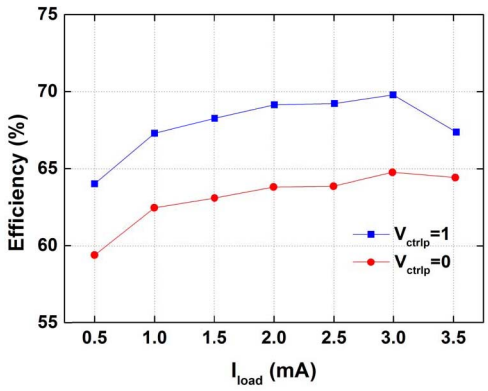

Fig. 14. Measured power efficiency of the high-voltage generator versus loading currents between the phase-shifted clock ($V_{ctrlp} = 1$) and the fixed clock ($V_{ctrlp} = 0$).

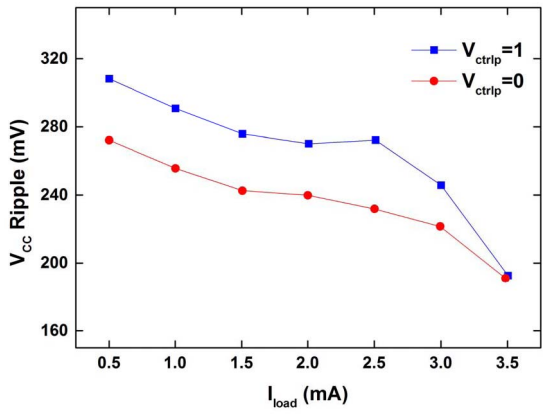

Fig. 15. Measurement result of output voltage ripple on 100-pF loading capacitance versus different loading current (I_{load}).

maximum power efficiencies are 64% and 69% between the conventional clocks and the proposed phase-shifted clocks schemes, respectively. It shows that the phase-shifted clocks for charge pump can smooth the charging current with improving the power efficiency. Fig. 15 shows the measurement results of output voltage ripples on 100-pF loading capacitance versus different loading current (I_{load}). The output voltage ripples increase slightly when the new clocking scheme is used. Chip area is reduced by using small integrated loading and pumping capacitance at the expense of degrading the performance of output voltage ripple. The maximum output ripple is 2.7% under 100-pF loading capacitance. But, it fully meets the requirements of medical applications. The charge balance performance of the stimulator, which is supplied by such a charge pump, is well enough [6].

Table I summarizes the key specifications of the proposed charge pump relative to the prior works, which include the

charge pumps with charging current smoothing technology and the step-up charge pumps with specialty of outputting a large current. Comparing with the smoothing technologies in [11] and [14], the proposed phase-shifted clocking scheme focuses on reducing the input current ripple in multi-stage charge pump. With the DC input voltage of 3.3 V, the proposed charge pump, which is capable of providing 11.5-V voltage with 3.5-mA loading current, can achieve DC conversion efficiencies of up to 69% by using integrated 400-pF capacitances.

IV. Conclusion

A new concept for smoothing the charging current is introduced and described in this work. The theoretical analyses indicate that the charging current of 3-stage cross-couple charge pump can be smoothed greatly when the clock signals are separated to each other by one-sixth pump cycle (T/6). This conclusion can be expanded as that the charging current of n-stage cross-couple charge pump can be smoothed greatly when the clock signals are separated to each other by $T/(2 \cdot n)$ ($m = 1/\mathrm{n}$) seconds. The charge pump with this new clocking scheme has been designed and successfully verified in a 0.18-μm 1.8-V/3.3-V CMOS process. Experimental results show that the charging current ripples of the charge pump are reduced by a factor of three with improving the power efficiency.

Appendix

The following discussions are the references for the charging current ($i_{total,new}(t)$) of charge pump with the new clocking scheme. In order to analyze and calculate those charging currents for simplicity, assuming that the output voltage of each stage charge pump with the new clocking scheme is the same as that of each stage charge pump with the conventional clocking scheme.

The new clocking schemes for charge pump are shown in Fig. 1(c). When the clock clkbub_1 goes from low to high, and clkbub_2 is in logic 0, the capacitor $\mathrm{C_{E2}}$ is charging by $\mathrm{C_{E6}}$. Defining $V_{C_{E2,new}}(0^-)$ as the initial voltage on capacitor $\mathrm{C_{E2}}$ at $t = 0$, it has been charge by capacitor $\mathrm{C_{E1}}$ with $\frac{T}{2} \cdot (1 - m)$ seconds. Referring to (12), $V_{C_{E2,new}}(t)$ can be approximately expressed as

$$V_{C_{E2,new}}(t) = c(t) \cdot \left[2 \cdot V_{DDH} - V_{C_{E2,new}}\left(0^-\right)\right] + V_{C_{E2,new}}\left(0^-\right). \tag{37}$$

Referring to (3)

$$V_{C_{E2,new}}\left(\frac{T}{2} \cdot m\right) = 2 \cdot V_{DDH} - \frac{T \cdot I_{out}}{2 \cdot C_E}. \tag{38}$$

With (37) and (38), the solutions for $V_{C_{E2,new}}(0^-)$ and $V_{C_{E6,new}}(\frac{T}{2} \cdot m)$ can be approximately expressed as

$$V_{C_{E2,new}}\left(0^-\right) = 2 \cdot V_{DDH} - \frac{T \cdot I_{out}}{2 \cdot C_E \cdot \left(1 - c\left(\frac{T}{2} \cdot m\right)\right)}. \tag{39}$$

$$V_{C_{E6,new}}\left(\frac{T}{2} \cdot m\right) = -V_{DDH} + \frac{c\left(\frac{T}{2} \cdot m\right) \cdot T \cdot I_{out}}{2 \cdot C_E \cdot \left(1 - c\left(\frac{T}{2} \cdot m\right)\right)}. \tag{40}$$

Referring to (11), $i_{12}(t)$, during $0 \le t < \frac{T}{2} \cdot m$, can be expressed as

$$i_{12}(t) = \varepsilon \cdot a(t) \cdot \frac{1}{2 \cdot \left(1 - c\left(\frac{T}{2} \cdot m\right)\right)}. \tag{41}$$

After $\frac{T}{2} \cdot m$ seconds, the clock clkbu_2 goes from high to low, the capacitor $\mathrm{C_{E5}}$ is charging by the capacitor $\mathrm{C_{E6}}$. The initial voltage on capacitor $\mathrm{C_{E5}}$ can be expressed as

$$V_{C_{E5,new}}\left(\frac{T}{2} \cdot m\right) = 2 \cdot V_{DDH} - \frac{T \cdot I_{out}}{C_E}. \tag{42}$$

With (12) and (42), $i_{12}(t)$, during $\frac{T}{2} \cdot m \le t < \frac{T}{2}$, can be $t < \frac{T}{2}$, can be expressed as

$$i_{12}(t) = \varepsilon \cdot a(t) \cdot \frac{2 - 3 \cdot c\left(\frac{T}{2} \cdot m\right)}{2 \cdot a\left(\frac{T}{2} \cdot m\right) \cdot \left(1 - c\left(\frac{T}{2} \cdot m\right)\right)}. \tag{43}$$

References

[1] W.-M. Chen *et al.*, "A fully integrated 8-channel closed-loop neural-prosthetic CMOS SoC for real-time epileptic seizure control," *IEEE J. Solid-State Circuits*, vol. 49, no. 1, pp. 232–247, Jan. 2014.

[2] C. Y. Lin, W. L. Chen, and M. D. Ker, "Implantable stimulator for epileptic seizure suppression with loading impedance adaptability," *IEEE Trans. Biomed. Circuits Syst.*, vol. 7, no. 2, pp. 196–203, Apr. 2013.

[3] I. Williams and T. Constandinou, "An energy-efficient dynamic voltage scaling neural stimulator for a proprioceptive prosthesis," *IEEE Trans. Biomed. Circuits Syst.*, vol. 7, no. 2, pp. 129–139, Apr. 2013.

[4] M. Monge *et al.*, "A fully intraocular high-density self-calibrating epiretinal prosthesis," *IEEE Trans. Biomed. Circuits Syst.*, vol. 7, no. 6, pp. 747–760, Dec. 2013.

[5] H. Chun, Y. Yang, and T. Lehmann, "Safety ensuring retinal prosthesis with precise charge balance and low power consumption," *IEEE Trans. Biomed. Circuits Syst.*, vol. 8, no. 1, pp. 108–118, May 2013.

[6] Z. Luo and M.-D. Ker, "A high-voltage-tolerant and precise charge-balanced neuro-stimulator in low voltage CMOS process," *IEEE Trans. Biomed. Circuits Syst.*, to be published.

[7] M.-D. Ker, S.-L. Chen, and C.-S. Tsai, "Design of charge pump circuit with consideration of gate oxide reliability in low-voltage CMOS process," *IEEE J. Solid-State Circuits*, vol. 41, no. 5, pp. 1100–1107, May 2006.

[8] J.-Y. Kim, Y.-H. Jun, and B.-S. Kong, "CMOS charge pump with transfer blocking technique for no reversion loss and relaxed clock timing restriction," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 56, no. 1, pp. 11–15, Jan. 2009.

[9] S. K. Kelly and J. L. Wyatt, "A power-efficient neural tissue stimulator with energy recovery," *IEEE Trans. Biomed. Circuits Syst.*, vol. 5, no. 1, pp. 20–29, Feb. 2011.

[10] H.-M. Lee, H. Park, and M. Ghovanloo, "A power-efficient wireless system with adaptive supply control for deep brain stimulation," *IEEE J. Solid-State Circuits*, vol. 48, no. 9, pp. 2203–2206, Sep. 2013.

[11] C. Lauterbach, W. Weber, and D. Romer, "Charge sharing concept and new clocking scheme for power efficiency and electromagnetic emission improvement of boosted charge pumps," *IEEE J. Solid-State Circuits*, vol. 35, no. 5, pp. 719–723, May 2000.

[12] Y. Ismail, H. Lee, S. Pamarti, and C.-K. K. Yang, "A 34 V charge pump in 65 nm bulk CMOS technology," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2014, pp. 408–409.

[13] J.-Y. Lee *et al.*, "A regulated charge pump with small ripple voltage and fast start-up," *IEEE J. Solid-State Circuits*, vol. 41, no. 2, pp. 425–432, Feb. 2006.

[14] Y. Lu *et al.*, "A 123-phase DC-DC converter-ring with fast-DVS for microprocessors," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2015, pp. 363–365.

[15] R. Karadi and G. V. Pique, "3-phase 6/1 switched-capacitor DC-DC boost converter providing 16 V at 7 mA and 70.3% efficiency in 1.1 mm^3," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2014, pp. 92–94.

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