ESD Protection Design for Touch Panel Control IC Against Latchup-Like Failure Induced by System-Level ESD Test

Ming-Dou Ker, *Fellow, IEEE,* Po-Yen Chiu, Wuu-Trong Shieh, and Chun-Chi Wang

***Abstract*— Due to the snapback holding voltage of high-voltage (HV) nMOS smaller than the maximum operating voltage, the traditional power-rail electrostatic discharge (ESD) clamp circuit implemented with such HV nMOS suffered latchup-like failure in a touch panel control IC after the system-level ESD test. A modified design on the power-rail ESD clamp circuit is proposed and verified in an HV CMOS process with 12 V double-diffused drain MOS device. With the holding voltage greater than the maximum operating voltage of 12 V, the touch panel equipped with the modified control IC can successfully pass the system-level ESD test of ±15 kV in the air-discharge test mode to meet the level 4 of IEC 61000-4-2 industry specification.**

***Index Terms*— Electrostatic discharge (ESD), latchup, system-level ESD test, transmission line pulsing (TLP).**

I. Introduction

With the combination of display panel and touch control interface, touch panel applications have been widely used in consumer electronics to improve their friendly utility and operating convenience. The typical schematic of a touch panel with the mutual-capacitance sensing method [1] to provide higher sensing resolution is shown in Fig. 1. The transmitter (TX) provides driving signals to TX electrode, and the driving signals also inject the relative signals into the receiver (RX) electrode through the mutual-capacitance array; then, the controller system processes the signals sensed from RX interface to recognize the touched positions. Fig. 2 shows the mutual-capacitance sensing method, when the finger touches the panel, the local electrostatic field is changed and alters the capacitance of the mutual capacitor (C_M). Thus, the capacitance difference will cause the RX signal to be different from other positions those are not touched. But, the capacitance variation after finger touched is much smaller than

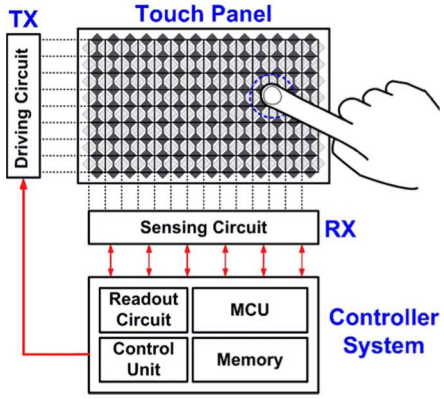

Fig. 1. Schematic of touch panel with mutual-capacitance sensing.

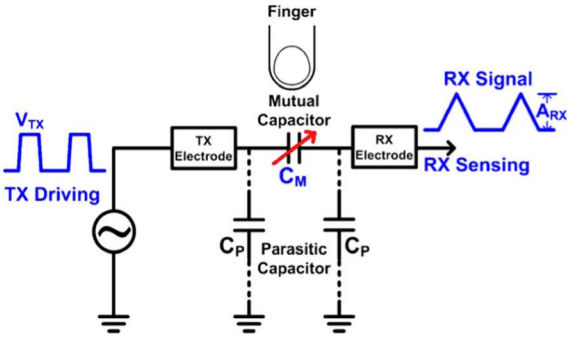

Fig. 2. Illustration of mutual-capacitance sensing method.

the capacitance of the parasitic capacitor (C_P), and it results in the touch sensing system to have a low signal-to-noise ratio. To overcome this issue, the typical method is to enlarge the TX driving signal voltage level, and the amplitude (A_{RX}) of RX signal will also be increased to raise the signal processing margin. Thus, the TX interface must be realized with high-voltage (HV) CMOS devices to provide higher voltage driving signals. Such a method has been widely adapted in the touch panel control ICs.

The electrostatic discharge (ESD) protection circuits were implemented for all input/output (I/O) and power (V_{DD}/V_{SS}) pins in this touch panel control IC against ESD damage. Two chip-level ESD tests are often used, the human-body-model (HBM) test [2] and machine-model (MM) test [3]. Besides, a system-level ESD test is applied to confirm the robustness of whole electronic product [4]. With the original version of ESD protection design, the touch panel control IC

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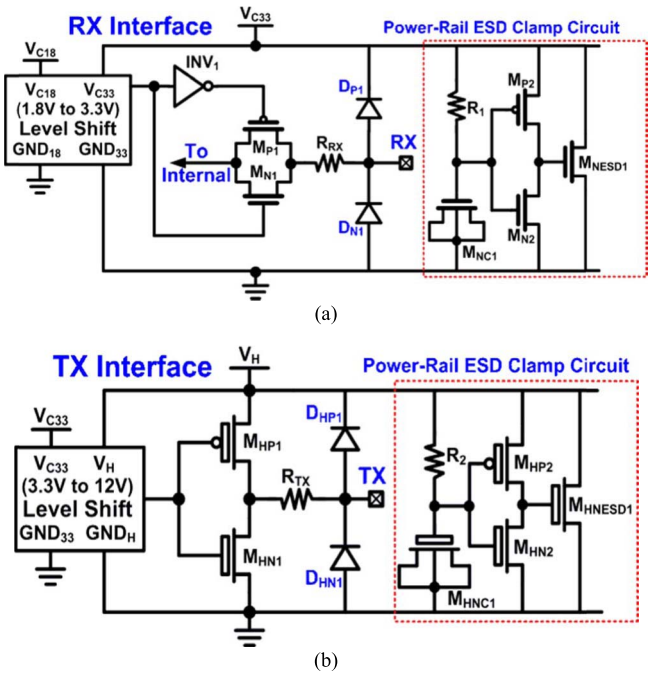

Fig. 3. Schematics of ESD protection design for (a) RX and (b) TX pins in a touch panel control IC.

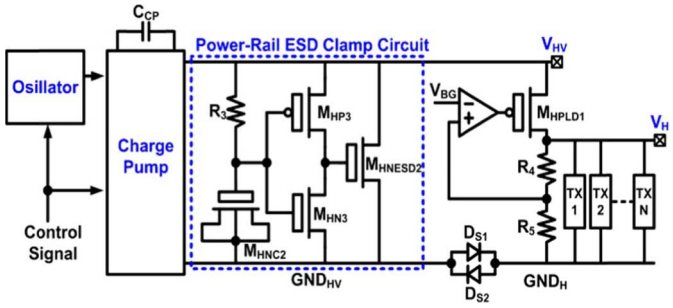

Fig. 4. Power-rail ESD clamp circuit for HV output (V_{HV} pin.

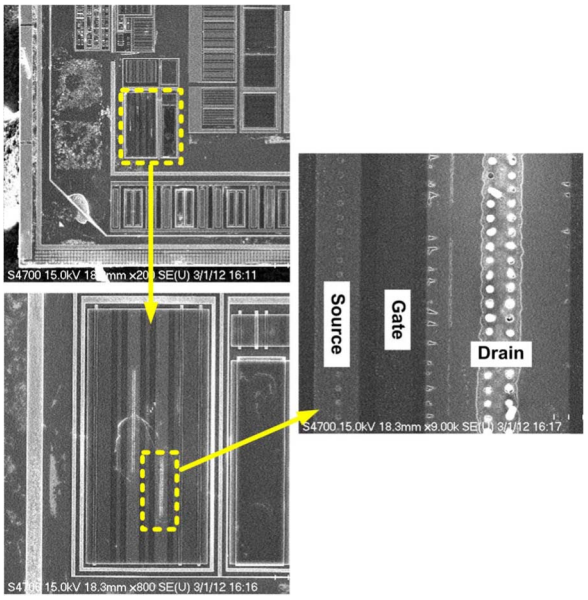

Fig. 5. SEM photograph to show the failure location on the HV power-rail ESD clamp circuit in the touch panel control IC after the system-level ESD test of ±15 kV in the air-discharge mode.

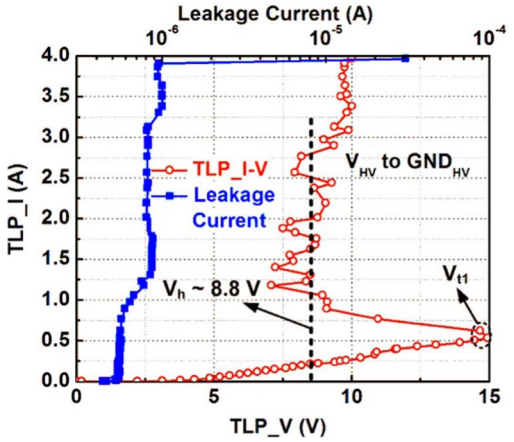

Fig. 6. TLP-measured *I*–*V* curve of the HV output pin from V_{HV} to GND_{HV} in the touch panel control IC.

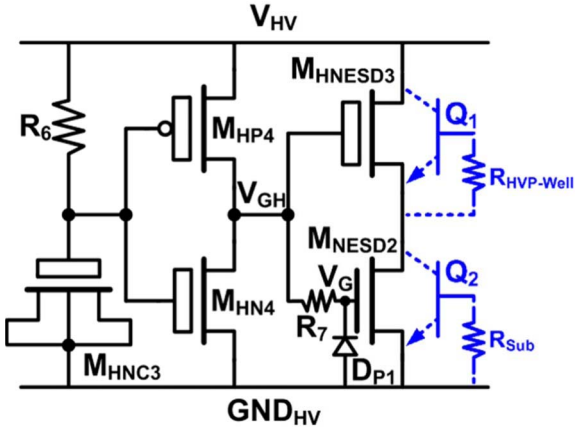

Fig. 7. Modified HV power-rail ESD clamp circuit against latchup-like issue in the touch panel control IC.

successfully achieved the chip-level ESD robustness at least 4 kV in HBM test and 400 V in MM test. However, after the system-level ESD test in a demo board with the touch panel together, the touch panel control IC started to conduct a large leakage current, and the 12 V HV output provided by the charge pump circuit cannot reach the correct voltage level. By failure analysis, the failure location was found on the HV power-rail ESD clamp circuit of the touch panel control IC.

In this brief, a modified design on the HV power-rail ESD clamp circuit was proposed to successfully solve this latchup-like issue in the touch panel control IC.

II. Original ESD Protection Design in the Touch Panel Control IC

A. ESD Protection Design

To comprehensively protect IC against ESD stresses, efficient paths to discharge ESD currents at all I/O pins are necessary. In the touch panel control IC, the major I/O pins are RX and TX pins. Fig. 3(a) and (b) shows the schematics of ESD protection for RX and TX pins, respectively, in the touch panel control IC. The ESD protection for RX pin is realized by diodes D_{P1} and D_{N1} with the power-rail

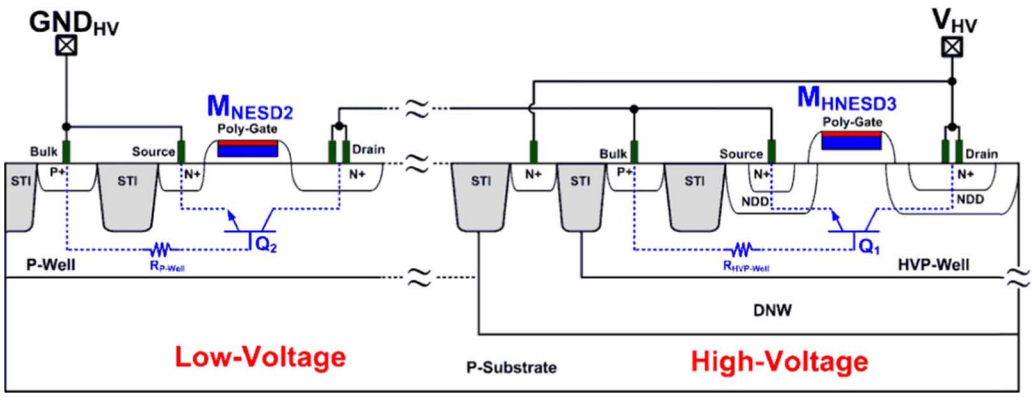

Fig. 8. Cross-sectional view of the stacked MOSFETs with an HV (12 V) n-type MOSFET M_{HNESD_3} and a low-voltage (3.3 V) n-type MOSFET M_{NESD_2}.

ESD clamp circuit [5], which includes an *RC*-based ESD-detection circuit (R_1, $M_{\rm NC1}$, M_{P2}, and M_{N2}) and a large n-type MOSFET ($M_{\rm NESD1}$). In the TX pin, its ESD protection design is similar to that of RX pin. But, in order to sustain in a high operating voltage of 12 V, the diodes ($D_{\rm HP1}$ and $D_{\rm HN1}$) are realized by HV diodes and the power-rail ESD clamp circuit is composed of HV MOSFETs ($M_{\rm HNC1}$, $M_{\rm HP2}$, $M_{\rm HN2}$, and $M_{\rm HNESD1}$). In the touch panel control IC, the 12 V HV power supply for TX interfaces is provided by on-chip charge pump circuit. To protect the power pin against ESD stresses, the HV power-rail ESD clamp circuit is also implemented at the HV output ($V_{\rm HV}$) pin, as that shown in Fig. 4.

B. ESD Test Results

The touch panel control IC was fabricated in a 1.8/3.3/12 V CMOS process with 12 V double-diffused drain MOS (DDDMOS) device. With a large channel width of 840 μm for realizing the main ESD devices ($M_{\rm NESD1}$, $M_{\rm HNESD1}$, and $M_{\rm HNESD2}$) in the power-rail ESD clamp circuits, the RX/TX pins, low-voltage (1.8/3.3 V) power pins, and HV (12 V) output pin can sustain ESD stresses at least 4 kV in HBM test and 400 V in MM test.

After the touch panel control IC assembled into a demo board with the touch panel together, when the system-level ESD gun applied a voltage of $\pm$15 kV at the panel edge (near the touch panel control IC) under the air-discharge mode, the display panel started to have some malfunctions. Inside the touch panel control IC, the HV output pin began to conduct a large leakage current. Moreover, the 12 V HV output, which provided by the charge pump circuit, cannot reach the correct voltage level. It presented a typical latchup-like failure on the 12 V voltage output.

C. Failure Analysis

By comparing the chip layout and the hot-spot image of the emission microscopy photograph, the leakage location was found at the HV power-rail ESD clamp circuit. The scanning electron microscope (SEM) was used to get the failure photograph on the touch panel control IC after the system-level ESD test, as that shown in Fig. 5. The failure point was found on the multiple-finger drain regions of $M_{\rm HNESD2}$ in the HV power-rail ESD clamp circuit.

In addition, the transmission line pulsing (TLP)-measured I–V curve of the HV output pin from $V_{\rm HV}$ to $\rm GND_{HV}$ is shown in Fig. 6, where the trigger voltage (V_{t1}) is $\sim$15 V and the snapback holding voltage (V_h) is only $\sim$8.8 V. Although I_{t2} can be up to $\sim$4 A, V_h of 8.8 V is lower than the operating voltage of 12 V in the touch panel applications. With a holding voltage smaller than the operating voltage, the ICs often suffered the latchup-like failure issue [6]–[9].

III. Modified Design of High-Voltage Power-Rail ESD Clamp Circuit

A. Modified ESD Protection Design

A modified design on the HV power-rail ESD clamp is proposed in Fig. 7, where a 12 V n-type MOSFET ($M_{\rm HNESD3}$) is stacked with a 3.3 V n-type MOSFET ($M_{\rm NESD2}$) to increase the total holding voltage. The modified design is also composed with an *RC*-based ESD-detection circuit (R_6, $M_{\rm HNC3}$, $M_{\rm HP4}$, and $M_{\rm HN4}$). The device cross-sectional view of the stacked n-type MOSFETs is drawn in Fig. 8. To avoid the gate of $M_{\rm NESD2}$ be directly stressed by the overshooting ESD pulse through the turned-ON $\rm M_{HP4}$ during ESD events, R_7 is connected to the gate terminal V_G of $M_{\rm NESD2}$. Moreover, a low-voltage diode D_{P1} is added from the V_G node to $\rm GND_{HV}$. Therefore, the gate voltage V_G at $M_{\rm NESD2}$ can be clamped to a safe voltage region by D_{P1} when an overshooting ESD voltage is occurring.

When a positive ESD pulse is applying at $V_{\rm HV}$ with $\rm GND_{HV}$ grounded, the ESD-detection circuit can turn ON $M_{\rm HNESD3}$ and $M_{\rm NESD2}$ to discharge ESD current. The parasitic n-p-n bipolar junction transistors (BJTs) Q_1 and Q_2 will be triggered on to conduct ESD current. On the contrary, when a negative ESD pulse is applying at $V_{\rm HV}$ with $\rm GND_{HV}$ grounded, the ESD current can be discharged through the parasitic diodes under the forward-based conditions.

B. Experimental Results

The modified HV power-rail ESD clamp circuit has been implemented in the touch panel control IC, which fabricated in a 1.8/3.3/12 V CMOS process with 12 V DDDMOS devices. Fig. 9 shows the whole chip photograph of the touch panel control IC. The corresponding layout top view of the modified

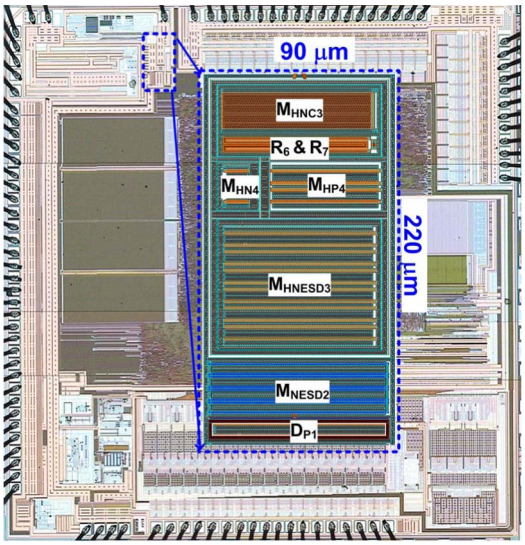

Fig. 9. Chip photograph of the touch panel control IC with the modified high-voltage power-rail ESD clamp circuit.

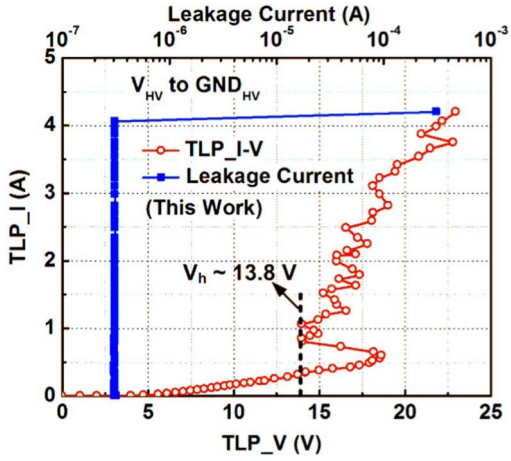

Fig. 10. TLP measured *I*–*V* curve of the modified high-voltage power-rail ESD clamp circuit.

HV power-rail ESD clamp circuit is also shown in Fig. 9 (inset), which occupied a silicon area of 90 μm × 220 μm. The channel widths of M_{HNESD3} and M_{NESD2} are 840 and 500 μm, respectively.

To investigate the holding voltage in the modified design, the TLP measured *I*–*V* curve is shown in Fig. 10. When the TLP voltage increased to ~18.6 V, the parasitic n-p-n BJTs are triggered on to cause snapback. After the snapback occurred, the voltage is clamped to ~13.8 V. Because the holding voltage of 13.8 V is greater than the operating voltage of 12 V, the touch panel control IC can be free to the latchup-like failure in the touch panel applications.

With the modified design, the touch panel control IC can still achieve the chip-level ESD robustness of at least 4 kV in HBM test and 400 V in MM test. Finally, the display panel equipped with the modified touch panel control IC can successfully pass the system-level ESD test of ±15 kV in the air-discharge mode without causing latchup-like failure again.

IV. Conclusion

In this practical case, the lower holding voltage of the power-rail ESD clamp circuit caused a touch panel control IC suffering the latchup-like failure after system-level ESD test. With the HV and low-voltage n-type MOSFETs stacked in the power-rail ESD clamp circuit, the modified design can achieve a total holding voltage higher than the operating voltage of touch panel applications. Therefore, the touch panel control IC with the modified power-rail ESD clamp circuit can be free to latchup-like failure under system-level ESD test. In addition, it also performed a good enough chip-level ESD robustness for the touch panel control IC.

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