System-Level ESD Protection for Automotive Electronics by Co-Design of TVS and CAN Transceiver Chips

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***Abstract*—This paper proposed a co-packaged methodology using transient voltage suppressor (TVS) chips and a controller area network (CAN) bus transceiver to ensure IEC 61000-4-2 system-level ESD protection. The design methodology is verified in a high-voltage silicon-on-insulator process for CAN transceiver chip and an 0.8-μm bipolar process for TVS chips. The *I–V* curves of the TVS and CAN transceiver chip are evaluated by the transmission line pulsing system with the pulse width of 100 ns. The breakdown voltage of the bi-directional TVS chips and CAN transceiver chip are higher than ±80 V compared with the ±70 V fault voltage tolerance requirement. The clamping voltage of the TVS device is lower than ±130 V to discharge ESD current before the CAN transceiver chip breakdown for effective ESD protection. The design target of parasitic inductance by bonding wires is calculated to meet the clamping voltage requirement. The CAN bus transceiver IC with TVS chips co-packaged has been evaluated to pass the IEC61000-4-2 contact ±15-kV stress without any hardware damages and latch-up issues.**

***Index Terms*—Controller area network (CAN), ESD, transient voltage suppressor (TVS).**

I. Introduction

INTELLIGENT vehicle systems have been used in automotive electronics for achieving car safety and communications between vehicle and sensors. The intelligent vehicle system with intelligent sensing and control algorithms can enhance driving safety by using collision warning and partially controlling the vehicle [1]–[4]. Due to the higher safety and reliability requirements for automotive applications, a reliable in-vehicle network with fault tolerance and high-speed is necessary for intelligent vehicle systems.

The controller area network (CAN) is a robust protocol used in the on-board diagnostics (OBD)-II vehicle diagnostics standard for connecting electronic control units (ECU) [5], [6].

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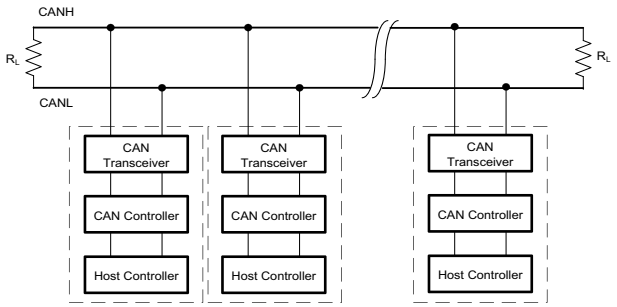

Fig. 1. System architecture of the CAN bus interface.

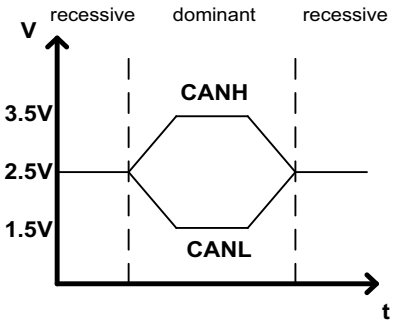

Fig. 2. CAN bus signal levels for the CANH and CANL at the recessive and dominant states.

The CAN bus is designed to operate at speeds ranging from 20 kb/s to 1 Mb/s. The connection of the CAN bus interface is shown in Fig. 1. As can be seen, the CAN transceiver is connected to the bus CANH and CANL. The CAN bus signal levels for CANH and CANL are shown in Fig. 2 and the signal range is described in Table I [7], [8]. When the bus is idle, CANH and CANL are biased to 2.5 V±0.5 V, which is called the recessive state. When the bus is active as the so-called dominant state, CANH is typically biased to 3.5 V, and CANL is typically biased to 1.5 V. The differential signaling of CAN protocol can bring about its high noise immunity and fault tolerance against a wide range of communication errors. To provide high robustness of fault voltage tolerance at CANH and CANL, the CAN transceiver physical layer must be able to sustain high voltage to avoid damage resulting from over voltage stress [9].

Ensuring system-level ESD protection for automotive electronics is absolutely necessary to ensure reliability and

TABLE I
THE LOGIC THRESHOLD VOLTAGE RANGE OF THE CAN BUS SIGNAL FOR THE CANH AND CANL AT THE RECESSIVE AND DOMINANT STATES

CAN Bus Line State	Signal	Minimum Voltage	Typical Voltage	Maximum Voltage
Dominant	CANH	2.75 V	3.5 V	4.5 V
	CANL	0.5 V	1.5 V	2.25 V
Recessive	CANH	2.0 V	2.5 V	3.0 V
	CANL	2.0 V	2.5 V	3.0 V

safety [10]–[13]. The CAN bus must have the ESD protection solutions on CANH and CANL to withstand IEC61000-4-2 direct pin injection stress [14]. Due to the latch-up issue and fault voltage tolerance considerations, the high-voltage silicon-on-insulator (SOI) process is necessary in designing the CAN transceiver IC [10]. On-chip system-level ESD protection is not suitable for sustaining high-energy transients, because a large silicon area is needed to increase the chip cost. In general, the off-chip TVS arrays are the best choice if the interface IC cannot provide the sufficient protection capability [15]. The system-level ESD robustness depends on the PCB trace layout and the clamping voltage of the off-chip TVS devices [16]. To obtain the best system-level ESD performance, the right TVS devices must be chosen, and the appropriate PCB layout guidelines should be followed. However, this may waste more PCB area and result in greater time spent for more R&D development.

In the current work, the co-packaging of the CAN transceiver IC and TVS chips for system-level ESD protection is proposed. The advantage of the co-packaged protection scheme is that system designers do not have to consider the TVS device specification and the PCB layout for ESD protection [17]. The direct pin injection system-level ESD robustness depends on the CAN transceiver IC itself. Moreover, the PCB space will be more compact by co-packaging the CAN transceiver IC and TVS chips. The proposed CAN bus transceiver IC with TVS chip integration has been evaluated to pass IEC 61000-4-2 contact discharge (class B) of ± 15 kV in real-time data transmissions without hardware damage and latch-up issue, with suitable analysis of the parasitic inductances by bonding wires.

II. DESIGN CONSIDERATIONS OF THE CO-PACKAGED CAN TRANSCEIVER IC AND TVS CHIPS

A. Proposed CAN Transceiver Design

The design scheme of the proposed co-packaged TVS chips and CAN bus transceiver is shown in Fig. 3. In terms of the fault voltage tolerance requirement, the HVNMOS and HVPMOS can tolerate 70 V at drain side. The 5V NMOS and PMOS are controlled by digital logical circuits to provide the driving current during dominant state and turn-off during recessive state. The on-chip ESD protection devices can basically provide a human-body-model (HBM) [18], machine-model (MM) [19], and charged-device-model (CDM) [20] ESD protection, which are realized by the bi-directional high-voltage PNP in the SOI process to sustain the 70 V fault voltage tolerance. Additional bi-directional TVS chips

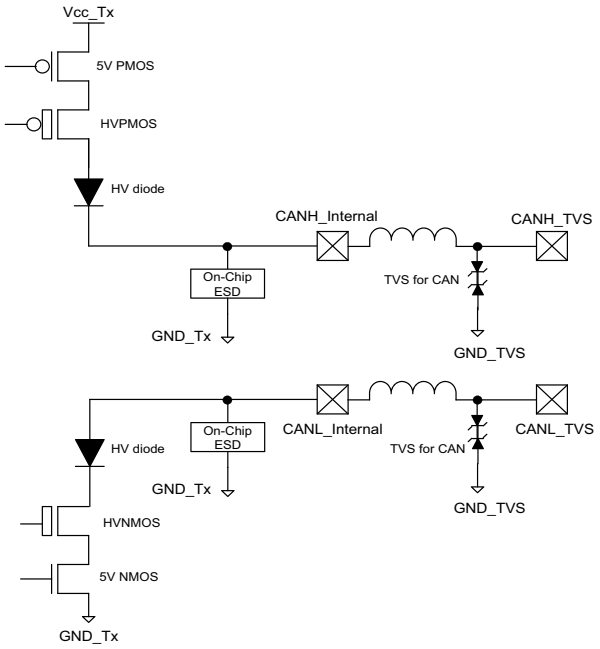

Fig. 3. Design scheme of the proposed co-packaged TVS chips and CAN bus transceiver.

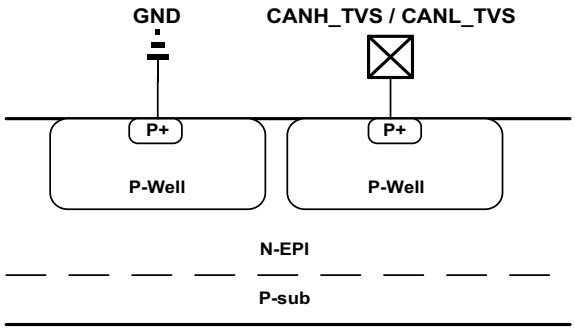

Fig. 4. Cross-sectional view of the proposed TVS device for CAN bus protection.

are co-packaged with the transceiver in the same package. The parasitic inductances are caused by the bonding wire to achieve the connection between the transceiver chip and TVS chips.

B. Proposed TVS Design

The proposed TVS is realized by a bi-directional high-voltage PNP in an 0.8-μm bipolar process. The cross-sectional view of the TVS device is shown in Fig. 4. As can be seen, the PNP device has symmetric I-V characteristics for positive or negative voltage stresses because of the symmetric junction of the N-epi and P-well. The trigger-on voltage of the TVS device must be higher than 70 V to meet the fault voltage tolerance requirement. To protect the CAN transceiver under system-level ESD stress, the trigger-on voltage (V_t) and clamping voltage (V_{Clamp}) of the TVS device must be lower than the breakdown voltage of the HVNMOS and HVPMOS in the transceiver. The design window of the TVS device is shown in Fig. 5.

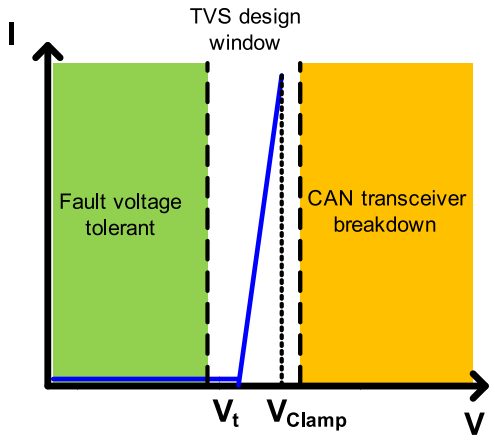

Fig. 5. ESD design window and I-V curve of the TVS device for the proposed CAN bus transceiver IC.

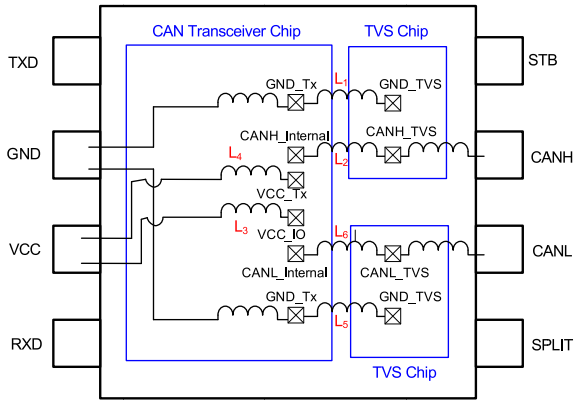

Fig. 6. Proposed protection scheme for the CAN bus with the co-packaged transceiver IC and TVS chips.

C. Co-Packaged CAN Transceiver and TVS

The proposed protection co-packaged scheme for the CAN bus with the transceiver IC and TVS chips is shown in Fig. 6. As can be seen, CANH and CANL pins are connected to CAN bus interface in the system. The TVS chips for system-level ESD protection are applied to these two pins to ensure safety and reliability. The CANH and CANL pins are bonded to the CANH_TVS and CANL_TVS on the TVS chips, respectively. Meanwhile, the CANH_internal and CANL_internal in the CAN transceiver chip are bonded to the CANH_TVS and CANL_TVS on the TVS chips, respectively. The parasitic inductances are caused by the bonding wire for the connection of the transceiver chip and TVS chips. To maximize the ESD protection capability, a GND pin is directly bonded to GND_TVS on the TVS chips. This is also ideal in minimizing the impedance of the ESD current discharging path through the TVS chips. However, the pin assignment of this package is already fixed for the system design. The GND pin is at the left-hand side and the TVS chips are at the right-hand side. The GND_TVS in the TVS chips and GND pin have to be bounded to the GND_Tx in the CAN transceiver chip. Therefore, the parasitic inductances L_1, L_2, L_5, and L_6 by the bonding wires should be calculated in designing the V_{Clamp} of the TVS device.

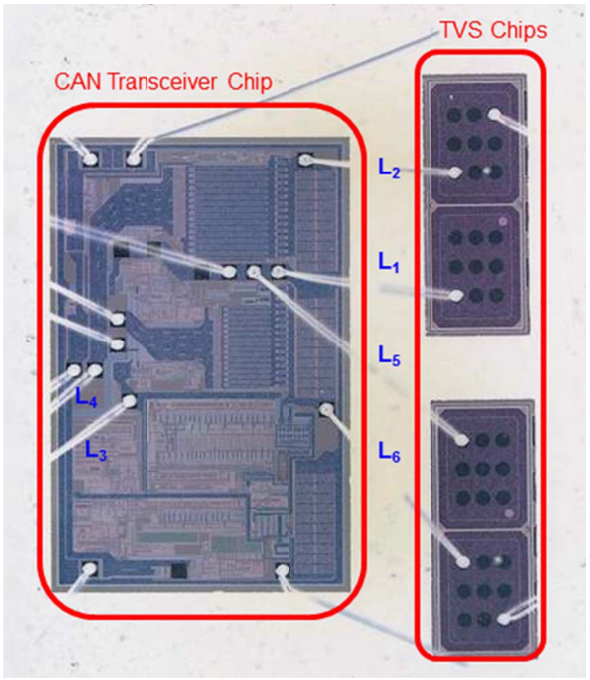

Fig. 7. Proposed whole chip of the co-packaged TVS chips and CAN bus transceiver IC. The TVS is a bi-directional high-voltage PNP device.

The whole chip of the co-packaged TVS chips and CAN bus transceiver IC is shown in Fig. 7. The layout area of one TVS chip is 1200 μm × 500 μm which can sustain higher than ±30 kV IEC61000-4-2 direct pin injection ESD stress. Two TVS chips are co-packaged in the IC to protect the CANH and CANL pins. The layout area of one on-chip ESD protection embedded in the CAN transceiver chip is 230 μm × 220 μm which can sustain ±8 kV HBM and ±800 V MM ESD stress. The L_1 to L_6 are the parasitic inductances by bonding wires for connection. The design consideration for the parasitic inductances is described in next section.

III. Co-Design With TVS and CAN Bus Transceiver

A. Evaluation of the TVS Device and On-Chip ESD Design

The DC I-V curves at 25°C and 125°C of the proposed TVS device have been evaluated by B2902A, as shown in Fig. 8. The leakage current at 60 V is around 1e-8 A at 25°C and 1e-7 A at 125°C. The breakdown voltage is around 80 V, which is suitable for 70 V fault voltage tolerance requirement of the CAN bus transceiver.

The parasitic capacitance of the proposed TVS device is around 11 pF, as evaluated by E4980A. The capacitance is lower than the 20 pF of the CAN bus transceiver requirement with 1 Mbit/s bit rate [7].

The secondary breakdown I-V curve of the TVS device and CAN transceiver chip with on-chip ESD protection design have been evaluated by Transmission-Line-Pulsing (TLP) system with the pulse width of 100 ns and the rise time of <1ns [21], [22], as shown in Fig. 9. The V_t of the

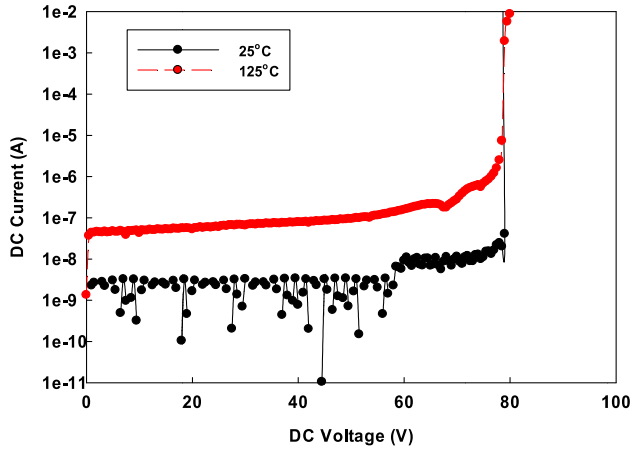

Fig. 8. DC measured I-V curves of the TVS device at 25°C and 125°C.

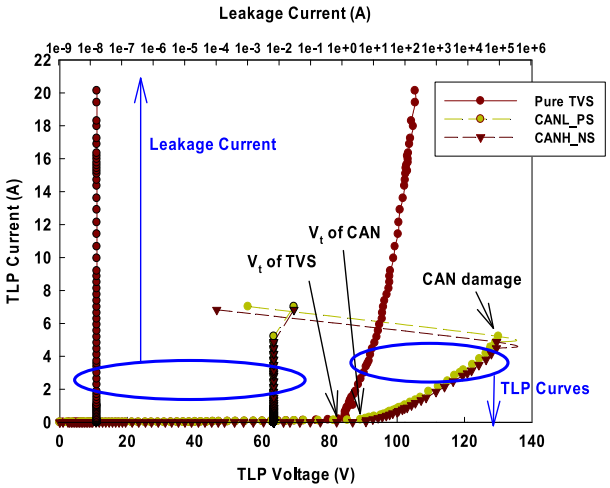

Fig. 9. TLP measured I-V curves of the TVS device and CAN transceiver without co-packaged TVS chips.

TVS device is ±85 V, which is higher than the fault voltage tolerance of ±70 V. There is no snapback phenomenon observed for the bi-directional PNP TVS device for latch-up free. The TVS device under TLP measurement can obtain a TLP current of up to 20 A without any obvious increase in the leakage current. According to the TLP I-V curve, the turned-on resistance (Ron) of the bi-directional PNP device is 1.0 ohm in the holding region. The V_t of the on-chip ESD protection device is ±90 V. The secondary breakdown is observed at 130 V for the CANL under positive stress and CANH under negative stress, which are the breakdown voltages of HVNMOS and HVPMOS, indicated in Fig. 3, respectively. The HVNMOS and HVPMOS are damaged by ESD stress after breakdown at 130 V. For negative stress at CANL and positive stress at CANH, the secondary breakdown occurred after the breakdown voltage of the HV diode plus HVNMOS and HVPMOS, respectively, which is much higher than 130 V. Therefore, the V_{Clamp} of TVS device has to be lower than ±130 V to protect the CAN transceiver chip. From the evaluation result, the proposed TVS device is suitable for system-level ESD protection in the co-packaged CAN bus transceiver IC.

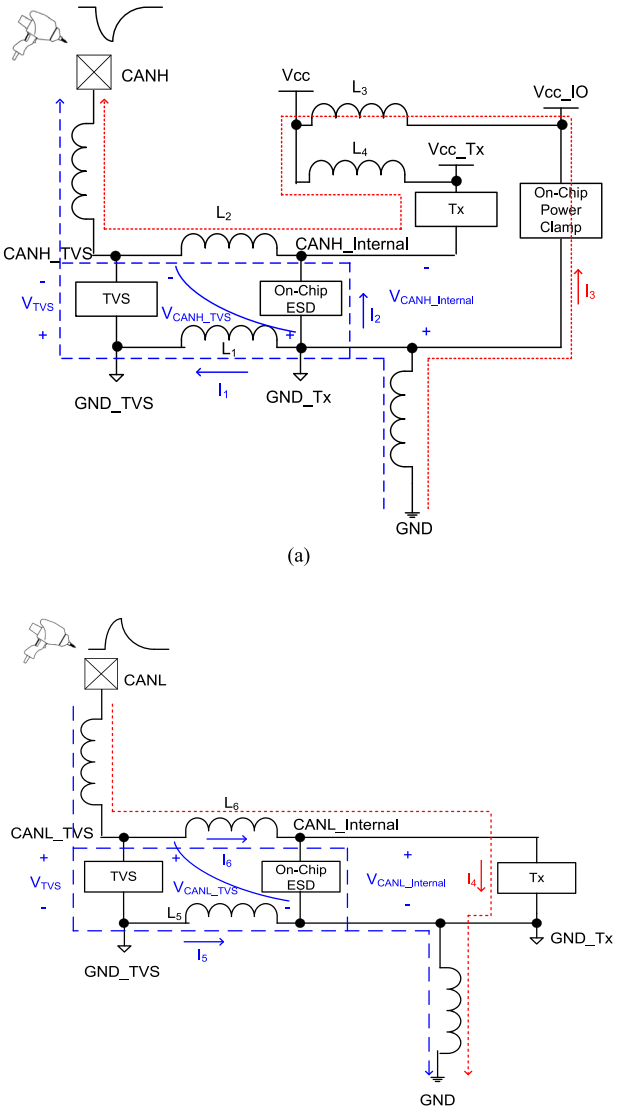

Fig. 10. Current discharge path of the proposed co-packaged TVS chips and CAN bus transceiver IC (a) CANH under negative ESD gun contact stress and (b) CANL under positive ESD gun contact stress.

B. Calculation of the Parasitic Inductances

The parasitic inductance is high for the ESD current due to the fast transience of the ESD pulse. For the co-design with TVS chips and CAN transceiver chip, the parasitic inductances by bonding wires must be considered to meet the design window for ESD protection. The current discharge paths of CANH under negative ESD gun contact stress and CANL under positive ESD gun contact stress with co-packaged TVS chips are shown in Fig. 10.

For the ESD protection of CANH under negative ESD gun contact stress in Fig. 10(a), the TVS has to discharge ESD current before the breakdown of Tx (V_{BD_TX}) occurs. The clamping voltage can be calculated as

$$I_1 * \omega L_1 + V_{TVS} = V_{CANH\_TVS} = V_{CANH\_Internal} + I_2 * \omega L_2 \quad (1)$$

$$V_{CANH\_Internal} < I_3 * \omega(L_3 + L_4) + V_{BD\_TX} \quad (2)$$

To sustain 8 kV ESD robustness of IEC61000-4-2, the ESD current must be 16 A [21]. From the TLP I-V curves in Fig. 9, the values in the formula are shown below

$$V_{TVS} = 105V \text{ at } I_1 = 16A \quad (3)$$
$$I_2 = I_{t2} \text{ of CANH\_NS} = 5A \quad (4)$$
$$V_{BD\_TX} = V_{t2} \text{ of CANH\_NS} = 130V \quad (5)$$

Given that I_3 before the breakdown of Tx is very small to be ignored, the design target of parasitic inductances for ESD protection of CANH under negative ESD gun contact stress can be predicted as

$$16A*\omega L_1 + 105V < 130V + 5A*\omega L_2 \quad (6)$$
$$16\omega L_1 - 5\omega L_2 < 25V \quad (7)$$

For the ESD protection of CANL under positive ESD gun contact stress in Fig. 10(b), the same method of analysis to calculate is given below

$$V_{TVS} + I_5 * \omega L_5 = V_{CANL\_TVS} = I_6 * \omega L_6 + V_{CANL\_Internal} \quad (8)$$

$$V_{CANL\_Internal} < V_{BD\_TX} (I_4 \text{ is very small to be ignored}) \quad (9)$$

To sustain 8 kV ESD robustness of IEC61000-4-2, the ESD current must be 16 A. From TLP I-V curves in Fig. 9, the values in the formula are shown below

$$V_{TVS} = 105V \text{ at } I_5 = 16A \quad (10)$$
$$I_6 = I_{t2} \text{ of CANL\_PS} = 5A \quad (11)$$
$$V_{BD\_TX} = V_{t2} \text{ of CANL\_PS} = 130V \quad (12)$$

The design target of the parasitic inductances for ESD protection of CANL under positive ESD gun contact stress can be predicted as below

$$105V + 16A*\omega L_5 < 5A*\omega L_6 + 130V \quad (13)$$
$$16\omega L_5 - 5\omega L_6 < 25V \quad (14)$$

In this CAN bus transceiver IC, the gold wire with diameter of 25 μm is used for the bonding wire. The parasitic inductance of this wire is 0.69 nH per millimeter [23]. Therefore, L_1, L_2, L_5, and L_6 in this work are 0.534, 0.445, 0.825, and 0.564 nH, respectively. Therefore, the values in the formulas (7) and (14) are shown below

$$16\omega L_1 - 5\omega L_2 = 0.41V \quad (15)$$
$$16\omega L_5 - 5\omega L_6 = 0.68V \quad (16)$$

From the above analysis, the co-design with TVS chips and CAN transceiver chip can provide effective ESD protection in the CAN bus transceiver IC.

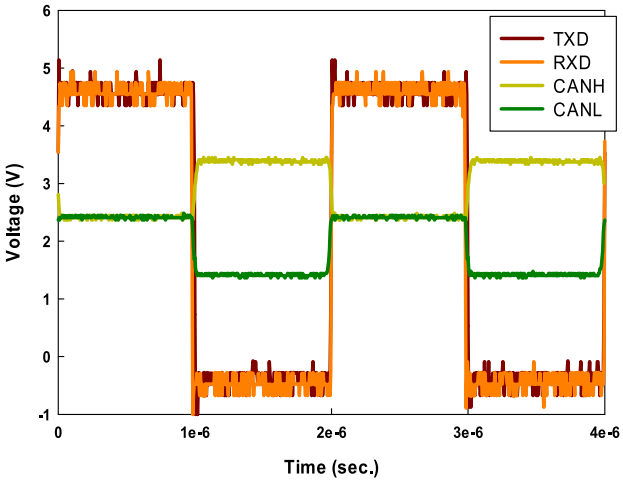

Fig. 11. Voltage waveforms of the signals at CANH and CANL during normal circuit operation.

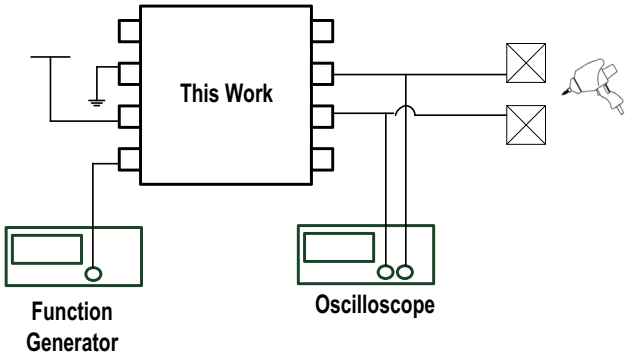

Fig. 12. System-level ESD testing setup for the co-packaged CAN bus transceiver IC with TVS chips.

IV. System Verification for CAN Bus Transceiver IC

For the function verification of the CAN bus transceiver IC, the voltage waveforms of the signals at CANH and CANL are shown in Fig. 11. When a logic high signal is biased at RXD, the CAN bus is in the recessive state. CANH and CANL are biased at 2.5 V. When a logic low signal is biased at RXD, the CAN bus is in the dominant state; CANH is typically biased to 3.5 V and CANL is typically biased to 1.5 V. Hence, the integrated TVS will not be triggered to cause function error during normal circuit operation.

The testing setup for the system verification of the CAN bus transceiver under ESD stress is shown in Fig. 12. The TVS chips are co-packaged in the IC to protect the CANH and CANL pins under system-level ESD stress. The function generator generated signals on RXD for real-time data transmissions. The waveforms of the signal at the CAN bus lines CANH and CANL are observed by using an oscilloscope. In the ESD contact discharge test, the CANH and CANL pins will be zapped to evaluate the direct pin injection protection capability of the CAN bus transceiver with TVS integration in the data flow condition. The waveforms of the signals at the CANH and CANL pins under 8 kV of IEC 61000-4-2 contact discharge at CANL are shown in Fig. 13. When the ESD stress

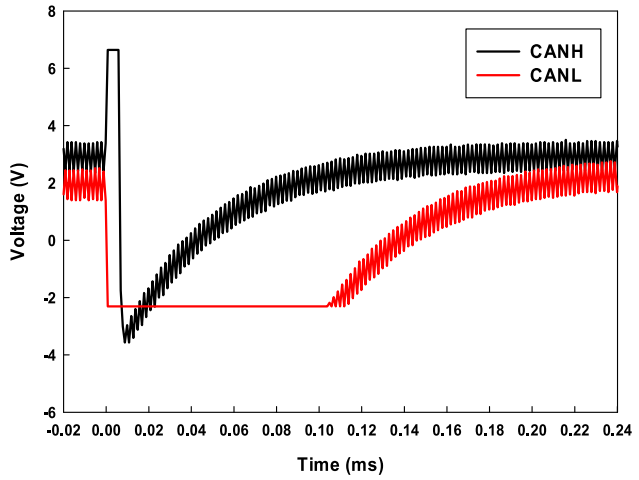

Fig. 13. Voltage waveforms of signals at CANH and CANL during IEC61000-4-2 ESD test of 8 kV at CANL.

TABLE II
COMPARISON OF THE ESD RESULTS OF THE CAN BUS TRANSCEIVER IC WITH AND WITHOUT CO-PACKAGED TVS CHIPS

Item	CANL to GND	CANH to GND
CAN Bus Transceiver without co-packaged TVS chips	±3 kV pass, ±4 kV fail	±2 kV pass, ±3 kV fail
CAN Bus Transceiver with co-packaged TVS chips	±15 kV pass	±15 kV pass

TABLE III
THE ELECTRICAL CHARACTERISTICS OF THE PROPOSED CO-PACKAGED CAN BUS TRANSCEIVER IC WITH TVS CHIPS

IEC61000-4-2 ESD Level at CANH and CANL (Air / Contact Discharge)	HBM at all Pins	Fault Voltage Tolerance at CANH and CANL
±15 kV	±8 kV	±70 V

occurs at 0 ms, the TVS is turned-on to discharge ESD current, and the signal will be out of the voltage range of normal circuit operation. After 0.22 ms, the voltage level will be auto-recovered to 2.5 V±1 V without any manual reset or hardware damage, and the real-time data flow will not be stopped. The CAN bus transceiver IC with TVS chips integration has been verified to have no hardware damage and latch-up issue after performing the system-level ESD test. To sum up, the proposed co-packaged CAN bus transceiver IC with TVS chips has been verified to pass IEC 61000-4-2 ±15 kV contact discharge (class B, system can be auto-recovered after ESD stress) in real-time data transmissions. The proposed co-work design methodology to co-package TVS chips in the CAN bus transceiver is both reliable and safe to use for automotive application.

The co-packaged CAN bus transceiver IC with TVS chips has been proposed in this work. The CAN transceiver chip was fabricated via a 0.5-μm high-voltage SOI process. The TVS chip was fabricated in an 0.8-μm bipolar process for system-level IEC 61000-4-2 ESD protection. The verification results for this CAN bus transceiver IC with and without TVS chips co-packaged are summarized in Table II. The system-level IEC 61000-4-2 ESD of the CAN bus transceiver without TVS chips co-packaged is only ±2 kV. The proposed CAN bus transceiver chip and TVS chips co-design can sustain ±15 kV system-level IEC 61000-4-2 ESD. The electrical characteristics of the proposed design are summarized in Table III. In this work, the high IEC61000-4-2 ESD level, on-chip HBM ESD level, and fault voltage tolerance is proposed to ensure high reliability and safety in automotive application.

V. CONCLUSION

As more and more cars are equipped with radars and sensors for intelligent vehicle systems, the CAN bus transceiver must be more reliable and robust against ESD event and must have fault voltage tolerance to ensure safety. Recently, direct pin injection of ESD stress at I/O ports has become a more stringent test to emulate ESD, CDE, or EOS events in field applications. The co-packaged TVS chips and CAN bus transceiver IC proposed in this work can sustain huge ESD energy. With suitable analysis on the parasitic inductances by bonding wires, the design target on the clamping voltage of the TVS device can be calculated. The breakdown voltage of the TVS device must be designed so that it is higher than ±70 V with fault voltage tolerance consideration. The CAN bus transceiver IC with TVS chip integration has been verified to pass IEC 61000-4-2 contact discharge (class B) of ±15kV in real-time data transmissions without hardware damage and latch-up issues. The analysis methodology for the proposed co-design with TVS chips and transceiver chip in CAN bus applications has been successfully verified against system-level ESD stress.

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