Comparison Between High-Holding-Voltage SCR and Stacked Low-Voltage Devices for ESD Protection in High-Voltage Applications

Chia-Tsen Dai and Ming-Dou Ker, *Fellow, IEEE*

***Abstract*— The modified silicon-controlled rectifier (SCR) fabricated in a 0.25-μm high-voltage (HV) bipolar-CMOS-DMOS (BCD) technology has been proposed to seek for both effective electrostatic discharge (ESD) protection and latchup immunity. Experimental results show that one of the proposed SCRs has a high holding voltage of up to ~30 V in the 100-ns transmission line pulsing measurement results. However, through the experimental verification by using the transient latchup test, the holding voltage of such proposed device decreases to ~20 V. It is due to the increased bipolar junction transistor current gains of the SCR path induced by the Joule-heating effect in the long-term measurement. For 20-V circuit applications, the ESD robustness of the proposed SCR with a holding voltage of ~20 V is lower than that of stacked low-voltage p-type MOS in the previous studies. Developing special modification of such HV devices is inefficient to achieve both effective ESD protection and latchup-free design in this 0.25-μm HV BCD technology.**

***Index Terms*— Electrostatic discharge (ESD), latchup, silicon-controlled rectifier (SCR).**

I. Introduction

With the characteristics of high power consumption and harsh operating environment in the high-voltage (HV) applications, rigorous reliability design is strongly needed for HV CMOS integrated circuits (ICs). Electrostatic discharge (ESD) protection is one of the most important reliability issues to CMOS ICs, especially in the HV applications. To protect the internal circuits and to avoid latchup issue, the I–V characteristics of on-chip ESD protection devices must be within the ESD protection design window [1], [2]. Silicon-controlled rectifier (SCR) device has widely been used as an efficient ESD protection device for its high ESD robustness within a small silicon area. Owing to the regenerative feedback of coupled n-p-n and p-n-p bipolar junction transistors (BJTs), the traditional SCR device features an extremely low holding voltage (V_h). However, the major challenge to apply SCR device for ESD protection in the HV applications is the latchup issue since its V_h is often much less than the supply voltage. During normal circuit operation, the noise might accidentally trigger the SCR-based ESD device, and then, the supply voltage kept the SCR path turned ON continuously. It would be burned out after a period of time under the circuit normal operating condition. Thus, the traditional SCR device was susceptible to latchup risk.

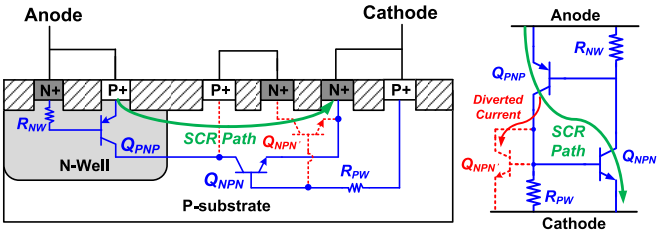

Fig. 1. Cross-sectional view and equivalent circuit diagram of a modified SCR with parasitic n-p-n BJT ($Q_{n\text{-}p\text{-}n'}$) in [3].

There have been some related studies to optimize the SCR device for high V_h [3]–[5]. In [3], a parasitic n-p-n BJT ($Q_{n\text{-}p\text{-}n'}$) was added into the traditional SCR device, as illustrated in Fig. 1. By partly diverting the SCR current through this parasitic BJT, it could break the positive feedback of the inherent p-n-p ($Q_{p\text{-}n\text{-}p}$) and n-p-n ($Q_{n\text{-}p\text{-}n}$) BJTs, and then increase the V_h. Based on such design concept, a modified SCR structure has been proposed in a 0.25-μm HV bipolar-CMOS-DMOS (BCD) process in this brief. One of the proposed SCRs can achieve a high V_h of up to ~30 V in the 100-ns transmission line pulsing (TLP) measurement results. In addition, whereas latchup event is a reliability issue with the time duration longer than milliseconds, the I–V characteristics of the proposed SCRs are also measured by curve tracer to validate their V_h [6]. Furthermore, transient latchup (TLU) test is applied to verify the measurement results [2].

In addition to the SCR-based design in this brief, the stacked configuration of low-voltage (LV) devices is another way to achieve high V_h for ESD protection in the HV applications, as reported in [7]–[9]. The ESD robustness and evaluation

Manuscript received September 30, 2017; revised November 20, 2017 and December 2, 2017; accepted December 15, 2017. Date of publication January 3, 2018; date of current version January 22, 2018. This work was supported by the Ministry of Science and Technology, Taiwan, under Contract MOST 105-2221-E-009-166 and Contract MOST 106-2622-8-009-007-TE1. The review of this brief was arranged by Editor E. Rosenbaum. *(Corresponding author: Ming-Dou Ker.)*

The authors are with the Institute of Electronics, National Chiao-Tung University, Hsinchu 30010, Taiwan (e-mail: ctdai.ee01g@g2.nctu.edu.tw; mdker@ieee.org).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TED.2017.2785121

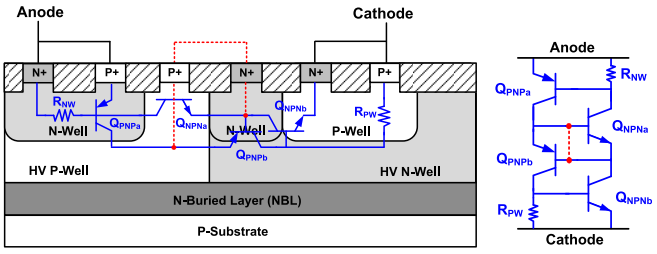

Fig. 2. Cross-sectional views and equivalent circuit diagrams of the proposed HVSCR_A, where the red dashed line is the p-n-connection path.

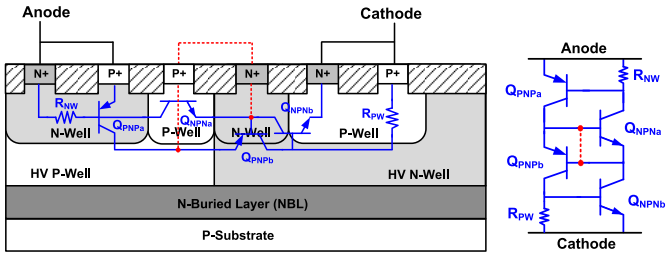

Fig. 3. Cross-sectional views and equivalent circuit diagrams of the proposed HVSCR_B, where the red dashed line is the p-n-connection path.

of latchup risk for the proposed SCRs will be discussed and compared with the performance of stacked LV devices in the 20-V circuit applications.

II. ESD Protection Devices

A. Device Structure of the Proposed SCR

Based on [3], a modified HVSCR structure realized with HV wells has been proposed in a 0.25-μm HV BCD process to achieve high V_h. The cross-sectional view and equivalent circuit diagram of the proposed type-A HVSCR (HVSCR_A) are shown in Fig. 2. The n-well (NW) and HV n-well (HVNW) are added to surround the p-well (PW) region of cathode side and both kept floating. The HV p-well (HVPW) region near anode side is surrounded by HVNW and N-buried layer for the isolation from p-substrate. The p-type doping (p^+) and the n-type doping (n^+) regions are added in HVPW and HVNW, respectively. By electrically connecting those doping regions, an additional path (p-n-connection path) from the collector of upper p-n-p BJT ($Q_{p\text{-}n\text{-}pa}$) to the collector of lower n-p-n BJT ($Q_{n\text{-}p\text{-}nb}$) is established, as red dashed line illustrated in Fig. 2. The flowing hole and electron carriers within the SCR path under the conduction state can be partly diverted through such additional path. It can suppress the positive feedback of the original SCR path for a higher V_h.

Further modified from the structure of the HVSCR_A, the proposed type-B HVSCR (HVSCR_B) illustrated in Fig. 3 is inserted with PW in HVPW to enhance the conduction efficiency of the additional path. Each proposed SCR is drawn with width of 200 μm and anode-to-cathode spacing of 14 μm. Compared with the traditional SCR, each proposed SCR is composed of a six-layer p-n-p-n-p-n structure. It forms a stacked SCR configuration in the equivalent circuit diagram that includes stacked p-n-p ($Q_{p\text{-}n\text{-}pa}$, $Q_{p\text{-}n\text{-}pb}$) and n-p-n ($Q_{n\text{-}p\text{-}na}$, $Q_{n\text{-}p\text{-}nb}$) BJTs.

B. I–V Characteristics of the Proposed SCR

Fig. 4(a) shows the 100-ns TLP measurement results of the HVSCR_A. The leakage currents are measured at 30 V. The TLP-measured V_h of the HVSCR_A without and with the p-n-connection path are 18.1 and 21.7 V, respectively. However, in the dc test results shown in Fig. 4(b), the dc-measured V_h of the HVSCR_A without and with p-n-connection path are 2.8 and 3.4 V, respectively. The reason causing such difference between TLP and dc test results is the increased BJT current

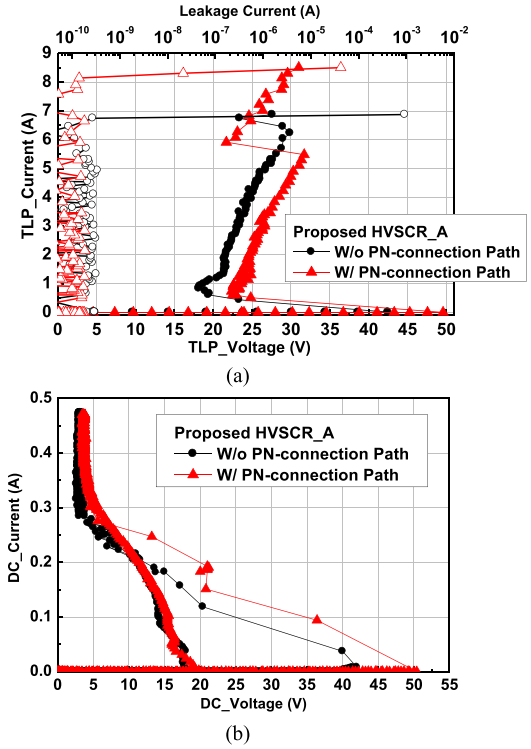

Fig. 4. *I–V* characteristics of the proposed HVSCR_A without or with p-n-connection path measured by (a) TLP system and (b) dc curve tracer.

gains of the SCR path induced by the Joule-heating effect in the dc measurement [6]. Accordingly, adding p-n-connection path in the HVSCR_A can only slightly increase its V_h. The TLP and dc measurement results of the HVSCR_B are shown in Fig. 5(a) and (b), respectively. The TLP-measured V_h of the HVSCR_B with p-n-connection path can rise to 33.8 V, and its dc-measured V_h is up to 21.4 V. Such high V_h is due to the enhanced conduction efficiency of the additional path in the HVSCR_B inserting PW in HVPW. Thus, adding p-n-connection path in the HVSCR_B can significantly increase its V_h. However, the TLP-measured failure current (I_{t2}) of the HVSCR_B with p-n-connection path is only 0.47 A.

The ESD levels of the proposed SCRs are further judged by the human-body model (HBM) ESD tester [10]. The detailed test results of the proposed SCRs in this brief are summarized in Table I. The proposed SCRs can exhibit high HBM ESD level of above 8 kV except the one with the highest V_h.

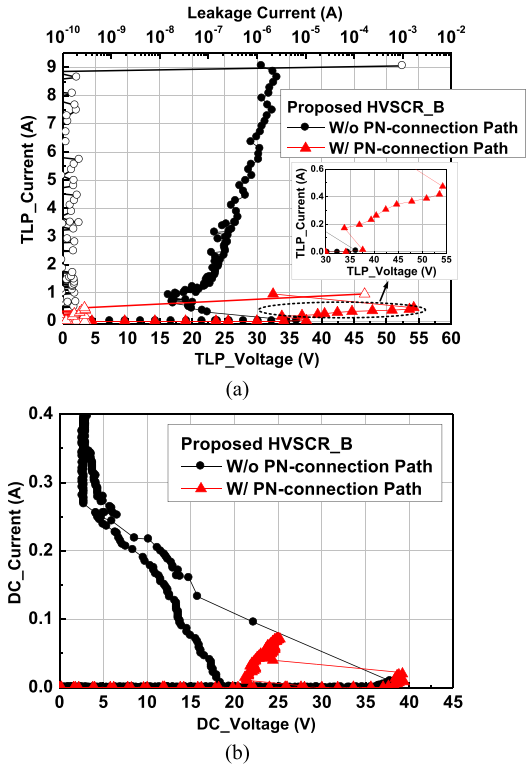

Fig. 5. *I–V* characteristics of the proposed HVSCR_B without or with p-n-connection path measured by (a) TLP system and (b) dc curve tracer.

TABLE I
COMPARISON OF TEST RESULTS OF THE PROPOSED SCR DEVICES

HVSCR Type	Type-A (W/o PN)	Type-A (W/ PN)	Type-B (W/o PN)	Type-B (W/ PN)
Width (μm)	200	200	200	200
Layout Area (μm^2)	9313	9313	9313	9313
V_{BD} (V)	36	48	34	34
DC V_h (V)	2.8	3.4	2.8	21.4
TLP V_h (V)	18.1	21.7	16.9	33.8
TLP I_{t2} (A)	6.74	8.14	8.84	0.47
HBM (V)	>8000 *	>8000 *	>8000 *	1000
HBM / Layout Area ($V/\mu m^2$)	>0.859	>0.859	>0.859	0.107
ESD Robustness	Good	Good	Good	Bad
Latchup Issue for 20-V Application	Risky	Risky	Risky	Safe

* limited by ESD test equipment.

The reason is that a high V_h may cause a high electric power to burn out the device during the conduction state, and hence degrade the device's ESD level. For the 20-V circuit applications, the proposed HVSCR_B with a high V_h of above 20 V can be applied for ESD protection and avoid latchup risk.

C. Transient Latchup Test on the Proposed SCR

To verify the TLP and dc measurement results, TLU test was applied in this brief. TLU test is an effective test method to evaluate the susceptibility of CMOS ICs to the latchup induced by transient noises [2]. The measurement setup for

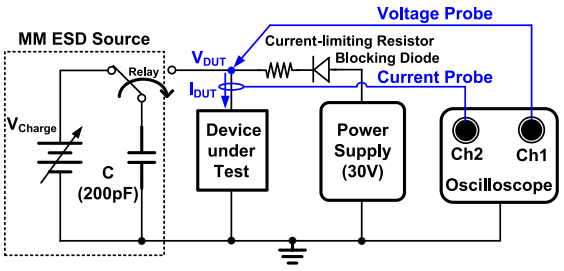

Fig. 6. Measurement setup of TLU test.

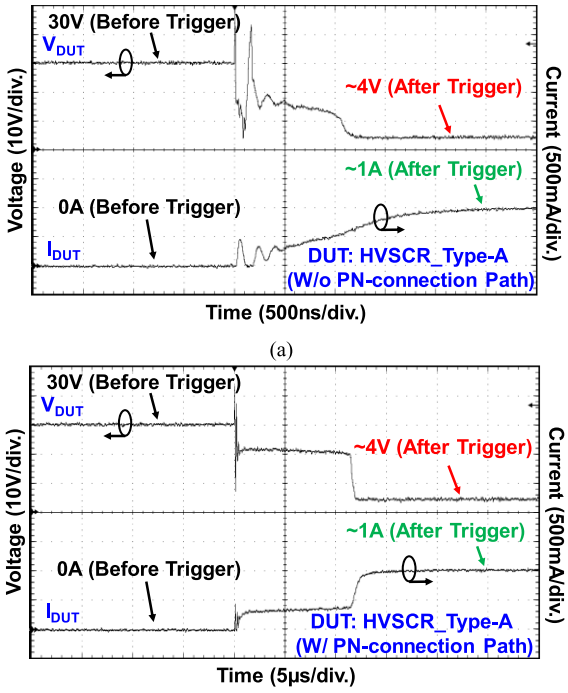

Fig. 7. Measured time-domain voltage and current waveforms of the proposed HVSCR_A (a) without and (b) with p-n-connection path.

TLU test is shown in Fig. 6. In the TLU test, the device under test (DUT) was initially biased at normal circuit operating voltage of 30 V. A transient noise is injected into DUT from the trigger source with a precharged voltage (V_{charge}). After the transient triggering, the DUT was driven into latchup state and clamped down the supply voltage. From the measured voltage and current waveforms shown in Fig. 7(a) and (b), the HVSCR_A without and with p-n-connection path both clamped the supply voltages up to ~4 V, which are similar to their values of dc-measured V_h. From the test results shown in Fig. 8(a) and (b), the HVSCR_B without and with the p-n-connection path clamped the supply voltages up to ~4 and ~24 V, respectively, which are also similar to their values of dc-measured V_h. In consequence, the TLU test has verified that the proposed SCR devices can greatly clamp the supply voltage to their own dc-measured V_h.

III. DISCUSSION

According to [7]–[9], the stacked configuration of LV devices is another way to achieve a high holding voltage

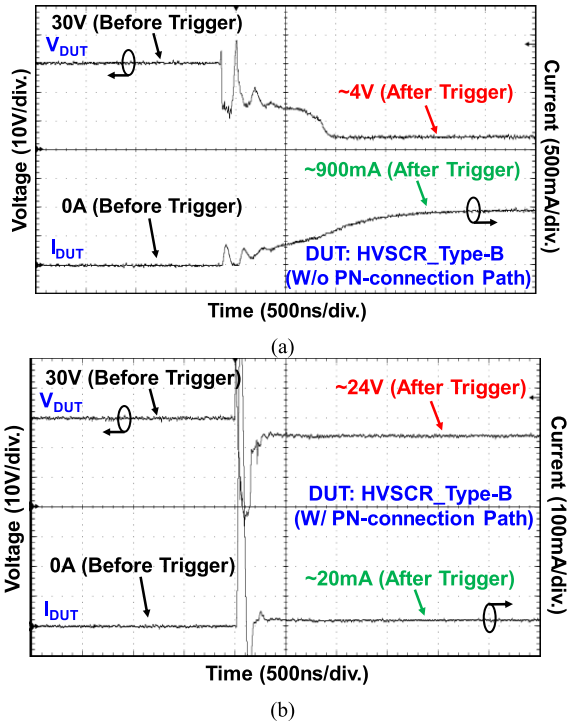

Fig. 8. Measured time-domain voltage and current waveforms of the proposed HVSCR_B (a) without and (b) with p-n-connection path.

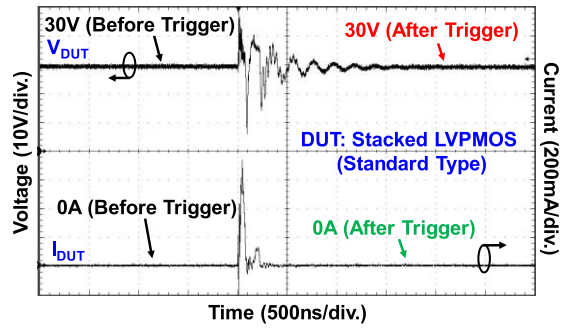

Fig. 9. Measured time-domain voltage and current waveforms of stacked standard LVPMOS.

for ESD protection in the HV applications. For the 20-V circuit applications, the test results of stacked LV p-type MOS (LVPMOS) with different structure modifications are listed in Table II. The total holding voltage and trigger voltage of stacked LVPMOS are the sum of a single device. The stacked number of LV device is adjusted to avoid the breakdown and latchup issue during normal circuit operation. From the comparison of test results among standard, type-3, and type-A stacked LVPMOS, the HBM ESD level per layout area can be improved by using the silicide blocking technique. In addition, the layout design of p-type guard ring that surrounds the stacked LVPMOS inappropriately can degrade its ESD performance. From the comparison of test results between the proposed SCRs and stacked LVPMOS, the HBM ESD level per layout area of stacked LVPMOS is higher than that of HVSCR_B with p-n-connection path when considering the latchup immunity in the 20-V circuit application. Moreover,

TABLE II
COMPARISON OF ESD PERFORMANCE OF DIFFERENT STACKED DEVICES

Device Type	LVPMOS (Standard) [7]	LVPMOS (Type-3) [8]	LVPMOS (Type-A) [9]
Technology	0.25μm HV BCD	0.25μm HV BCD	0.5μm HV BCD
W/L of each MOS (μm)	800/0.5	360/0.8	800/0.5
Silicide Blocking	No	Yes	No
P-Guard Ring for each MOS	Yes	Yes	No
Stack Number	4	3	3
Layout Area (μm^2)	12356	20288	9512
V_{BD} (V)	36	24.2	30.7
DC V_h (V)	37	27.6	26
TLP V_h (V)	36	26.19	25.9
TLP I_{t2} (A)	1.6	2.71	1.87
HBM (V)	2400	5000	3000
HBM / Layout Area ($V/\mu m^2$)	0.195	0.246	0.315
ESD Robustness	Good	Good	Good
Latchup Issue for 20-V Application	Safe	Safe	Safe

the TLU test result of stacked standard LVPMOS is shown in Fig. 9 to verify its latchup immunity. Therefore, stacked LV devices for ESD protection in the HV applications are an efficient way to meet the desired ESD protection design window.

IV. CONCLUSION

The characteristics of the proposed SCRs have been investigated in a 0.25-μm HV BCD technology. From the measurement results, it was found that the Joule-heating effect could dramatically decrease the V_h of the proposed SCR even if it was fabricated in a six-layer p-n-p-n-p-n structure. On the contrary, there is no degradation on V_h from the dc measurements in the previous studies with the stacked LV devices. Moreover, ESD robustness of the proposed SCR device is reduced when a high V_h is achieved. Consequently, developing special modification of such HV devices is inefficient to achieve both effective ESD protection and latchup-free design, as compared with the stacked configuration of LV devices, in this 0.25-μm HV BCD technology.

ACKNOWLEDGMENT

The authors would like to thank G.-L. Lin and Y.-N. Jou from Vanguard International Semiconductor Corporation for their valuable technical support and chip fabrication in HV process.

REFERENCES

[1] S. H. Voldman, *Latchup*. Hoboken, NJ, USA: Wiley, 2007.
[2] M.-D. Ker and S.-F. Hsu, *Transient-Induced Latchup in CMOS Integrated Circuits*. New York, NY, USA: Wiley, 2009.

[3] Y.-C. Huang and M.-D. Ker, "A latchup-immune and robust SCR device for ESD protection in 0.25-μm 5-V CMOS process," *IEEE Electron Device Lett.*, vol. 34, no. 5, pp. 674–676, May 2013, doi: 10.1109/LED.2013.2252456.

[4] Y.-F. Chang *et al.*, "High flexibility SCR clamp for ESD protection in BCD power technology," in *Proc. 36th EOS/ESD Symp.*, Tucson, AZ, USA, Sep. 2014, pp. 1–5.

[5] Z. Wang, M. Klebanov, R. B. Cooper, W. Liang, S. Courtney, and J. J. Liou, "No-snapback silicon-controlled rectifier for electrostatic discharge protection of high-voltage ICs," *IEEE Electron Device Lett.*, vol. 36, no. 11, pp. 1121–1123, Nov. 2015, doi: 10.1109/LED.2015.2479612.

[6] W. Y. Chen, M. D. Ker, and Y. J. Huang, "Investigation on the validity of holding voltage in high-voltage devices measured by transmission-line-pulsing (TLP)," *IEEE Electron Device Lett.*, vol. 29, no. 7, pp. 762–764, Jul. 2008, doi: 10.1109/LED.2008.2000910.

[7] C.-T. Dai and M.-D. Ker, "Study on ESD protection design with stacked low-voltage devices for high-voltage applications," in *Proc. 52nd IEEE IRPS*, Waikoloa, HI, USA, Jun. 2014, pp. EL.5.1–EL.5.2, doi: 10.1109/IRPS.2014.6861136.

[8] K.-N. Tang *et al.*, "Stacked low-voltage PMOS for high-voltage ESD protection with latchup-free immunity," in *Proc. APEMC*, Taipei, Taiwan, May 2015, pp. 325–328, doi: 10.1109/APEMC.2015.7175270.

[9] S.-F. Liao *et al.*, "Impact of guard ring layout on the stacked low-voltage PMOS for high-voltage ESD protection," in *Proc. 22nd ECCTD*, Trondheim, Norway, Aug. 2015, pp. 1–4, doi: 10.1109/ECCTD.2015.7300108.

[10] *Standard Test Method for Electrostatic Discharge (ESD) Sensitivity Testing: Human Body Model (HBM)-Component Level*, Standard ANSI/ESDA/JEDEC JS-001-2017, 2017.

Chia-Tsen Dai received the M.S. degree from National Chiao-Tung University, Hsinchu, Taiwan, in 2012, where he is currently pursuing the Ph.D. degree with the Institute of Electronics.

His current research interests include electrostatic discharge protection designs and latchup prevention in the high-voltage CMOS technologies.

Ming-Dou Ker (F'08) received the Ph.D. degree from the Institute of Electronics, National Chiao-Tung University (NCTU), Hsinchu, Taiwan, in 1993.

He is currently a Distinguished Professor with the Department of Electronics Engineering, NCTU, and also the Director of the Biomedical Electronics Translational Research Center, NCTU.

Prof. Ker is currently serving as an Editor for the IEEE TRANSACTIONS ON DEVICE AND MATERIALS RELIABILITY, and an Associate Editor for the IEEE TRANSACTIONS ON BIOMEDICAL CIRCUITS AND SYSTEMS.