Design of Power-Rail ESD Clamp With Dynamic Timing-Voltage Detection Against False Trigger During Fast Power-ON Events

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***Abstract*— The *RC*-based power-rail electrostatic discharge (ESD) clamp with nMOS of large size has been widely utilized to enhance the ESD robustness of CMOS integrated circuits. However, such circuit design that only detects the rising time of ESD pulse may be accidentally triggered in some conditions, such as fast power-ON, hot-plug, and envelope tracking applications. In this paper, a new power-rail ESD clamp circuit with transient and voltage detection function has been proposed and implemented in a 0.18-μm 1.8-V CMOS technology. The measurement results from the silicon chip have demonstrated that the new proposed power-rail ESD clamp circuit with adjustable minimum starting voltage ($V_{starting}$) can achieve good ESD robustness and avoid triggering under fast power-ON condition. In addition, the proposed circuit has a low standby leakage current of 270 nA at 125 °C under normal power-ON condition.**

***Index Terms*— Diode string, electrostatic discharge (ESD), ESD protection, power-rail ESD clamp circuit.**

I. Introduction

With the development of integrated circuits (ICs), improving circuit performance and reliability of IC products have been the ultimate goal in the IC industry. The electrostatic discharge (ESD) protection has become the major concern on the reliability of IC products [1], [2]. ESD specification of commercial IC products was required to be higher than 1 kV in the human-body-model (HBM) ESD test [3], [4]. To sustain good ESD robustness, the active power-rail ESD clamp circuit plays an important role in whole-chip ESD protection design [5], [6]. A typical on-chip power-rail ESD clamp circuit is shown in Fig. 1(a), where the detection mechanism is the *RC*-delay technique [5]. During ESD stress condition, the *RC*-delay technique keeps the voltage of V_{rc} at a logic *low*, and then turns ON the main ESD clamping MOSFET (M_{ESD}) to discharge ESD current. However, this circuit is unable to distinguish between the ESD pulse zapping to V_{DD} and the circuit operating under fast power-ON condition.

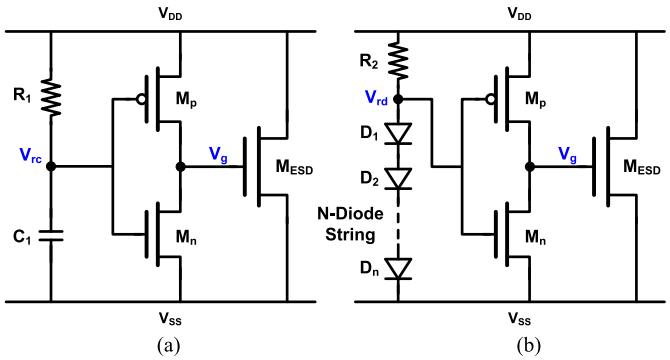

Fig. 1. Traditional power-rail ESD clamp circuits with (a) *RC*-delay technique [5] and (b) diode-triggered mechanism [7].

Besides the *RC*-delay technique, the voltage detection mechanism has also been adopted in power-rail ESD clamp circuit design [7]–[9]. A diode string was often used to detect the voltage level of V_{DD}. Fig. 1(b) shows a typical diode-triggered power-rail ESD clamp circuit. When the ESD stress voltage on V_{DD} is larger than the turn-ON voltage of the diode string, the ESD current flows through the diode string to cause a voltage drop across the resistor R_2. Then, the pMOS (M_p) can be turned ON and trigger ON the M_{ESD} to discharge ESD current. Under normal circuit operating condition, the operating voltage on V_{DD} must be lower than the turn-ON voltage of the diode string to keep the diode-triggered power-rail ESD clamp circuit in the OFF state. Unfortunately, the diode string often suffered a leakage issue [10], [11], especially in the high-temperature environment.

According to the previous reports, the traditional power-rail ESD clamp circuit with either detection mechanism should be further improved. In consideration of the false trigger event, several solutions had been reported to improve the traditional design, such as hybrid-triggered method [12]–[14], adjustable trigger voltage method [15], dynamic time-constant adjustment method [16], and adjustable holding voltage method [17].

In this paper, a new power-rail ESD clamp circuit against false trigger event is proposed. The design concept is illustrated in Fig. 2. The main ESD clamping MOSFET can only be triggered on during the ESD stress condition through the AND gate, when detecting the fast transient as well as the desired

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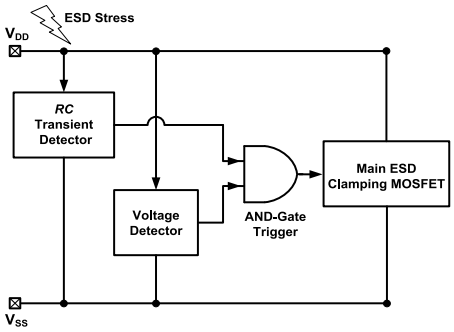

Fig. 2. Design concept of the proposed power-rail ESD clamp circuit with double detection mechanisms.

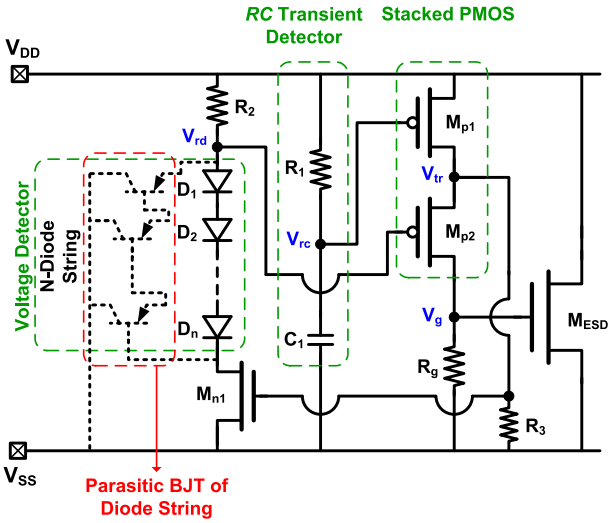

Fig. 3. Proposed power-rail ESD clamp circuit with double detection mechanisms.

voltage level. In the circuit implementation, this new design adopts the stacked pMOS to achieve the desired function for controlling the main ESD clamping MOSFET to discharge ESD current. The proposed power-rail ESD clamp circuit has been verified in a 0.18-μm 1.8-V CMOS process. By using the double detection mechanisms, the proposed power-rail ESD clamp circuit can exhibit high immunity against false trigger event during fast power-ON condition. In addition, it also has a lower standby leakage current under normal power-ON 1.8-V condition in comparison with the previous designs.

II. New Power-Rail ESD Clamp Circuit

A. Circuit Implementation

The power-rail ESD clamp circuit should be designed to meet the desired specification and also with the simplified circuit structure to save silicon area. Based on the design concept of Fig. 2, the proposed power-rail ESD clamp circuit is shown in Fig. 3, where the double detection mechanisms are adopted to overcome the false trigger issue. The proposed circuit can be divided into four parts, which include *RC* transient detector, voltage detector, stacked PMOS, and the main ESD clamping MOSFET. The voltage detector is composed of diode string, and the size of each diode is designed as 10×10 μm^2 in layout. To make sure that the power-rail

TABLE I
Design Parameters of Power-Rail ESD Clamp Circuits

Design parameters	*RC*-based power-rail ESD clamp circuit (Fig. 1a)	Diode-triggered power-rail ESD clamp circuit (Fig. 1b)	Proposed power-rail ESD clamp circuit (Fig. 3)
Capacitor	C_1=1 pF	none	C_1=1 pF
Resistor (Ω)	R_1=100 k	R_2=100 k	R_1=100 k R_2=100 k R_3=2 k R_g=2 k
PMOS W/L (μm /μm)	M_p=80/0.3	M_p=80/0.3	M_{p1}=80/0.3 M_{p2}=80/0.3
NMOS W/L (μm /μm)	M_n=20/0.35	M_n=20/0.35	M_{n1}=2/0.35
Diode (D_n) W*L (μm *μm)	none	10*10	10*10
Diode number	none	4	4
Main ESD clamping MOSFET W/L (μm /μm)	M_{ESD}=400/0.35	M_{ESD}=400/0.35	M_{ESD}=400/0.35

ESD clamp circuit is in OFF state under normal power-ON 1.8-V condition, the diode string in the proposed power-rail ESD clamp circuit is selected with four diodes. The typical *RC* time constant of 100 ns is selected with the resistor (R_1) of 100 kΩ and the capacitor (C_1) of 1 pF. The resistor (R_2) that connects diode string is selected as 100 kΩ. By using the silicide blocking option supported by foundry, ESD robustness of the main ESD clamping MOSFET (M_{ESD}) can be further improved [18]. In this paper, the channel width of M_{ESD} is designed as 400 μm with silicide blocking. The stacked pMOS M_{p1} and M_{p2} are used to control the gate of M_{ESD}. The channel widths of M_{p1} and M_{p2} are both selected as 80 μm to ensure that the M_{ESD} can be triggered on quickly under ESD stress conduction. The nMOS M_{n1} with channel width of 2 μm is used to reduce the standby leakage current along the diode string. The R_3 used to trigger the M_{n1} is selected as 2 kΩ. To ensure that the M_{ESD} is triggered on by the controlling circuit, not by the coupling effect through the parasitic capacitance of M_{ESD}, the trigger resistor (R_g) is chosen as 2 kΩ. The design parameters of the devices among the power-rail ESD clamp circuits are listed in Table I, and the detailed discussion on the design parameters is shown in Section II-B.

B. Circuit Simulation

1) ESD-Like Waveform Condition: In the simulation of ESD-like waveform, the rising time of 10 ns and the pulsewidth of 100 ns are selected on the basis of HBM. In addition, the drain-substrate junction breakdown voltage of nMOS in this process is about 8 V. Therefore, the voltage of ESD-like waveform is selected as 5 V to avoid drain-substrate junction breakdown of M_{ESD} during the ESD stress condition. For consideration of the circuit design, the characteristic of the proposed power-rail ESD clamp circuit is influenced by the trigger resistor R_g, the diode string, and the resistor R_2. By using the *HSPICE* simulation, the affecting factors of the proposed circuit are discussed in this section.

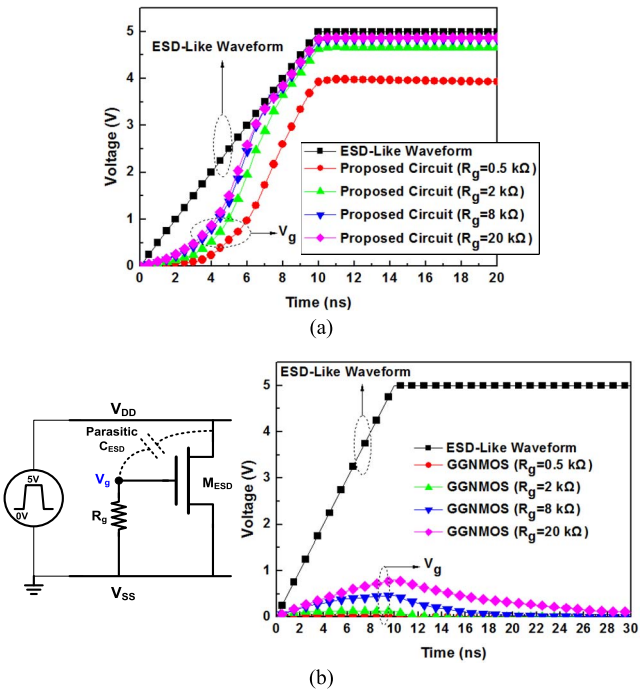

Fig. 4. Simulation results of the voltage on the node V_g of (a) proposed power-rail ESD clamp circuit with different values of the trigger resistor (R_g) and (b) GGNMOS with different values of the trigger resistor (R_g).

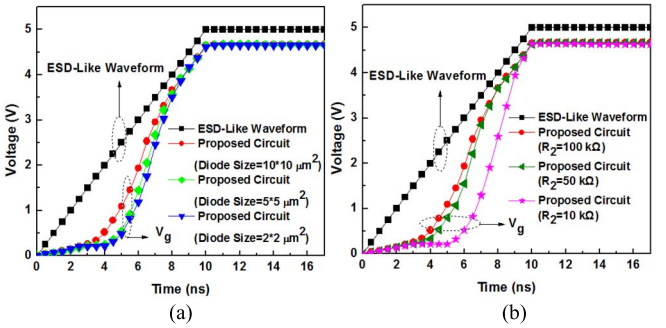

Fig. 5. Simulation results of the voltage on the node V_g of the proposed power-rail ESD clamp circuit with (a) three different sizes of diode in the diode string ($R_2 = 100$ kΩ) and (b) three different values of R_2 (diode size $= 10 \times 10$ μm^2) during the ESD-like waveform condition.

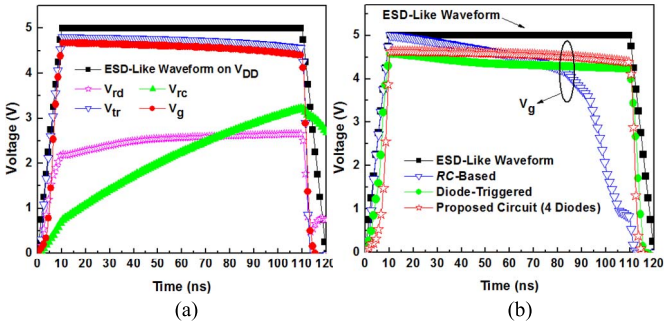

Fig. 6. Simulation results of (a) voltage on each node of the proposed power-rail ESD clamp circuit during the ESD-like waveform condition and (b) voltage on the node V_g of the three power-rail clamp circuits during the ESD-like waveform condition.

One affecting factor is the trigger resistor R_g, the value of which depends on the turn-ON speed and the coupling effect of $M_{\rm ESD}$ under ESD-like waveform condition. In order to decide the value of R_g, the simulation results that are compared with gate-grounded nMOS (GGNMOS) are shown in Fig. 4. Except the value of R_g, the parameters of the proposed circuit are fixed as listed in Table I. In Fig. 4, large R_g can enhance turn-ON speed of the circuit under ESD-like waveform, but cause a severe coupling effect through the parasitic capacitance to bias the gate of $M_{\rm ESD}$. To ensure that the $M_{\rm ESD}$ can be triggered on quickly under ESD stress conduction without severe coupling effect, the value of R_g is chosen as 2 kΩ. Another affecting factor is the diode string. The traditional P+/NW diode has the parasitic vertical P-N-P BJT structure, which is shown in Fig. 3. The diode string has been modeled in P-N-P BJT model, and the foundries have also provided the corresponding SPICE models to circuit designers. Based on the P-N-P BJT model with device parameters provided from foundry, the junction size of each diode in the diode string is selected as 2×2, 5×5, and 10×10 μm^2. Except the diode size of the diode string, the parameters of the proposed circuit are fixed as listed in Table I for simulation. Fig. 5(a) shows the *HSPICE*-simulated voltages on the node V_g of the proposed circuit with different sizes of the diode string. A large-sized diode can improve the turn-ON speed of the proposed circuit during ESD stress. Thus, the layout size of each diode is chosen as 10×10 μm^2. The last affecting factor is the resistor R_2, which uses to trigger ON the M_{p2}. The values of the R_2 are varied in 10, 50, and 100 kΩ. Fig. 5(b) shows the simulated voltages on the node V_g of the proposed circuit with three different resistor values of the R_2. Small R_2 will degrade the turn-ON speed of the proposed circuit. Thus, the value of R_2 is selected as 100 kΩ.

To observe the circuit behavior under ESD-like waveform conditions, Fig. 6(a) shows the simulated voltages on each node of the proposed circuit with transient waveform. During the ESD stress condition, the voltage level of the node $V_{\rm rc}$ is increased much slower than the voltage level on the $V_{\rm DD}$. Due to the delay of the voltage increase on the node $V_{\rm rc}$, the M_{p1} device is turned ON and conducts a voltage into the node $V_{\rm tr}$ to turn-ON the M_{n1} device. When the voltage level of ESD waveform is higher than the normal operating voltage, it will trigger ON the diode string to keep the voltage on the node $V_{\rm rd}$ lower than $V_{\rm DD}$. Because the voltage level on the node $V_{\rm rd}$ is lower than $V_{\rm DD}$, the M_{p2} device is turned ON to conduct a voltage into the node V_g to trigger ON the $M_{\rm ESD}$. Fig. 6(b) shows the performance comparison among the *RC*-based power-rail ESD clamp circuit, the diode-triggered power-rail ESD clamp circuit, and the proposed power-rail ESD clamp circuit with four diodes during ESD-like waveform condition. These three power-rail ESD clamp circuits are turned ON completely during the ESD stress condition.

2) Normal Power-ON Condition: On the contrary, the normal power-ON voltage waveform has a rise time in the order of millisecond (ms) and a lower voltage (1.8 V). Fig. 7(a) shows the simulated voltages on the each node of the proposed circuit under normal power-ON condition. The rising time of normal power-ON condition is chosen as 1 ms. With the slow-rising

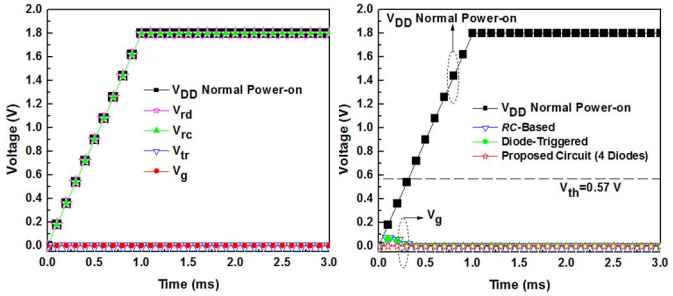

Fig. 7. Simulation results of (a) voltage on each node of the proposed power-rail ESD clamp circuit under 1.8-V normal power-ON condition and (b) voltage on the node V_g of the three power-rail clamp circuits under 1.8-V normal power-ON condition.

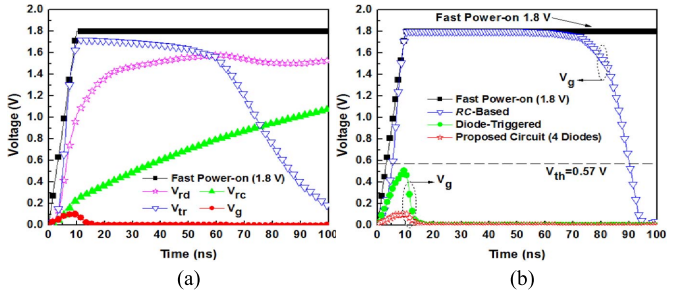

Fig. 8. Simulation results of (a) voltage on each node of the proposed power-rail ESD clamp circuit during fast power-ON condition and (b) voltage on the node V_g of the three power-rail ESD clamp circuits during fast power-ON condition.

power-ON voltage, the voltage at the node V_{rc} will be able to follow the V_{DD} voltage in time. The normal power-ON voltage is lower than the turn-ON voltage of the diode string, which will turn OFF the M_{p2}. Since the M_{p1} and the M_{p2} are kept in OFF state, the voltage level on the node V_g is kept at 0 V to turn OFF the M_{ESD}. Fig. 7(b) shows voltage level on the node V_g among the three power-rail ESD clamp circuits under normal power-ON condition. These three power-rail ESD clamp circuits are kept in OFF state under 1.8-V normal power-ON condition.

3) Fast Power-ON Condition: Under the fast power-ON condition, the power-ON voltage waveform has a rise time in the order of nanosecond (ns) with normal operating voltage level. Thus, the rising time of 10 ns and the voltage of 1.8 V are selected for simulation. Fig. 8(a) shows the simulated voltages on each node of the proposed circuit during fast power-ON condition. The fast power-ON waveform will turn-ON the M_{p1} device ($1.8\ \text{V} - V_{rc} > V_{th(Mp1)}$), but it cannot trigger ON the diode string ($1.8\ \text{V} < nV_{ON(diode)}$). So, the voltage level on the node V_g is kept at about 0 V to turn OFF the M_{ESD}. Fig. 8(b) shows the comparison of simulated voltage on the node V_g among three power-rail ESD clamp circuits during the fast power-ON condition. The simulation results show that the *RC*-based power-rail ESD clamp circuit has been falsely triggered on during the fast rising period, and the peak voltage on the node V_g of diode-triggered power-rail ESD clamp circuit is higher than the proposed power-rail ESD clamp circuit. The large peak voltage on the node V_g during the fast power-ON condition will increase the risk of false trigger event.

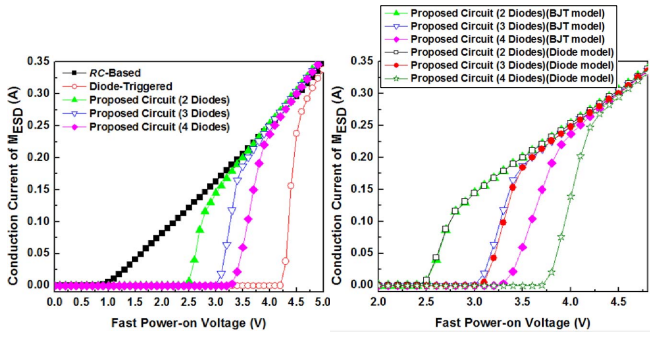

Fig. 9. Simulation results of (a) conduction current among the five power-rail ESD clamp circuits during different fast power-ON voltages and (b) comparisons between diode model and P-N-P BJT model in the diode string of the proposed power-rail ESD clamp circuits during different fast power-ON voltages.

Consequently, the new proposed power-rail ESD clamp circuit has the best immunity against false trigger during the fast power-ON conditions.

An in-deep discussion, the minimum starting voltage ($V_{starting}$) means that the turn-ON voltage of power-rail ESD clamp circuit is an important factor. As shown in Figs. 6(a), 7(a), and 8(a), if the $V_{tr} - V_{rd} < V_{th(Mp2)}$, the proposed power-rail ESD clamp circuit will be kept in OFF state. The minimum starting voltage depends on the turn-ON voltage of the diode string and turn-ON voltage of M_{p1}. Thus, the minimum trigger voltage of the proposed power-rail ESD clamp circuit can be expressed as

$$\begin{aligned} V_{starting} &= V_{ds(Mn1)} + nV_{ON(diode)} + V_{ON(Mp1)} \\ &\approx nV_{ON(diode)} + V_{ON(Mp1)} \end{aligned} \quad (1)$$

where n and $V_{ON(diode)}$ are the number and the turn-ON voltage of the diode, respectively. Fig. 9(a) shows that the simulation results of *RC*-based power-rail ESD clamp circuit, diode-triggered power-rail ESD clamp circuit, and the proposed circuit with four diodes under different fast power-ON voltage conditions. By adjusting the number of diodes in the detection circuit, the proposed power-rail ESD clamp circuit can be utilized under different supply voltages. The proposed circuit with two diodes and the one with three diodes are also simulated, as shown in Fig. 9(a). The $V_{starting}$ was defined to be the voltage at which the device can conduct 20-mA current. Thus, the minimum starting voltage of the *RC*-based power-rail ESD clamp circuit, the diode-triggered power-rail ESD clamp circuit, and the proposed power-rail ESD clamp circuit with diode numbers of 2, 3, and 4 are 1.3, 4.2, 2.5, 3.1, and 3.3 V, respectively. In this 1.8-V application, the proposed circuit can further reduce the numbers of diode. However, for the pMOS turn-ON voltage ($V_{ON(Mp1)}$) of 1.3 V ($1.3\ \text{V} - V_{rc} > V_{th(Mp1)}$) and single-diode turn-ON voltage of 0.6 V, the minimum starting voltage of the proposed power-rail ESD clamp circuit with four diodes is 3.3 V, which is lower than the expected value (3.6 V). The reason is shown in Fig. 9(b), where the comparisons between diode model and p-n-p BJT model in the diode string are presented. The simulation results show that increasing the number of diodes will degrade the

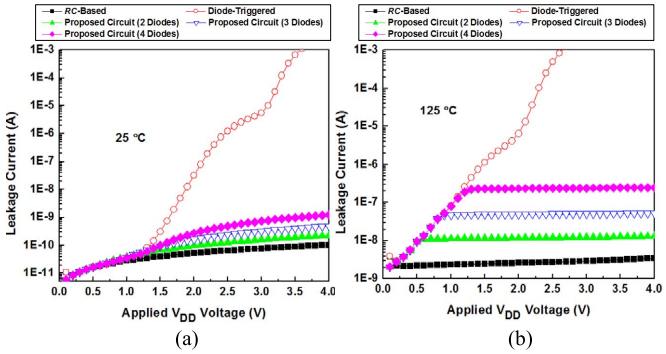

Fig. 10. Simulated dc *I–V* curves of the *RC*-based power-rail ESD clamp circuit, diode-triggered power-rail ESD clamp circuit, and the three proposed power-rail ESD clamp circuits at (a) room temperature (25 °C) and (b) high temperature (125 °C).

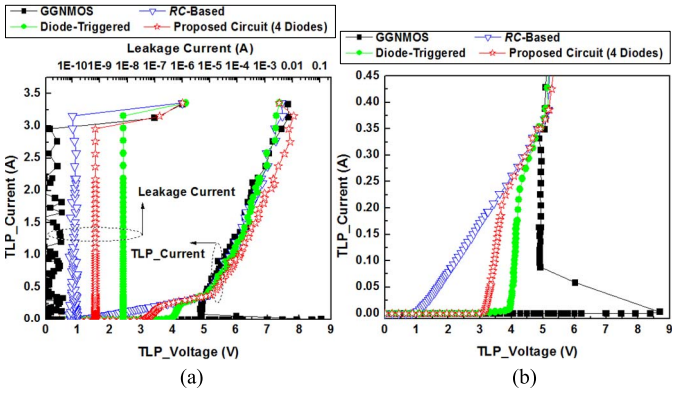

Fig. 11. TLP measured *I–V* characteristics of (a) stand-alone nMOS (GGNMOS), *RC*-based power-rail ESD clamp circuit, diode-triggered power-rail ESD clamp circuit, and the proposed power-rail ESD clamp circuit with four diodes and (b) zoomed-in illustration for the minimum starting voltage (V_{starting}) and trigger voltage (V_{t1}).

minimum starting voltage due to the parasitic leakage path of P+/NW diode.

4) Standby Leakage: The standby leakage current with dc bias of the three power-rail ESD clamp circuits are simulated and shown in Fig. 10. The *RC*-based power-rail ESD clamp circuit has the lowest leakage current, closely followed by the proposed circuit, while the diode-triggered power-rail ESD clamp circuit has the highest one. Though the diode-triggered power-rail ESD clamp circuit has large R_2 and four diodes to reduce leakage current, it still suffered the leakage issue at high temperature (125 °C). The leakage current of the proposed circuit with four diodes at room temperature (25 °C) and high temperature (125 °C) under 1.8-V bias is 190 pA and 230 nA, respectively. The leakage current is dominated by the diode string due to the leakage path of the P+/NW diode. By using the M_{n1} and double-detection mechanism, the proposed circuit definitely has a lower leakage current. Besides, the proposed circuit can reduce the number of diodes to further decrease the leakage current under normal power-ON 1.8-V condition.

III. Experimental Results

The power-rail ESD clamp circuits studied in this paper are implemented in a 0.18-μm 1.8-V CMOS process. The resistor is adopted by the P-type poly resistor, and the capacitor is realized by the metal–insulator–metal capacitor. The diode is selected as traditional p+/n-well diode, and its junction area is designed as 10×10 μm^2. In order to compare with diode-triggered power-rail ESD clamp circuit and verify the P-N-P BJT model of the diode string, the diode number of the proposed circuit is selected as four. The channel width of the main ESD clamping MOSFET is designed as 400 μm with silicide blocking.

A. Transmission-Line Pulsing (TLP) Measurement

To investigate the device behavior during ESD zapping stress, a transmission-line-pulsing (TLP) generator gave an ESD-like waveform with pulsewidth of 100 ns and rising time of 10 ns. The important parameters of TLP measurement *I–V* curve are trigger voltage (V_{t1}), holding voltage (V_h), and second breakdown current (I_{t2}), respectively. Fig. 11 shows the comparison of TLP *I–V* curves among all power-rail ESD clamp circuits and a stand-alone GGNMOS. In Fig. 11, the GGNMOS has the snapback phenomenon but the others have not. The GGNMOS has the snapback phenomenon because it discharged the ESD current by the junction breakdown operation of the parasitic BJT. The minimum starting voltage (V_{starting}) was defined to be the voltage at which the device can conduct 20-mA current. Hence, the V_{t1} of GGNMOS and the V_{starting} of *RC*-based power-rail ESD clamp circuit, diode-triggered power-rail ESD clamp circuit, and proposed power-rail ESD clamp circuit with four diodes are 8.7, 1.3, 4.1, and 3.2 V, respectively, which corresponds to the simulated value. Besides, the holding voltage of GGNMOS is 4.9 V. In the ESD level, the ESD robustness only depends on the dimension of M_{ESD}. Consequently, the second breakdown current is the same for all test circuits with the same device dimension of M_{ESD} (400 μm). All these measurement results are listed in Table II. According to the measurement results, the turn-ON behavior of GGNMOS and diode-triggered power-rail ESD clamp circuit is slower than the *RC*-based power-rail ESD clamp circuit and the proposed ESD power-rail clamp circuit. However, the V_{starting} of *RC*-based power-rail ESD clamp circuit is lower than normal operating voltage, which has a high risk of the false trigger event. Therefore, the proposed power-rail ESD clamp design has a good ESD robustness, suitable turn-ON speed, and without false trigger issue.

B. ESD Robustness

The component-level HBM ESD robustness of the fabricated ESD circuits has been tested. In this test, the failure criterion is defined as 20% increase from the original leakage current under 1.8-V VDD bias. The ESD test results of all power-rail ESD clamp circuits are also listed in Table II. The HBM ESD robustness of GGNMOS, *RC*-based power-rail ESD clamp circuit, diode-triggered power-rail ESD clamp circuit, and proposed power-rail ESD clamp circuit are all the same of 5.2 kV. The ESD robustness of all test circuits is the same due to the same device dimension of the main ESD clamping MOSFET for ESD current discharge.

TABLE II
MEASURED RESULTS OF STAND-ALONE nMOS (GGNMOS) AND POWER-RAIL ESD CLAMP CIRCUITS

Test Circuits	V_{t1} (V)	$V_{starting}$ (V)	V_h (V)	I_{t2} (A)	HBM (kV)
GGNMOS	8.7	none	4.9	3.1	5.2
RC-based power-rail ESD clamp circuit (Fig. 1a)	none	1.2	none	3.1	5.2
Diode-triggered power-rail ESD clamp circuit (Fig. 1b)	none	4.1	none	3.1	5.2
Proposed power-rail ESD clamp circuit with 4 diodes (Fig. 3)	none	3.2	none	3.1	5.2

TABLE III
VF-TLP MEASURED RESULTS OF STAND-ALONE nMOS (GGNMOS) AND POWER-RAIL ESD CLAMP CIRCUITS

Test Circuits	VF-V_{t1} (V)	VF-$V_{starting}$ (V)	VF-V_h (V)	VF-I_{t2} (A)
GGNMOS	5.4	none	4.7	5.6
RC-based power-rail ESD clamp circuit (Fig. 1a)	none	1.2	none	5.6
Diode-triggered power-rail ESD clamp circuit (Fig. 1b)	none	1.8	none	5.6
Proposed power-rail ESD clamp circuit with 4 diodes (Fig. 3)	none	2.2	none	5.6

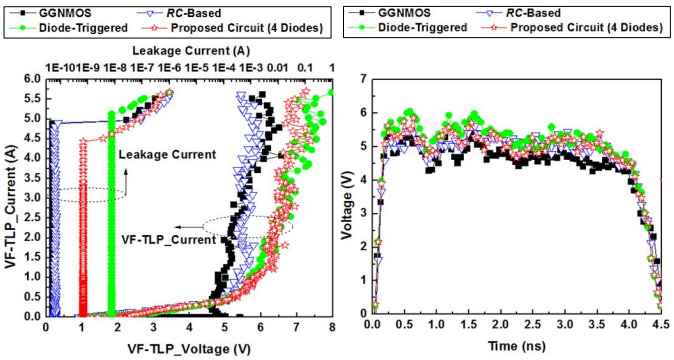

Fig. 12. VF-TLP measured results of (a) *I–V* characteristics of stand-alone nMOS (GGNMOS), *RC*-based power-rail ESD clamp circuit, diode-triggered power-rail ESD clamp circuit, and the proposed power-rail ESD clamp circuit with four diodes and (b) voltage waveform under 500-mA VF-I_{t2} condition.

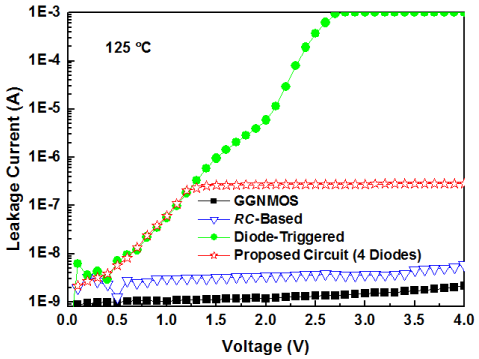

Fig. 13. Measured dc *I–V* curve of the *RC*-based power-rail ESD clamp circuit, diode-triggered power-rail ESD clamp circuit, and the proposed power-rail ESD clamp circuit with four diodes at 125 °C.

C. VF-TLP and Transient Overshoot Measurement

Besides the component-level HBM, the charge-device model (CDM) is another important ESD issue. To characterize the CDM robustness of test circuits, the very-fast TLP (VF-TLP) test method has been reported [19], [20]. The VF-TLP is an important measurement method that is utilized to verify the performance of the ESD protection devices turn-ON behavior during ESD stress with short-pulsewidth. The second breakdown current of VF-TLP (VF-I_{t2}) means the maximum sustaining current during CDM test, which can be related to the CDM level. In this paper, the rising time of 200 ps and the pulsewidth of 5 ns is selected. Fig. 12(a) shows the comparison of VF-TLP *I–V* curves among power-rail ESD clamp circuits. In the ESD stress of short-pulsewidth, the VF-V_{t1} of GGNMOS and the VF-$V_{starting}$ of *RC*-based power-rail ESD clamp circuit, diode-triggered power-rail ESD clamp circuit, and the proposed power-rail ESD clamp circuit with four diodes are 5.4, 1.2, 1.8, and 2.2 V, respectively. The trigger voltage of GGNMOS and minimum starting voltage of diode-triggered power-rail ESD clamp circuit and the proposed power-rail ESD clamp circuit have the degradation phenomenon due to the parasitic capacitance of the M_{ESD}. The minimum starting voltage of these circuits is shifted more than 30%, as compared to the TLP measurement results. According to the VF-I_{t2} of 5.6 A, the proposed ESD clamp circuit has a good CDM robustness. All these measurement results are listed in Table III.

For observing the characteristics of the test circuits in initial turn-ON condition during the very-fast ESD transient, the voltage waveform has been shown in Fig. 12(b), which is chosen under 500-mA condition of VF-TLP current. As shown in Fig. 12(b), the voltage of all test circuits has no significant overshoot, and the clamping voltage is about 5 V. The overshoot voltage is not obvious under the small ESD current.

D. DC I–V Curve

Fig. 13 shows the dc *I–V* curves of the power-rail ESD clamp circuits at high temperature (125 °C). In this paper, the operational voltage is selected as 1.8 V, so the leakage current at 1.8 V should be noticed. In Fig. 13, the leakage current of the diode-triggered power-rail ESD clamp circuit has dramatically increased because the diode string is turned ON to trigger ON the M_{ESD}. For the measured results at 125 °C, the leakage currents of GGNMOS, *RC*-based power-rail ESD clamp circuit, diode-triggered power-rail ESD clamp circuit, and the proposed power-rail ESD clamp circuit with four diodes are 1, 3, 2837, and 270 nA, respectively. The leakage current is dominated by the diode string due to the leakage path of the P+/NW diode. In spite of using large R_2 and four diodes, the diode-triggered power-rail ESD clamp circuit

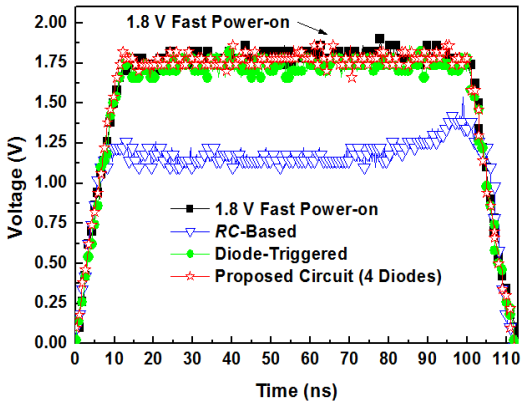

Fig. 14. Measured voltage waveform of the three fabricated power-rail ESD clamp circuits during 1.8-V fast power-ON waveform.

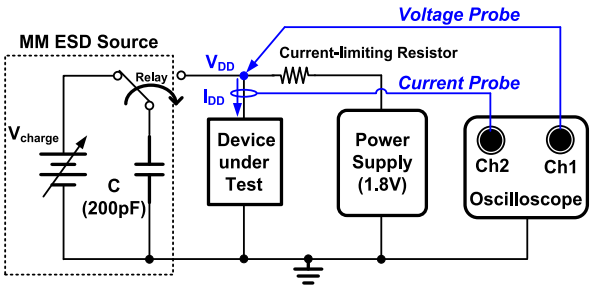

Fig. 15. Component-level TLU measurement setup with bipolar trigger [23].

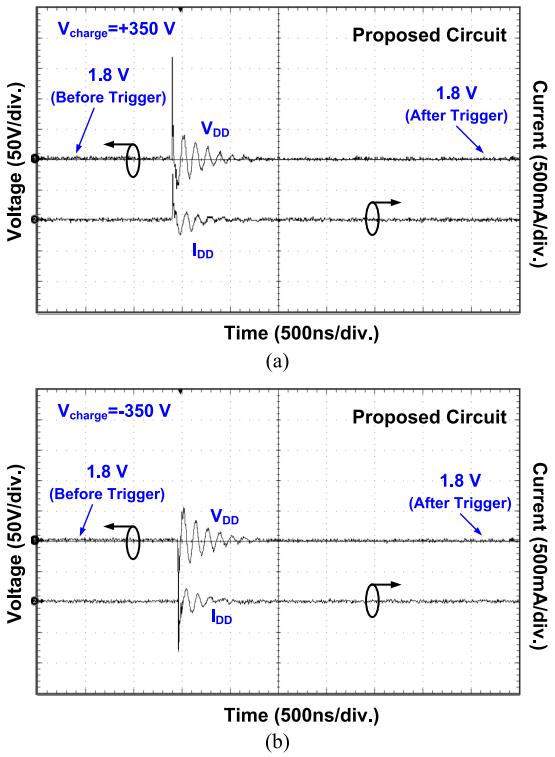

Fig. 16. Measured time-domain voltage and current waveforms of the proposed circuit under TLU measurement with V_{charge} of (a) +350 V and (b) −350 V.

could not reduce the leakage current. By using the M_{n1} and double-detection mechanism, the proposed circuit definitely decreases leakage current. In addition, the leakage current of diode string can be further reduced by additional circuitry, such as cladded diode string [10], snubber-clamped diode string [21], or resistor-shunted diode string [22]. Accordingly, the leakage issue through the diode string can be effectively reduced by those additional bias techniques for the power-rail ESD clamp circuit being applied to other processes.

E. Fast Power-ON Test and Transient-Induced Latchup (TLU) Measurement

To investigate the turn-ON behavior of the power-rail ESD clamp circuits under the fast power-ON condition, using a function generator to create a waveform with low voltage and nanoscale rising time. The pulsewidth of 100 ns and the rise time of 10 ns are selected in this paper, and the voltage is chosen as 1.8 V. Fig. 14 shows the measured results of power-rail ESD clamp circuits during the fast power-ON condition. In Fig. 14, the voltage waveform of *RC*-based power-rail ESD clamp circuit has been dropped to 1.1 V because it is accidentally triggered on by the fast rising pulse. The diode-triggered ESD clamp circuit and the proposed ESD clamp circuit have no false trigger under such a fast power-ON test.

The latchup-like issue is another factor that needs to be considered. According to previous studies, the power-rail ESD clamp circuit with feedback technique to enhance the turn-ON time would suffer some latchup-like failures after transient-induced latchup (TLU) test [23]. Thus, the proposed power-rail ESD clamp circuit without enhancing turn-ON time technique is free from latchup-like issue. To observe latchup-like issue, the TLU measurement has been used to investigate the susceptibility of device under normal operation condition with noise coupling [24]. The measurement setup for TLU test is shown in Fig. 15. The device under test (DUT) is initially biased at normal circuit operating voltage of 1.8 V. The current-limiting resistance is selected as 5Ω. The transient noise is created by the machine model ESD source. The voltage and current waveforms of the DUT are monitored by the oscilloscope. The precharge voltage (V_{charge}) is selected as 350 V. The TLU measurement results of the proposed power-rail ESD clamp circuit with four diodes are shown in Fig. 16. The latch-on state does not occur under positive or negative stress condition because the minimum starting voltage of the proposed circuit is higher than the supply voltage, and the feedback technique is not applied in this design.

IV. Discussion

Table IV presents performance comparisons between the proposed circuit and the traditional circuits. Only with the single-detection mechanism of power-rail ESD clamp circuit has some deadly shortcoming. The *RC*-based power-rail ESD clamp circuit has the risk of false trigger, and the diode-triggered power-rail ESD clamp circuit has a large leakage current under normal circuit operating condition. These flaws can be solved by the proposed power-rail ESD clamp circuit.

TABLE IV
PERFORMANCE COMPARISONS BETWEEN THE PROPOSED POWER-RAIL ESD CLAMP CIRCUIT AND TRADITIONAL POWER-RAIL ESD CLAMP CIRCUITS

	RC-based power-rail ESD clamp circuit (Fig. 1a)	Diode-triggered power-rail ESD clamp circuit (Fig. 1b)	Proposed power-rail ESD clamp circuit (Fig. 3)
Layout Area (μm^2)	2392	2970	3227
Leakage	Low	high	low
Fast power-on issue	risk	immune	immune
Adjustable minimum starting voltage	NO	YES	YES

This new design with simple structure to accomplish the double-detection mechanisms can successfully overcome the false trigger. Furthermore, by adjusting the diode number in the diode string, the proposed circuit can be applied to different supply voltages with limited leakage current. Therefore, the proposed power-rail ESD clamp circuit can achieve better performance for whole-chip ESD protection in IC products.

V. CONCLUSION

The proposed power-rail ESD clamp circuit adopts both the transient detection and voltage detection with stacked pMOS to control the main ESD clamping MOSFET. As compared to the traditional power-rail ESD clamp circuits, the experimental results in a 0.18-μm 1.8-V CMOS process have successfully verified that the proposed power-rail ESD clamp circuit can sustain good ESD robustness without suffering the false trigger issue. The standby leakage current along the proposed power-rail ESD clamp circuit under the normal circuit operating condition has also been effectively reduced by adding a feedback nMOS in series into the diode string. The new power-rail ESD clamp circuit proposed in this paper is a useful ESD protection solution to achieve the whole-chip ESD protection design in CMOS IC products.

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