Self-Reset Transient Detection Circuit for On-Chip Protection Against System-Level Electrical-Transient Disturbance

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***Abstract*—A new self-reset transient detection circuit for on-chip protection against a system-level electrical-transient disturbance is proposed. This circuit is designed to detect the occurrence of system-level electrical-transient disturbance events, and automatically reset the system to initial state for the next detection. In addition, the reset time can be adjusted to meet the different requests of system recovery time in microelectronic products. The circuit performance has been investigated by HSPICE simulation and verified in silicon chip. The experiment results in a 0.18-μm complementary metal-oxide semiconductor (CMOS) process with 1.8-V devices have confirmed the detection and self-reset functions of the proposed on-chip self-reset transient detection circuit under system-level electrostatic discharge and electrical-fast-transient testing conditions. With firmware co-design, the proposed detection circuit can provide an effective on-chip solution to recover the microelectronic system from the system-level transient disturbance-induced abnormal state to a known stable state. Therefore, the immunity level of microelectronic products equipped with CMOS integrated circuits against electromagnetic susceptibility can be effectively enhanced.**

***Index Terms*—Electrical-fast-transient (EFT) test, electromagnetic susceptibility (EMS), electrostatic discharge (ESD), system-level ESD test, transient detection circuit.**

I. Introduction

ELECTROMAGNETIC susceptibility (EMS) has become an important reliability issue in modern microelectronic products equipped with CMOS integrated circuits (ICs). With more various applications of microelectronic products, the equipped CMOS ICs suffer more electrical-transient disturbances in the complex end-user environments [1], [2]. In addition, the progress of CMOS technology that continuously scales down the transistor dimensions makes the CMOS ICs more susceptible to the EMS events. It has been found that such electrical transients can cause hardware damages or system malfunctions of the internal CMOS ICs, even if the CMOS ICs have passed the component-level electrostatic discharge (ESD) specifications [3]–[10].

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TABLE I
CLASSIFICATIONS OF SYSTEM-LEVEL ESD AND EFT TEST RESULTS

Criterion	Classification
Class A	Normal performance within limits specified by the manufacturer, requestor or purchaser.
Class B	Temporary loss of function or degradation of performance which ceases after the disturbance ceases, and from which the equipment under test recovers its normal performance, without operator intervention. **(Automatic Recovery)**
Class C	Temporary loss of function or degradation of performance, the correction of which requires operator intervention. **(Manual Recovery)**
Class D	Loss of function or degradation of performance which is not recoverable, owing to damage to hardware or software, or loss of data.

In order to meet the rigorous EMS immunity requested by the IC industry, some international test standards have been established, such as IEC 61000-4-2 standard for the system-level ESD test [5], and IEC 61000-4-4 standard for the electrical-fast-transient (EFT) test [6]. During the system-level ESD or EFT tests, the fast electrical transients are coupled to the power, ground, and input/output (IO) pins of the CMOS ICs inside the equipment under test (EUT) to interfere the system operation. Table I shows the evaluation of system-level ESD or EFT test results, which is classified by judging whether the performance of EUT is lost or degraded after the system-level ESD or EFT test. Generally, the microelectronic products have to reset automatically without operator intervention to pass the specification of "Class B."

Traditional solutions to protect microelectronic products against the system-level electrical-transient disturbances are to add some discrete noise-bypassing components or board-level noise filters on the printed circuit board (PCB) [11], [12]. However, the board-level solutions may increase the cost of IC products. In the previous works, some chip-level solutions have been developed to achieve cost efficiency [13]–[16]. It has been proven that an on-chip transient detection circuit co-designed with system operating firmware and power-on reset (POR) circuit can automatically recover the system from the abnormal state after the electrical-transient disturbances to help IC products meet the immunity level of Class B. The transient detection circuit can detect the system-level ESD-generated or EFT-induced transients coupling on the

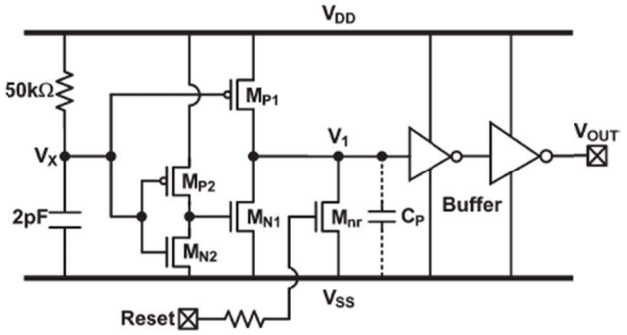


Fig. 1. Previous on-chip transient detection circuit [15].

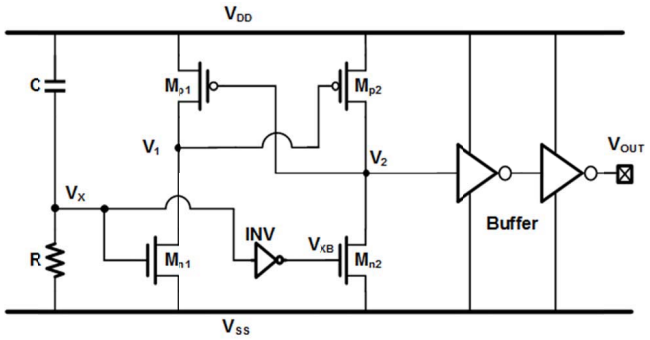


Fig. 2. New proposed on-chip self-reset transient detection circuit.

power/ground lines of CMOS ICs. The output state of the transient detection circuit can be changed from the initial state after the system-level ESD or EFT test. It can be used as the system recovery signal to execute the system recovery procedure.

Fig. 1 shows a previous on-chip transient detection circuit [15]. The device M_{nr} was used to provide an initial voltage level to 0 V at node V_1 and the output node (V_{OUT}) under normal power-on condition. When system recovery was completed, a reset signal was given to release the voltage level at V_{OUT} for detecting the next electrical transients. However, considering the mistriggering from the reset signal or POR circuit during the electrical transients, the detection circuit might lose its function.

A new on-chip self-reset transient detection circuit fabricated in a 0.18-μm CMOS process with 1.8-V devices has been proposed in this work. The proposed transient detection circuit is capable of both detection and self-reset functions to avoid the mistriggering from the reset signal. In addition, the reset time can be adjusted to meet the different requests of system recovery time. The circuit function has been investigated by HSPICE simulation. The system-level ESD gun and the EFT generator are used to evaluate the detection function of the proposed transient detection circuit. The experimental results in a 0.18-μm CMOS process have verified that the proposed transient detection circuit can successfully detect the occurrence of electrical transients during system-level ESD or EFT testing conditions.

II. Self-Reset Transient Detection Circuit

The proposed on-chip self-reset transient detection circuit is designed to detect the occurrence of system-level ESD-generated or EFT-induced positive and negative electrical transients. Under the normal operating condition, the output state (V_{OUT}) of detection circuit is kept at 0 V as logic "0." When the transient disturbance happens, the output state (V_{OUT}) will transit from 0 V to 1.8 V as logic "1" and latch at this state. After a latch time, the voltage level of output state (V_{OUT}) will return to initial state as logic "0" for detecting the next electrical-transient events. Thus, the detection and self-reset functions of the proposed detection circuit can be realized together.

A. Circuit Implementation

The proposed transient detection circuit is shown in Fig. 2. Capacitor C and resistor R are used as the detection part of the circuit. The memory unit of detection circuit comprises two NMOS devices (M_{n1} and M_{n2}), two cross-coupled PMOS devices (M_{p1} and M_{p2}), and an inverter (INV). Another two inverters are designed as the buffer for output signal (V_{OUT}).

Under the normal power-on condition, the voltage level of node V_X is biased at 0 V by the resistor R, and the voltage level of node V_{XB} is biased at 1.8 V through the inverter (INV). At this moment, M_{n1} is turned off, and M_{n2} is turned on to pull down the voltage of node V_2. With the positive feedback device M_{p1}, the voltage level of node V_1 is pulled high to logic "1," and voltage level of node V_2 is finally pulled low to logic "0." Through the buffer with two inverters, the initial output voltage (V_{OUT}) of this proposed transient detection circuit is kept at 0 V. When the system-level ESD or EFT event happens, the transient voltage is coupled to the node V_X through the capacitor C, and the node V_{XB} will be pulled low via the INV. Then the NMOS device M_{n2} will be turned off, and M_{n1} will be turned on to pull down the voltage level of node V_1 to logic "0." The PMOS device M_{p2} acts as the positive feedback to pull up the voltage level of V_2 to logic "1," M_{p1} will finally be turned off. The voltage level of V_{OUT} will transit from 0 V to 1.8 V as logic "1" through the buffer. When the system-level ESD or EFT event ends, the voltage level of node V_X is gradually discharged to 0 V through the resistor R, and then V_{XB} is pulled high to 1.8 V. Then, M_{n1} is turned off and M_{n2} is turned on again. The M_{n2} will pull low the voltage level of node V_2, and the voltage level of node V_1 will be pulled high through the positive feedback device M_{p1}. After a latch time, the output voltage of the proposed transient detection circuit will be changed from 1.8 V to 0 V again. The proposed transient detection circuit can finally reset the voltage level of output signal (V_{OUT}) to its initial state.

As the operation principles of the proposed on-chip self-reset transient detection circuit mentioned above, the M_{n1} and M_{p2} are designed with large device size (W/L) to detect the fast electrical transients effectively. In order to keep the state stored at node V_2 with a requested latch time, the M_{n2} and M_{p1} are designed with small size. Table II shows the device dimensions for this proposed on-chip self-reset transient detection circuit used in the following simulations.

TABLE II
DEVICE DIMENSIONS USED IN THE PROPOSED ON-CHIP TRANSIENT DETECTION CIRCUIT

Device	Width/Length
M_{p1}	1/0.18 (μm)
M_{n1}	6/0.18 (μm)
M_{p2}	6/0.18 (μm)
M_{n2}	1/0.18 (μm)

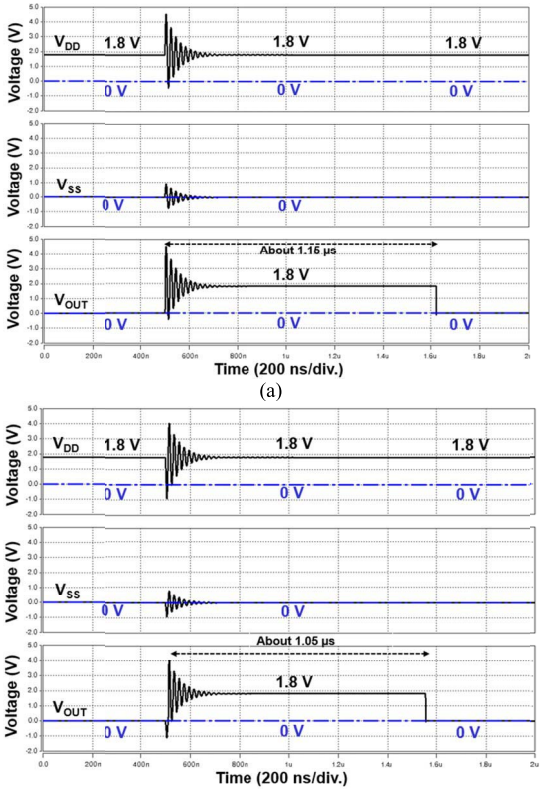


Fig. 3. Simulated V_{DD}, V_{SS}, and V_{OUT} waveforms of the new proposed on-chip self-reset transient detection circuit under system-level ESD tests with (a) positive-going and (b) negative-going underdamped sinusoidal voltages.

B. HSPICE Simulation

1) System-Level ESD Testing Conditions: System-level ESD test is intended to simulate end-user ESD events of microelectronic products in the real world. The IEC 61000-4-2 standard defined by International Electrotechnical Commission (IEC) is the most common test standard for system-level ESD test in industry [5]. According to the previous study [15], an underdamped sinusoidal voltage source with a damping factor parameter is used to simulate system-level ESD-induced electrical transients coupling on power/ground lines in the proposed transient detection circuit. Figs. 3(a) and 3(b) show the simulated V_{DD}, V_{SS}, and V_{OUT} waveforms in HSPICE simulation. The initial dc voltage of 1.8 V (0 V) is set to V_{DD} (V_{SS}) under the normal power-on condition. The positive-going underdamped sinusoidal voltage with applied voltage amplitude (V_a) of +3 V on

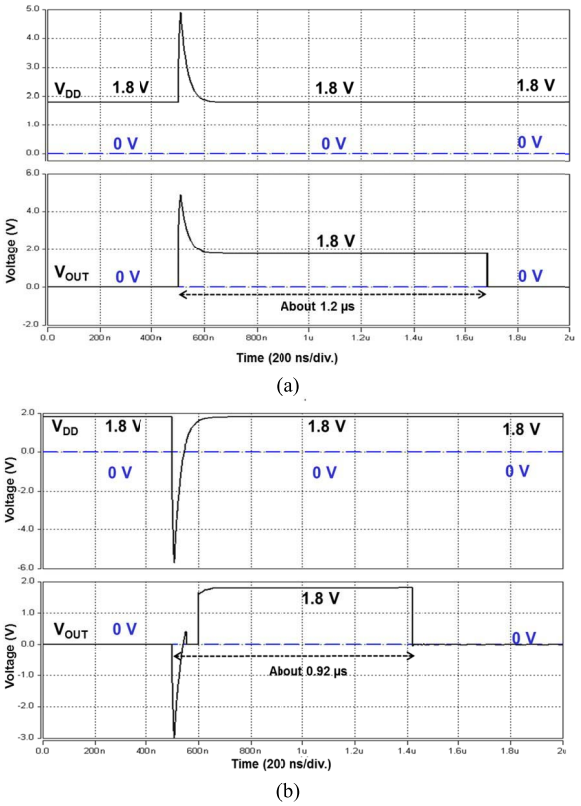


Fig. 4. Simulated V_{DD} and V_{OUT} waveforms of the new proposed on-chip self-reset transient detection circuit under EFT tests with (a) positive and (b) negative exponential voltages pulse coupled to V_{DD}.

V_{DD} and V_a of +1 V on V_{SS} are used to simulate the transient disturbance under positive system-level ESD test. The negative-going underdamped sinusoidal voltage with V_a of −3 V on V_{DD} and V_a of −1 V on V_{SS} are used to simulate the transient disturbance under negative system-level ESD test. From the simulated waveforms, V_{OUT} can simultaneously act with the corresponding positive or negative underdamped sinusoidal voltage waveform. When the system-level ESD event ends, V_{DD} (V_{SS}) returns to 1.8 V (0 V), but V_{OUT} is still latched at 1.8 V. After the latch time of 1.15 μs (1.05 μs) in the positive (negative) system-level ESD test simulation, V_{OUT} is automatically reset to 0 V.

2) EFT Testing Conditions: EFT test is used to simulate the switching transients caused by the interruption of inductive loads such as relays, switch contactors, etc. The test specifications are specified in the IEC 61000-4-4 standard [6]. To simulate the EFT-induced electrical transients under EFT test, an approximated exponential pulse is used in HSPICE simulation [15]. Fig. 4(a) shows the simulated V_{DD} and V_{OUT} waveforms of the proposed transient detection circuit with positive and negative exponential pulse disturbances on V_{DD} line, respectively. When the exponential pulse with an amplitude of +5 V is coupled on V_{DD} line, V_{OUT} acts simultaneously with a positive-going exponential pulse and changes to 1.8 V from initial voltage level of 0 V. After the latch time of ∼1.2 μs, the voltage level of V_{OUT} is automatically reset to 0 V. Fig. 4(b) shows the simulated V_{DD} and

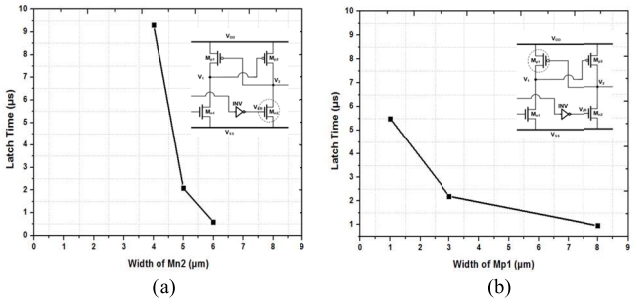


Fig. 5. Relations between latch time and (a) width of M_{n2}, (b) width of M_{p1}. The channel lengths of M_{n2} and M_{p1} are fixed at 0.18 μm.

V_{OUT} waveforms of the proposed transient detection circuit under a negative exponential pulse disturbance with an amplitude of -6 V coupled on V_{DD} line. V_{OUT} acts simultaneously with a negative-going exponential pulse and changes to 1.8 V finally from 0 V. After the latch time of ~0.92 μs, the voltage level of V_{OUT} is automatically reset to 0 V. From the HSPICE simulation results, the output voltage (V_{OUT}) of the proposed transient detection circuit can successfully transit from 0 V to 1.8 V by detecting the occurrence of system-level ESD or EFT events, and then automatically reset to 0 V after a designed latch time. The detection and self-reset functions of the proposed transient detection circuit can be further verified in the silicon chip.

C. Latch Time Control

During the ESD- or EFT-induced transient disturbances, the M_{p2} is turned on to pull high the voltage level at node V_2 in the proposed transient detection circuit, and then changes the output voltage (V_{OUT}) from 0 V to 1.8 V. When the transient disturbance ends, owing to the voltage levels of nodes V_X changed to 0 V and V_{XB} changed to 1.8 V, M_{n1} will be turned off and M_{n2} will be turned on. Then, the voltage level at node V_2 can control the drain current of M_{p1}, which can gradually charge the voltage level at node V_1. Meanwhile, the voltage level at node V_2 will be gradually discharged through device M_{n2}. Finally, node V_1 will be logic "1" and node V_2 will be logic "0." The duration of node V_2 kept at logic "1" is defined as the latch time, which can be adjusted by the drain current of M_{p1}. In order to increase the latch time, M_{p1} should be biased in subthreshold region for greatly reducing its drain current. The drain current of M_{p1} (I_{dp1}) in subthreshold region has the relationship as:

$$I_{d_{p_1}} \propto \frac{W_{p_1}}{L_{p_1}} exp\left(\frac{V_{gs_{p_1}}}{n * V_T}\right) \; where \; V_{gs_{p_1}} = V_2 - V_{DD}. \quad (1)$$

Thus, the latch time can be adjusted with the device dimensions of M_{n2} and M_{p1}. To investigate the latch time, the transistor sizes of the proposed self-reset transient detection circuit are enlarged, as listed in Table III. The relations between latch time and device dimensions of M_{n2} and M_{p1} are shown in Figs. 5(a) and 5(b), respectively. It is observed that the curve of M_{p1} is more linear than that of M_{n2}. Therefore, adjusting the device dimension of M_{p1} can get a better latch time control.

TABLE III
DEVICE DIMENSIONS USED IN THE PROPOSED ON-CHIP TRANSIENT DETECTION CIRCUIT FOR HSPICE SIMULATION OF LATCH TIME

Device	Width/Length
M_{p1}	3/0.18 (μm)
M_{n1}	30/0.18 (μm)
M_{p2}	30/0.18 (μm)
M_{n2}	5/0.18 (μm)

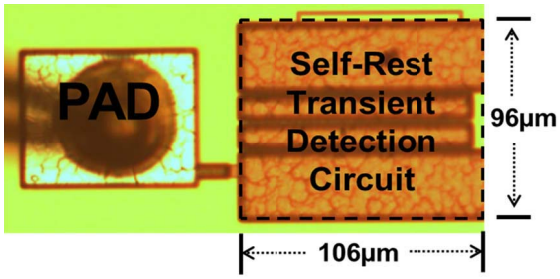


Fig. 6. Die photograph of the new proposed on-chip self-reset transient detection circuit fabricated in a 0.18-μm CMOS process.

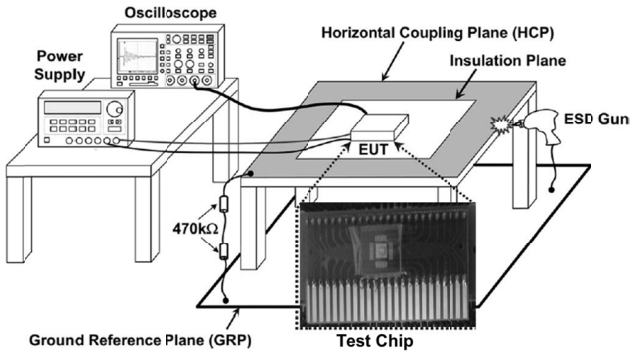


Fig. 7. Measurement setup for a system-level ESD test with indirect contact-discharge test mode [15].

III. EXPERIMENTAL RESULTS

The new on-chip self-reset transient detection circuit has been proposed and fabricated in a 0.18 μm CMOS process with 1.8-V devices. The silicon area of the proposed transient detection circuit is 106μm × 96μm, as shown in Fig. 6.

A. System-Level ESD Test

According to the IEC 61000-4-2 standard, the contact-discharge test mode is used for the system-level ESD test in this work. The contact discharge is applied to the conductive surfaces of the EUT (direct discharge) or to the horizontal or vertical coupling planes (indirect discharge). Fig. 7 shows the measurement setup of the system-level ESD test with indirect contact-discharge test mode. The EUT is put on a wooden table that stands on the ground reference plane (GRP). Insulation plane is used to isolate the EUT from the horizontal coupling plane (HCP) placed on the table. ESD gun is used as the system-level ESD generator. In addition, the discharge return cable of the ESD gun is connected to the GRP directly and the HCP is connected to the GRP with two 470 kΩ resistors in series. When the ESD gun zaps the HCP, the ESD-coupled

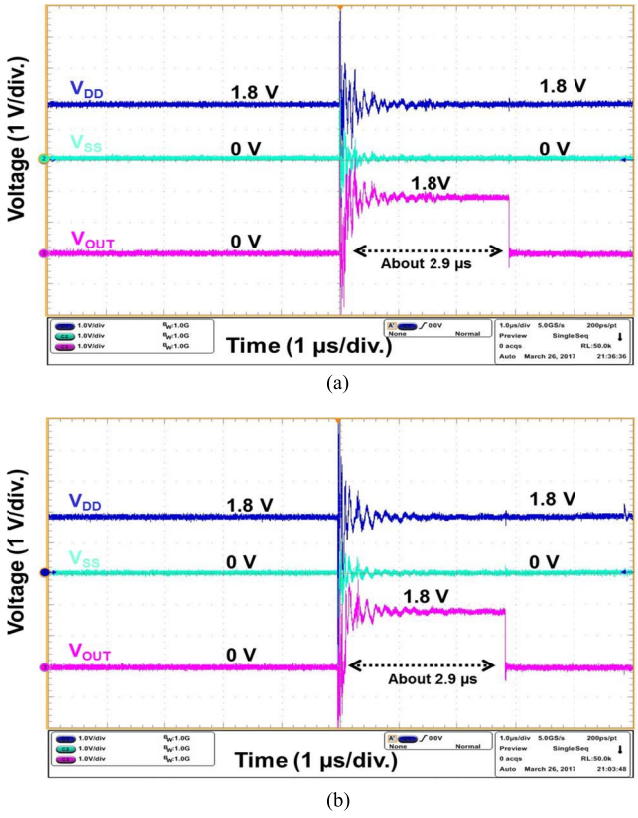


Fig. 8. Measured V_{DD}, V_{SS}, and V_{OUT} waveforms of the new proposed on-chip self-reset transient detection circuit under system-level ESD tests with ESD voltages of (a) +0.2 kV and (b) -0.2 kV.

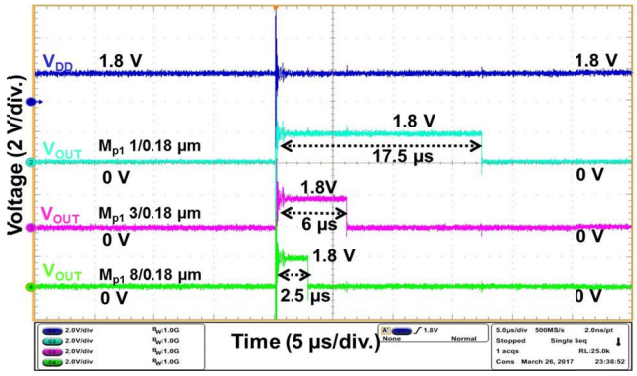


Fig. 9. Measured V_{DD} and V_{OUT} waveforms of the new proposed on-chip self-reset transient detection circuit with different channel widths of M_{p1} under system-level ESD test with an ESD voltage of +300 V.

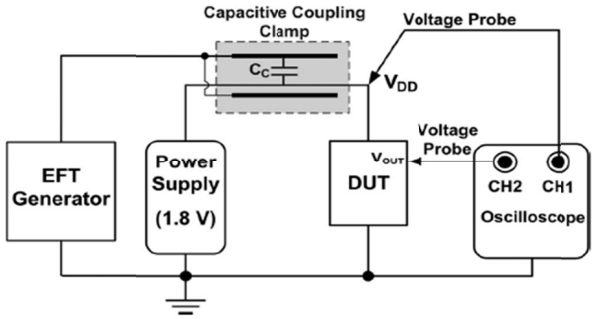


Fig. 10. Measurement setup for an EFT test combined with a capacitive coupling clamp.

electrical transient will disturb the power lines of the CMOS ICs inside the EUT.

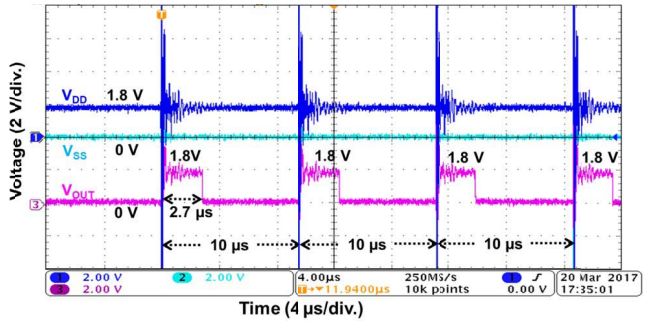
Fig. 8(a) shows the measured V_{DD}, V_{SS}, and V_{OUT} waveforms of the proposed transient detection circuit under system-level ESD test with an ESD voltage of +0.2 kV zapping on the HCP. During the period with ESD-induced electrical-transient disturbance, the normal voltage levels of V_{DD} and V_{SS} are influenced simultaneously. The voltage level of V_{DD} (V_{SS}) rapidly increases from 1.8 V (0 V), and the voltage level of V_{OUT} also increases simultaneously with the appearance of a positive-going underdamped sinusoidal waveform. Finally, the output voltage (V_{OUT}) of the proposed transient detection circuit transits from 0 V to 1.8 V and keeps at 1.8 V with a latch time of ~2.9 μs. Therefore, the proposed transient detection circuit can sense the positive-going electrical transient on the power lines and reset the output voltage (V_{OUT}) level to its initial state.

Fig. 8(b) shows the measured V_{DD}, V_{SS}, and V_{OUT} waveforms of the proposed transient detection circuit under system-level ESD test with an ESD voltage of -0.2 kV. During the ESD-induced electrical-transient disturbance, the voltage level of V_{DD} (V_{SS}) rapidly decreases from 1.8 V (0 V), and the voltage level of V_{OUT} is disturbed simultaneously. Finally, the output voltage (V_{OUT}) of the proposed transient detection circuit transits from 0 V to 1.8 V and keeps at 1.8 V with a latch time of ~2.9 μs. Thus, the detection and self-reset functions of the proposed transient detection circuit have been verified by the experimental results in silicon chip and HSPICE simulation.

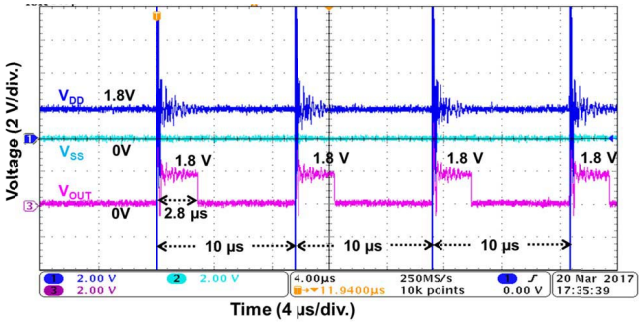
Fig. 9 shows the measured V_{OUT} waveforms with different latch times under system-level ESD test with an ESD voltage of +300 V. Other devices' dimensions in the proposed transient detection circuit are as the values listed in Table III. The duration of V_{OUT} voltage kept at 1.8V is increased from 2.5 to 17.5 μs when the channel width of M_{p1} decreases from 8 to 1 μm. Verified by the measured waveforms, the latch time is inversely proportional to the channel width of M_{p1}.

B. EFT Test

Fig. 10 shows the measurement setup for an EFT test combined with a capacitive coupling clamp. The output of EFT generator is directly connected to the capacitive coupling clamp, which provides the ability of coupling the fast transients and bursts to the circuit under test without any galvanic connection. The cables from the power supply equipment are placed inside the capacitive coupling clamp. The typical capacitance between the cable and clamp ranges from 50 to 200 pF. To provide maximum coupling capacitance between the cable and clamp, the EFT generator is connected to the end of clamp that is nearest to the EUT. Thus, the EFT voltage can be coupled to the power cable via the capacitor of capacitive coupling clamp. The digital oscilloscope can monitor the voltage responses of V_{DD}, V_{SS}, and V_{OUT} of the proposed transient detection circuit under EFT test.



(a)



(b)

Fig. 11. Measured V_{DD}, V_{SS}, and V_{OUT} waveforms of the new proposed on-chip self-reset transient detection circuit under EFT tests with EFT voltage of (a) +0.2 kV and (b) -0.2 kV. The repetition rates are 100 kHz.

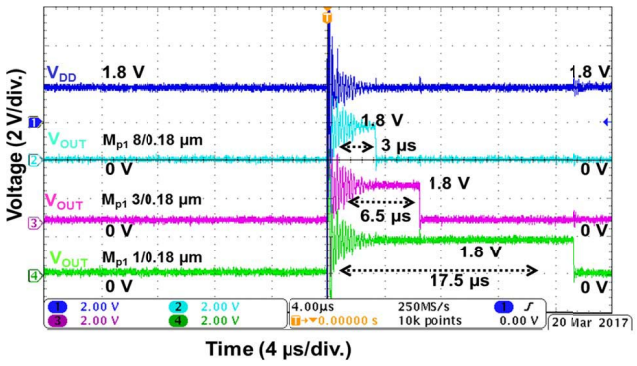


Fig. 12. Measured V_{DD} and V_{OUT} waveforms of the new proposed on-chip self-reset transient detection circuit with different channel widths of M_{p1} under EFT test with an EFT voltage of +300 V.

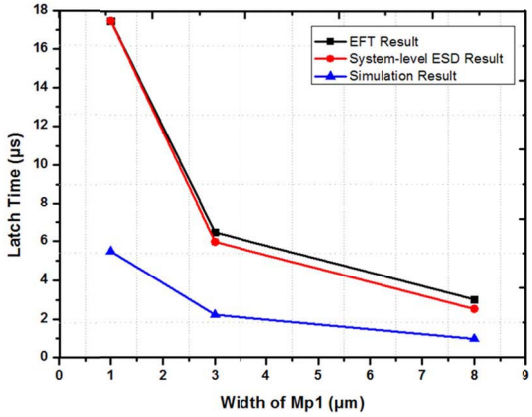


Fig. 13. Relations between the different channel widths of M_{p1} and the latch times under system-level ESD, EFT tests, and HSPICE simulation.

Fig. 11(a) shows the V_{DD}, V_{SS}, and V_{OUT} waveforms under EFT test with an EFT voltage of +200 V and a repetition rate of 100 kHz. The period of the EFT pulses is 10 µs. During the EFT test, V_{OUT} is influenced simultaneously with positive-going underdamped sinusoidal voltage coupled to the V_{DD} and V_{SS} lines. In each EFT pulse, the voltage level of V_{OUT} transits from 0 V to 1.8 V, and then returns to 0 V after a latch time of 2.7 µs, for detecting the next EFT pulse.

Fig. 11(b) shows the V_{DD}, V_{SS}, and V_{OUT} waveforms under EFT test with an EFT voltage of -200 V and a repetition rate of 100 kHz. During the EFT test, V_{OUT} is influenced simultaneously with negative-going underdamped sinusoidal voltage coupled to the V_{DD} and V_{SS} lines. In each EFT pulse, the voltage level of V_{OUT} transits from 0 V to 1.8 V, and then returns to 0 V after a latch time of 2.8 µs, for detecting the next EFT pulse.

Fig. 12 shows the measured V_{OUT} waveforms with different latch times under EFT test with EFT voltage of +300 V during a single pulse. The channel widths of M_{p1} are designed with 1, 3, and 8 µm, respectively, to control the latch time. Other devices' dimensions in the proposed transient detection circuit are as the values listed in Table III. The duration of V_{OUT} voltage kept at 1.8V is increased from 3 to 17.5 µs when the channel width of M_{p1} decreases from 8 to 1 µm. Verified by the measured waveforms, the latch time is inversely proportional to the channel width of M_{p1}.

C. Discussion

From the measurement results under system-level ESD or EFT tests, the measured latch times in these two test results are almost the same. However, these latch times are much larger than those from HSPICE simulation results. Fig. 13 shows the relations between the channel width of M_{p1} and the latch time under the system-level ESD, EFT tests, and HSPICE simulation conditions. The reason causing such latch time difference is that the real electrical-transient disturbances coupled into CMOS IC under system-level ESD or EFT tests are more complicated than those in HSPICE simulation results.

The real transient disturbance coupled on the power lines is not an ideal underdamped sinusoidal voltage. The duration and amplitude of the transient disturbance could be much larger than the simulation case. Due to the transient disturbance with higher amplitude, the voltage level of node V_2 in Fig. 2 will be overshooting to a higher value that causing a longer latch time. Furthermore, the latch time is highly related to the current capacity of the latching device (M_{p1}) in its subthreshold region. Unfortunately, there should be some deviation of the subthreshold current between the fabricated chip and simulation circuit, which causes the difference of latch time between experimental measurement and simulation results.

D. System Application

To perform the system recovery when the ESD- or EFT-induced electrical transients happen, the detection result from the proposed transient detection circuit can be used as a system

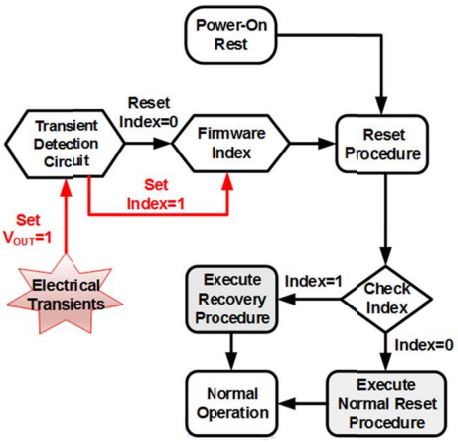


Fig. 14. Firmware flowchart combined with the self-reset transient detection circuit to recover system when electrical transients happen.

recover index for firmware check. For example, the output state (V_{OUT}) of the proposed transient detection circuit is initially set as logic "0" under normal power-on condition. The index of system is set to logic "0" by the V_{OUT} state. When electrical-transient disturbance happens, the proposed transient detection circuit can detect the occurrence of electrical-transient disturbance and transit the V_{OUT} state from logic "0" to logic "1." At this moment, the firmware index is also changed to logic "1" by V_{OUT} state and then initiates the firmware recovery procedure to restore the system to a known stable state. After the recovery procedure, the transient detection circuit will reset V_{OUT} state to logic "0" by itself, and then reset the firmware index to logic "0" again. Fig. 14 shows the firmware recovery flowchart combined with the transient detection circuit.

In this flowchart, the firmware index can be only set by the output state (V_{OUT}) of self-reset transient detection circuit. There is no need to add a reset data path from the power-on reset (POR) circuit to the transient detection circuit in this firmware flowchart. Whether or not the reset data path or POR circuit is mistriggered under electrical-transient disturbance, the system recovery procedure can be still initiated to rescue the system from the abnormal condition. Therefore, the solution of firmware combined with the on-chip self-reset transient detection circuit can provide a more efficient protection for the microelectronic products against the electrical transients.

IV. Discussion

The time constant of RC timer in the proposed transient detection circuit is typically designed in the order of microseconds to distinguish the transition of ESD pulse in the order of nanoseconds from the power-on transition of milliseconds. Therefore, the time constant of RC timer can't be shrunk to further reduce the layout area of proposed transient detection circuit. However, there were some previous works [17]–[19] reported to detect ESD transient with circuit skill of current mirror to reduce the device size of RC timer. Such modified designs on the RC circuits may be applied to further reduce the device size of RC timer in this proposed transient detection circuit. In addition, there is power-rail ESD clamp circuit in the IC products to meet the chip-level ESD specification, which was often realized with the CR-inverters-NMOS structure [20]. With the power-rail ESD clamp circuit and self-reset transient detection circuit integrated in a chip, the same RC timer circuit can be used to provide both of the transient disturbance detection and power-rail ESD clamp circuit to further save the total layout area.

V. Conclusion

A new on-chip self-reset transient detection circuit has been proposed and successfully verified in a 0.18-μm CMOS process. The detection sensitivity and self-reset function of the proposed on-chip self-reset circuit have been investigated by HSPICE simulation and confirmed by the experiment results under system-level ESD and EFT tests. Compared with the previous designs, the new proposed transient detection circuit is capable of both the detection and self-reset functions without additional devices for the reset function. In addition, the reset time of the proposed transient detection circuit can be adjusted to meet the different requests of system recovery time in microelectronic products. With firmware co-design, the proposed on-chip self-reset transient detection circuit can provide an on-chip solution to enhance the immunity level of microelectronic products equipped with CMOS ICs effectively against the system-level electrical-transient disturbance.

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