A High-Voltage-Tolerant and Power-Efficient Stimulator With Adaptive Power Supply Realized in Low-Voltage CMOS Process for Implantable Biomedical Applications

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***Abstract*— A high-voltage-tolerant and power-efficient stimulator with adaptive power supply is proposed and realized in a 0.18-μm 1.8-V/3.3-V CMOS process. The self-adaption bias technique and stacked MOS configuration are used to prevent issues of electrical overstress and gate-oxide reliability in low-voltage transistors. The on-chip high-voltage generator uses a pulse-skip regulation scheme to generate a variable dc supply voltage for the stimulator by detecting the headroom voltage on the electrode sites. With a dc input voltage of 3.3 V, the on-chip high-voltage generator provides an adjustable dc output voltage from 6.7 to 12.3 V at a step of 0.8 V, which results in a maximal system power efficiency of 56% at a 2400-μA stimulus current. The charge mismatch of the stimulator is down to 1.7% in the whole stimulus current range of 200–3000 μA. The in vivo experiments verified that epileptic seizures could be suppressed by the electrical stimulation provided by the proposed stimulator. In addition, the reliability measurements verified that the proposed stimulator is robust for electrical stimulation in medical applications.**

***Index Terms*— Epileptic seizure suppression, charge balance, charge pump, power efficiency, high-voltage-tolerant, stimulator.**

I. Introduction

EPILEPSY is a group of neurological disorders resulting from excessive and abnormal discharges in the brain. People suffering from epilepsy may experience aimless movements, uncontrolled body movements, and a loss of awareness. Most epilepsy patients can be cured by the antiepileptic drugs (AEDs). However, approximately 30% of patients suffer from medically refractory epilepsy [1]. Patients who have suffered from focal seizures with a clearly identified epileptogenic zone can benefit from epilepsy brain surgery. There are different types of brain surgeries such as temporal lobectomy, lesionectomy, extra temporal resection, and hemispherectomy. However, resection surgery is a non-reversible treatment that may exhibit high risks such as the loss of physical functions.

New therapies of treating seizures are being vigorously pursued. There are three different electric stimulation therapies that can prevent or stop seizures, such as vagus nerve stimulation (VNS) therapy, responsive neurostimulation (RNS) therapy, and deep brain stimulation (DBS) therapy. VNS therapy is designed to control epileptic seizures by sending regular, mild pulses of electrical energy to the brain by stimulating the left vagus nerve in the neck. In 2000, a large prospective study of VNS was reported by DeGiorgio [2]. This study involved 195 patients over a 15-month period at 20 medical centers. At 12 months, the reduction in seizure frequency was 45%. RNS is another therapy to control partial onset seizures which are not controlled with medication. The stimulator is placed under the scalp and within the skull. One or two leads are then placed at the seizure target and connected to the stimulator. RNS system can automatically monitor brain signals and provide stimulation to abnormal electrical events just when it is needed. Under the sponsorship of NeuroPace, a randomized, placebo-controlled, double-blind, multicenter clinical study in 191 patients was reported by Morrell in 2011 [3]. The stimulators were placed approximately over the seizure focus in 191 patients. Clinical trials showed that 38% improvement in stimulated group versus 17% in sham-stimulated group.

DBS therapy is a fairly new treatment for epilepsy and is being researched. A deep brain stimulator system (one product of Medtronic) consists of stimulator, extension wire, and lead. Stimulator is a programmable pacemaker device which creates electric pulses. Lead is a coated wire which delivers electric pulses to the brain tissue. There are a number of electrodes at the tip of the lead. Extension wire is an insulated wire that connects the lead to the stimulator. DBS therapy has several advantages over brain surgery. Firstly, DBS therapy is not always necessary to know the precise location of the seizure focus. Secondly, DBS therapy is relatively noninvasive because it is no required removal of brain tissue. Thirdly, DBS therapy is reversible with cessation of stimulation or removal of the stimulator devices. Finally, the stimulation parameters of DBS system are adjustable. Overall, DBS therapy is flexible

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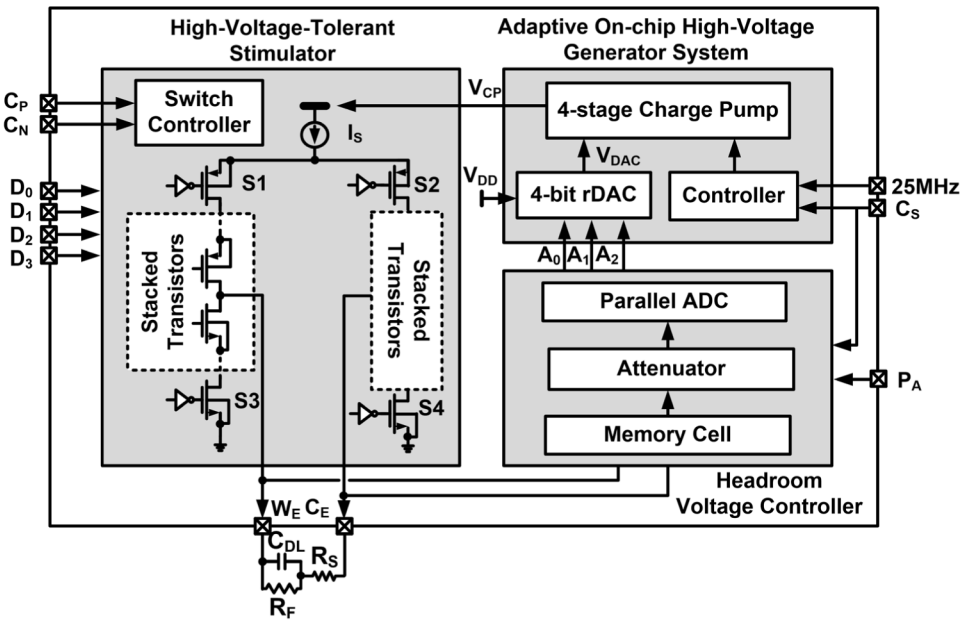


Fig. 1. The overall architecture of the proposed stimulator with adaptive supply control in the LV CMOS process. The rising edge of C_S starts the charge pump, and the rising edge of P_A starts the power supply self-adjusting operation. D_0 to D_3 control the magnitude of the stimulus current. C_P and C_N control the switches of the stimulator. C_{DL}, R_F and R_S represent the double-layer capacitance, the faradaic charge transfer, and the solution impedance, respectively. In addition, C_{DL}, R_F and R_S are assumed as 500nF, 10MΩ, and 4kΩ, respectively.

and recoverable. Under the sponsorship of Medtronic, a large, randomized, and controlled clinical study in 110 patients was reported by Fisher in 2010 [4]. The stimulation site is Anterior Nucleus of the Thalamus (ANT). Clinical trials showed that seizures were reduced 40% in stimulated group versus 15% in placebo group. Overall, Clinical trials have verified that DBS is helpful for some people whose epilepsy is difficult to be cured, and who cannot have brain surgery to remove or separate the part of the brain that is thought to cause seizures to happen.

A closed-loop DBS system that continuously monitors the brain's activity is an ongoing engineering technology [5]–[7]. However, a circuit designer faces a number of challenges while designing a stimulator, such as the realization of high-level integration (to reduce the size of the implanted devices) and the reduction of medical costs. In [7], a fully integrated closed-loop DBS system for controlling epileptic seizures was developed in a low-voltage (LV) CMOS process. It consisted of analogue front-end amplifiers, an ADC, a bio-signal processor and an electrical stimulator in the LV CMOS process. The LV CMOS process has long been a popular choice to realize a system on a chip (SoC) for enhancing integration and reducing cost. The electrical stimulator is an exception because the required supply voltage of a stimulator is typically much higher than that of the LV CMOS process. A high operating voltage may damage the transistors in an LV CMOS process. Therefore, one approach is to use the high-voltage (HV) process to design the stimulator [8]–[13]. However, the HV devices should be manufactured by using a standard CMOS process with some special layout techniques and HV layers. The size and cost of the implanted stimulator are disadvantageously increased. In addition, studies have reported high-voltage-tolerant stimulators realized in LV CMOS processes [7], [14], [19]. One of the advantages of this approach is that the neuro-stimulator can be fully integrated with the microcontroller or biomedical signal processor into an SoC fabricated using a digital technology for enhancing integration and reducing the cost.

The effective loading impedance to the stimulator will significantly vary in vivo because of the locations, distances, and the implantation time of the electrodes [15]–[18]. Therefore, we need a stimulator which is adaptable to loading impedance. The adaptive supply control technique is an effective method to load the varied impedance. When the stimulator delivers charges to the electrode, the supply voltage can be automatically adjusted depending on the loading impedance; this will ensure that the transistors in the current generator have enough voltage headroom to stay saturated. In [14], a precise charge-balanced and high-voltage-tolerant neuro-stimulator had been designed and successfully verified in a LV CMOS process. However, the stimulator was inadaptable to the loading impedance.

In this study, we propose a stimulator with a self-adaption bias circuit and loading impedance adaptability to withstand four times the nominal supply voltage ($4\times V_{DD}$) without compromising on device reliability. The HV generator of the stimulator uses a pulse-skip regulation scheme to achieve high power efficiency. The stimulator chip has been fabricated in a 0.18-μm 1.8-V/3.3-V CMOS process and successfully verified using animal tests.

II. Circuit Implementation

Fig. 1 depicts the overall architecture of the proposed stimulator with adaptive supply control in an LV CMOS process.

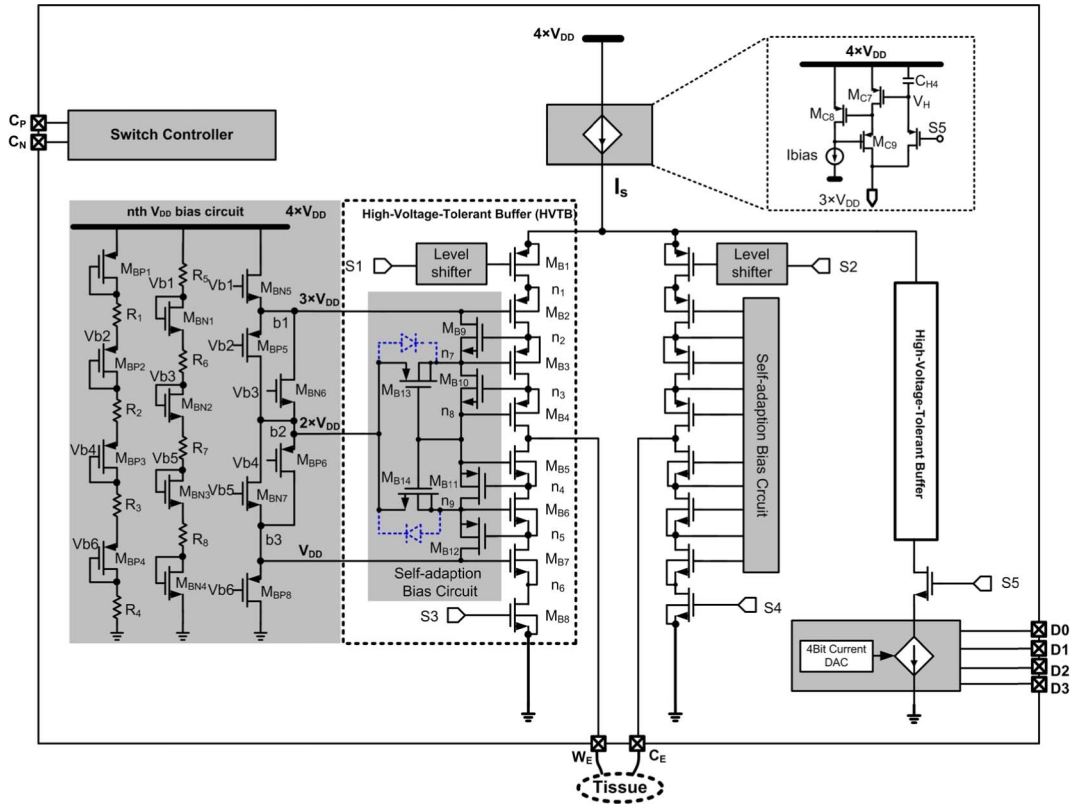


Fig. 2. The detailed schematic of the proposed high-voltage-tolerant and charge balanced stimulator.

It consists of a high-voltage-tolerant stimulator, an adaptive on-chip high-voltage generator system (AHGS) and a headroom voltage controller (HVC). The HVC consists of a capacitive voltage divider and an ADC [1]. The stimulator is designed to generate biphasic current pulses, which include the cathodic current pulse and anodic current pulse. An interphase interval is interposed within the two phases of the biphasic pulses. The HVC is activated in the interphase interval. The output swing of the stimulator is firstly reduced by the capacitive voltage divider, and then digitized by using the ADC. After the HVC is activated, it will detect the headroom voltage of the stimulator and then generate the control signals (A_0, A_1 and A_2) to adjust the stimulator supply. In the proposed system, the supply voltage of the stimulator can be adjusted to the lowest level without degrading the charge balance performance. This mechanism is aimed to minimize the voltage drop across I_S and the stacked transistors of the stimulator; this will maximize the overall efficiency of the stimulator and reduce the thermal rise in the chip.

A. High-Voltage-Tolerant and Charge Balanced Stimulator

The proposed stimulator uses stacked transistors to withstand the high power supply voltage. If *n* transistors are stacked, it can withstand *n* times the nominal supply voltage ($n \times V_{DD}$) without degrading the transistor reliability. Previous studies have reported $2 \times V_{DD}$-tolerant buffers, $3 \times V_{DD}$-tolerant buffers and $5 \times V_{DD}$-tolerant buffers and verified them successfully in the LV CMOS process [20], [21]. Fig. 2 depicts the detailed schematic of the proposed high-voltage-tolerant and charge-balanced stimulator, which is realized with the 3.3-V PMOS and NMOS transistors with a deep n-well layer. It consists of a high-voltage-tolerant buffer (HVTB), a high-voltage-tolerant level shifter, a current source (I_S), and a four-bit current DAC.

The $4 \times V_{DD}$ HVTB with the nth V_{DD} bias circuit is depicted on the left of Fig. 2. Transistors (M_{BN5} and M_{BP5}) perform the function of the push-pull stage. The voltages at the nodes b_1, b_2, and b_3 are set as $3 \times V_{DD}$, $2 \times V_{DD}$, and V_{DD}, respectively. The output stage consists of four stacked transistors for the pull-up switch and the pull-down switch, respectively. A self-adaption bias circuit is designed to keep the voltages across the terminals of the stacked transistors within the safe voltage range of $1 \times V_{DD}$ during the operation. The bodies of transistors (M_{B13} and M_{B14}) are connected to the nodes (n_7 and n_9), respectively. The level shifter converts the low-level voltage to high-level voltage with the DC offset of $3 \times V_{DD}$. A non-overlap clock circuit is designed to drive the level shifter for avoiding the short-circuit current in the high-voltage-tolerant buffer.

Transistors (M_{C7}, M_{C8}, and M_{C9}), the capacitor (C_{H4}), and the switch (S5) form the basic current memory cell (I_S), which is a sample-and-hold circuit. When the switch S5 is turned on, the output current (I_{DAC}) of the four-bit current DAC is sampled to the memory capacitor (C_{H4}). When the switch S5 is turned off, the current I_{DAC} is copied to the output current of I_S.

The stimulator is designed to generate biphasic current pulses with an interphase delay. After a one-cycle biphasic

stimulation is finished, the anodic and cathodic electrodes are short-circuited to the ground.

Compared to the high-voltage-tolerant stimulators described in [7] and [19], one of the main advantages of the proposed stimulator is that the proposed high-voltage-tolerant stimulator can withstand continuous exposure to the $4\times V_{DD}$ square waveforms without degradation when the outer transistors (M_{B1} and M_{B8}) are turned off. The $4\times V_{DD}$ square waveforms may be generated on the inactive electrodes in a multi-channel stimulator, because the charge may transfer from the active electrodes to the inactive electrodes through tissues. Let us assume that the initial-voltage on the output port is $4\times V_{DD}$. Then, the previous state of the quiescent voltages at the nodes n_1, n_2, n_3, n_4, n_5, n_6, n_7, n_8 and n_9 will be $4\times V_{DD}$, $4\times V_{DD}$, $4\times V_{DD}$, $3\times V_{DD}$, $2\times V_{DD}$, V_{DD}, $3\times V_{DD}$, $3\times V_{DD}$, and $2\times V_{DD}$, respectively. When the square voltage waveform goes from $4\times V_{DD}$ to 0 V on the output port W_E, the circuit operates in four phases. In phase 1, the node W_E is discharged from $4\times V_{DD}$ to $3\times V_{DD}$. Consequently, the transistor M_{B2} is turned off and the nodes n_1, n_2 and n_3 are finally charged to $3\times V_{DD}$. In phase 2, the node W_E is discharged from $3\times V_{DD}$ to $2\times V_{DD}$. The voltages at the nodes W_E, n_2, n_3, n_4, n_7 and n_8 decrease. When the voltage at n_8 decreases to $2 \times$ VDD, the transistor M_{B13} turns on, and the transistor M_{B14} turns off. Therefore, n_7 is charged to $2\times V_{DD}$ through the transistor M_{B13}. Subsequently, the transistor M_{B3} is turned off, and the node n_2 is finally discharged to $2\times V_{DD}$. As a result, the node n_4 is discharged to $2\times V_{DD}$. In phase 3, the node W_E is discharged from $2\times V_{DD}$ to V_{DD}. The voltages at the nodes W_E, n_3, n_4, n_5 and n_9 decrease, and the transistor M_{B4} is turned off. Finally, the nodes n_3, n_4, n_5, n_8 and n_9 are charged to V_{DD}. In phase 4, the node W_E is charged from V_{DD} to 0 V. The nodes n_4, n_5 and n_6 are charged to 0 V. In the whole transition process, the voltages across the terminals of the stacked transistors are kept within the safe voltage range of $1\times V_{DD}$.

B. Adaptive On-Chip High-Voltage Generator System

The AHGS of the stimulator uses a pulse-skip regulation scheme to achieve high power efficiency [22]. The overall architecture is depicted in Fig. 3(a). It consists of a four-stage charge pump, a four-phase clock generator, a comparator, a four-bit resistor DAC (rDAC), and an on-chip loading capacitor (C). The 4-bit rDAC provides a variable reference voltage based on the input control bits (A_0, A_1, A_2, and A_3), where A_3 is connected to V_{DD}. The comparator is used to detect the output voltage (V_{CP}) of the charge pump by the resistive voltage divider. When $V_D > V_R$, C_{EN} is set to low to stop the clock C_{CP}, where V_R is the output voltage of the four-bit rDAC, V_D is provided by the resistive divider. Otherwise, C_{EN} would be high. The four-phase clock generator is used to generate the non-overlap clock to reduce the reversion and switching losses of the charge pump. When the control signal C_S goes from low to high, AHGS begins to work.

High power efficiency is a critical factor for charge pumps. The various sources of power loss in the charge pump are the redistribution loss, conduction loss, switching loss, and reversion loss [22], [23]. All kind of power loss should be minimized for designing a high-efficiency charge pump.

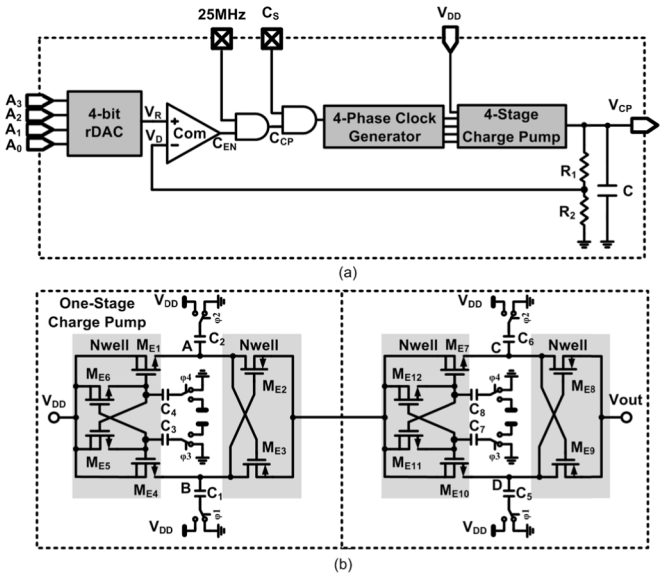


Fig. 3. (a) The overall architecture of the high voltage generator A_3 is connected to V_{DD}. (b) The detailed schematic of the two-stage charge pump. The pumping capacitors (C_1, C_2, C_5, and C_6) are realized with 100-pF MIM capacitors.

The regulated charge pump consists of the four-stage charge pump in an LV CMOS process. Each of the stages is implemented as a four-phase voltage doubler (FPVD). Fig. 3(b) illustrates an example of the two-stage charge pump. The separated capacitor pairs (C_1 and C_2) and (C_3 and C_4) are used to make the FPVD reduce the conduction loss. A voltage doubler cell (M_{E5} and M_{E6}) is used to separate the gate drive for the NMOS switches (M_{E1} and M_{E4}) from that for the PMOS switches (M_{E2} and M_{E3}). By doing this, the reverse currents are eliminated. The bulk terminals of the devices are connected to the respective sources and the body terminals.

Fig. 4(a) depicts the timing diagram for the four-stage charge pump $\varphi 1$, $\varphi 2$, $\varphi 3$, and $\varphi 4$. Fig. 4(b) depicts the detailed schematic of the four-phase clock generator. The operation of the charge pump can be explained as follows. First, let us consider the case when the clock signals $\varphi 1 = 0$, $\varphi 2 = 1$, $\varphi 3 = 1$, and $\varphi 4 = 0$. In this scenario, transistors (M_{E1}, M_{E3}, M_{E7}, and M_{E9}) are turned off, and transistors (M_{E2}, M_{E4}, M_{E8}, and M_{E10}) are turned on. Thus, the nodes B, A, D, and C are charged to V_{DD}, $2\times V_{DD}$, $2\times V_{DD}$, and $3\times V_{DD}$, respectively. Second, let us consider the case when the clock signal $\varphi 3$ goes from high to low as shown in Fig. 4(a). In this scenario, transistors (M_{E5}, M_{E6}, M_{E11}, and M_{E12}) are turned off. Therefore, no charge flows from the current stage back to the previous stage. By doing this, the reversion loss of the charge pump is eliminated. Third, let us consider the case when the clock signal N1 goes from high to low. In this scenario, the voltage at node N3 increases to high, as a result, one end of each of the capacitors (C_1, C_2, C_5, and C_6) is hung up, and the transmission gate between $\varphi 1$ and $\varphi 2$ is

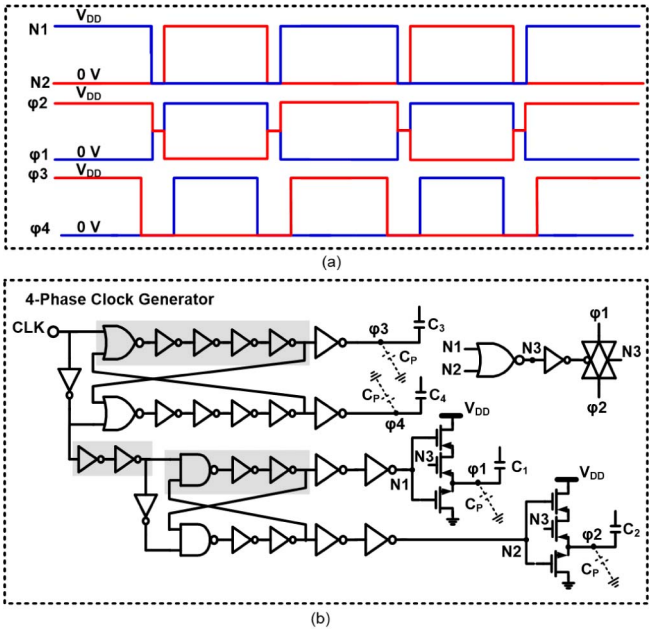


Fig. 4. (a) The timing diagram for the four-stage charge pump. (b) The detailed schematic of the four-phase clock generator.

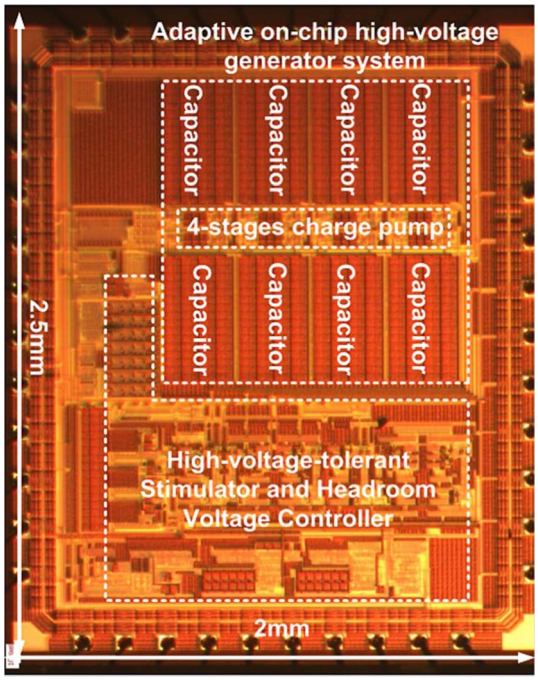


Fig. 5. Photo of the fabricated fully integrated stimulator with adaptive power supply. The silicon area is 5 mm^2.

turned on. The voltage at the node $\varphi 1$ equals the voltage at the node $\varphi 2$, the charges on the parasitic capacitance of capacitors (C_1, C_2, C_5, and C_6) are equalized. By doing this, the parasitic capacitance losses (or switching losses) are cut by ~50%. Fourth, let us consider the case when the clock signal N2 goes from low to high. In this scenario, the node A is discharged to V_{DD}, and the node B is charged to $2\times V_{DD}$. In addition, transistors M_{E3} and M_{E9} are turned on. Finally, consider the case when the clock signal $\varphi 4$ goes from low to high. In this scenario, transistors M_{E1} and M_{E7} are turned on. The nodes C and D are charged to $2\times V_{DD}$ and $3\times V_{DD}$, respectively.

III. Experimental Results

The stimulator chip was fabricated in a 0.18-μm 1.8-V/3.3-V CMOS process. The die photo is shown in Fig. 5. The control signals are generated by the off-chip FPGA (Spartan-3 XC3S400) from Xilinx. AHGS is supplied by B2902A, which is a precise source and measure unit from Agilent; V_{DD} is 3.3 V. The voltages are measured by the oscilloscope (MSO5104) from Tektronix.

A. Adaptive On-Chip High-Voltage Generator System

Fig. 6 depicts the measured output voltage of AHGS using the pulse-skip regulation scheme. Once AHGS is activated, AHGS generates a 12.3-V output voltage with a rising time of ~1 μs. First, the stimulator begins with cathodic stimulation under 12.3 V. During the interphase delay stage, the power supply self-adjusting operation starts (i.e. HVC is activated). Therefore, the output voltage of AHGS is quickly adjusted to the lowest level. Then, the stimulator starts an anodic stimulation. Fig. 6 provides the zoomed in view of the output voltage in the off-state stage (the stimulator stops stimulation).

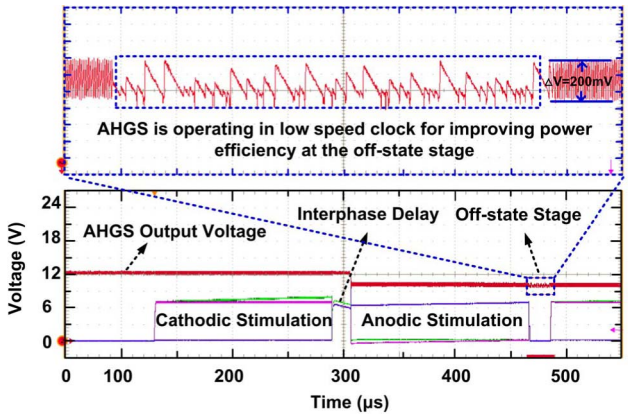


Fig. 6. The measured output voltage of AHGS using the pulse-skip regulation scheme. In the off-state stage, the stimulator stops stimulation; therefore, AHGS operates at low clock speed for improving power efficiency.

The figure illustrates that AHGS is operating in the low-speed clock. In this way, power efficiency is improved because AHGS provides only small bias currents for the stimulator in the off-state stage.

B. Power Efficiency and Charge Mismatch

Power efficiency (η_{eff}) is calculated by multiplying the stimulus current by the supply voltage of the stimulator and dividing the result by the overall power consumed by the stimulator. Fig. 7 compares the output voltages of AHGS and the overall power efficiency of the stimulation system against the stimulus current graphs between the adaptive and the fixed supplies when R_S is 4 kΩ and C_{DL} is 500 nF. In Fig. 7(a), the adaptive supply was measured against the stimulus current

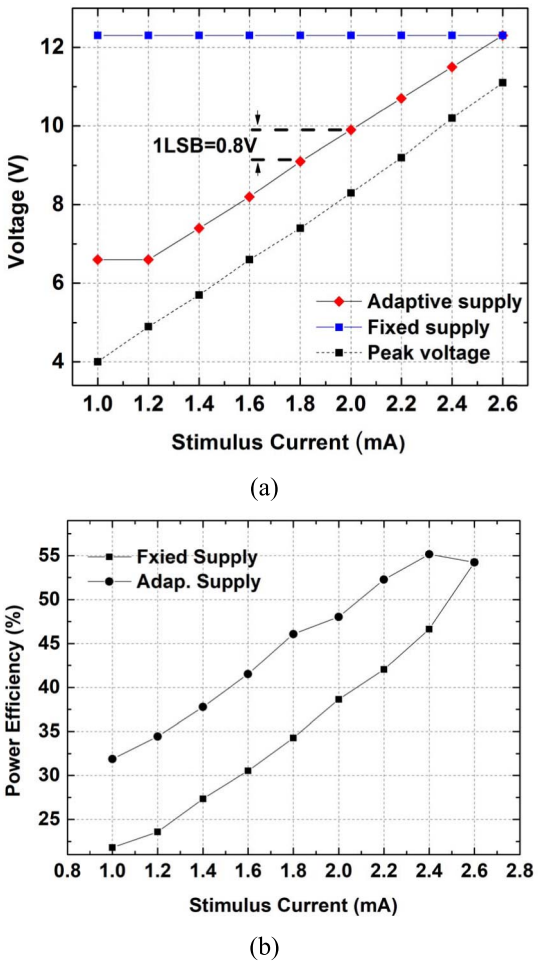


Fig. 7. (a) The output voltage of AHGS of stimulation system vs. stimulus currents between adaptive and fixed supplies when R_S is 4 kΩ and C_{DL} is 500 nF. (b) The power efficiency of stimulation system vs. stimulus currents between adaptive and fixed supplies when R_S is 4 kΩ and C_{DL} is 500 nF.

at 0.8 V increments between 6.7 and 12.3 V. Fig. 7(b) compares the power efficiencies of the stimulation system against the stimulus current between the fixed and adaptive mechanisms. The results show that the stimulation system power efficiency with the adaptive supply control (32% ∼ 55%) is higher than that of the fixed supply (21% ∼ 46%) under 4-kΩ R_S and 500-nF C_{DL}. It can be clearly seen that power efficiency is improved by using this proposed system.

Fig. 8(a) depicts an oscilloscope capture of the residual voltage on the 500-nF Teflon capacitor at 2400-μA stimulus current. Both electrodes are short-circuited to the ground once after every 100 cycles of the biphasic stimulation for ensuring precision in measurements. The accumulated residual voltage at the end of the 100th biphasic stimulation under the fixed 12.3-V power supply is 149.2 mV. Thus, the residual voltage of one-cycle biphasic stimulation is 1.492 mV. The charge mismatch is defined as the charge error divided by the injected charge in the one-cycle biphasic stimulation. Thus, the charge mismatch is 0.745 nC/384 nC = 0.2%. Fig. 8(b) compares the residual voltage on the loading capacitor C_{DL} and the charge mismatch against the stimulus current between the fixed and the adaptive mechanisms.

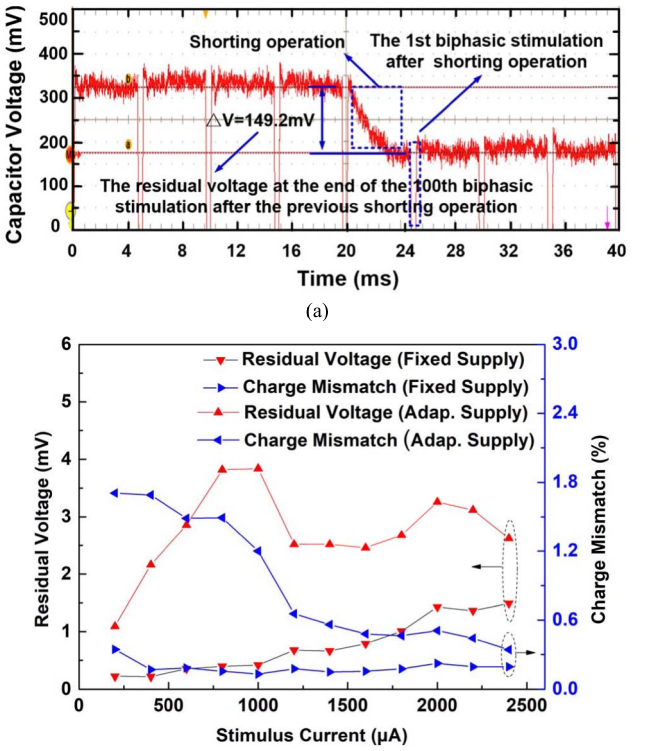
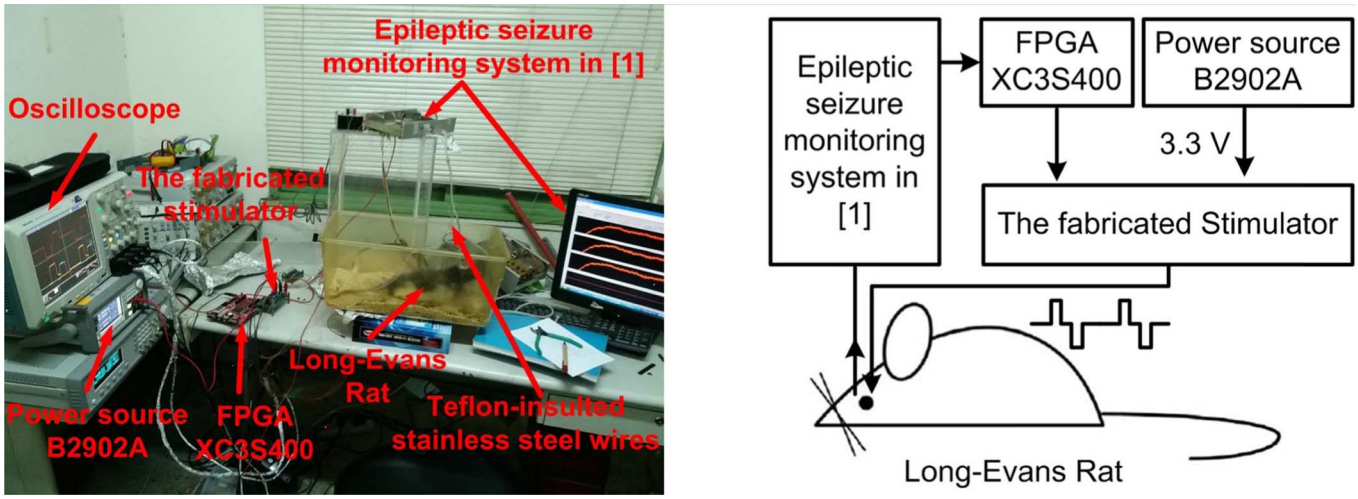


Fig. 8. (a) An oscilloscope capture of the voltage on the 500-nF Teflon capacitor at 2400-μA stimulus current, which allow measurements of the accumulated residual voltage at the end of the 100th biphasic stimulation. (b) The residual voltages on the loading capacitor C_{DL} in Fig. 1 and the charge mismatch of stimulation system vs. stimulus currents between adaptive and fixed supplies.

C. Animal Experiments

All the experiments done on animals and the experimental procedures were reviewed and approved by the Institutional Animal Care and Use Committee of National Cheng-Kung University, Taiwan. Fig. 9(a) depicts the measurement setup of the integration experiment of the proposed stimulator and the closed-loop epileptic seizure monitoring system. The adult Long-Evans rat suffered from spontaneous spike-wave discharges [7]. The electrodes for detection and stimulation were bilaterally implanted over the area of the frontal barrel cortex (lateral 2.0 mm, anterior 2.0 mm in relation to the bregma) and the right-side zona incerta of the Long-Evans rat (lateral 2.5 mm, posterior 4.0 mm and depth 6.7–7.2 mm). Teflon-insulted stainless steel wires (#7079, A-M Systems) having 50-μm diameter were used to measure the electroencephalography (EEG) signals and stimulus current. The epileptic seizure monitoring system was used to detect the epileptic seizures with intensive and rapid brain activities [1], [18]. Fig. 9(b) depicts the simplified diagram of the measurement setup for the animal test. The size of the LSB of the four-bit current DAC in the proposed stimulator is adjusted to 7 μA. Whenever the epileptic seizure monitoring system detects an epileptic seizure, the stimulator is manually activated. The stimulus current of the pulse train with an amplitude of ±35 μA, 0.5-ms pulse width, 2.5-ms period and 500-ms duration was used to suppress the epileptic seizure in the



(a) (b)

Fig. 9. (a) The measurement setup of the integration experiment of the proposed stimulator and the closed-loop epileptic seizure monitoring system. (b) Diagram of measurement setup for animal test.

TABLE I
PERFORMANCE COMPARISON WITH PRIOR STUDIES IN A LOW-VOLTAGE CMOS PROCESS

Parameter	JSSC 2013 [15]	TBCAS 2013 [19]	JSSC 2014 [7]	This work
Technology	0.5μm LV CMOS	65nm LV CMOS	0.18μm LV CMOS	0.18μm LV CMOS
Applications	CCS- Stimulator	CCS-Stimulator	CCS-Stimulator	CCS-Stimulator
Operation Voltage	2.5~4.6 V with 0.3V step	±2.5V	10V	6.7~12.3 V with 0.8V step
Output Stage Stacked Buffer	1PMOS/1NMOS	2PMOS/2NMOS	3PMOS/3NMOS	4PMOS/4NMOS
Output Buffer Bias Technique	-	Dynamic bias according to stimulation phase	Dynamic bias according to stimulation phase	Self-adaption bias technique
Reliability Measurements in the Off State	-	No	No	Yes
Charge Mismatch	-	≤2.24%	-	≤0.3%@the fixed supply ≤1.7%@the adaptive supply
System Power Efficiency	58%@1.5mA	-	-	56%@2.4mA

Long-Evans rat. Fig. 10 depicts an oscilloscope capture of the voltages on the electrodes. AHGS is turned on to generate a 12.3-V power supply for the stimulator. Subsequently, the cathodic stimulation and power supply self-adjusting operations are activated. After the power supply self-adjusting operation in the interphase interval is completed, AHGS is adjusted to generate the 8.3-V power supply for the stimulator with 2.3-V voltage headroom. Fig. 11(a) and Fig. 11(b) show

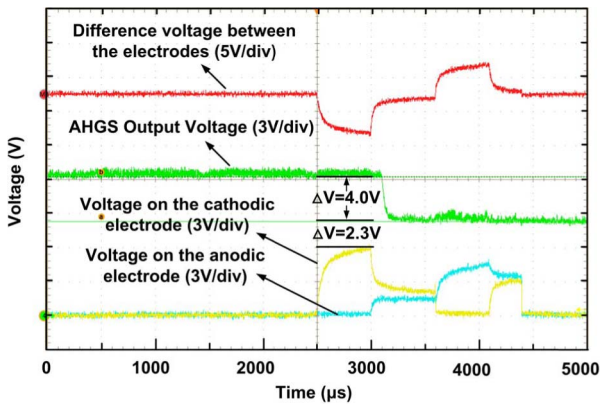


Fig. 10. An oscilloscope capture of the voltages on the electrodes and output port of AHGS in the animal test. The stimulus current is 35 μA.

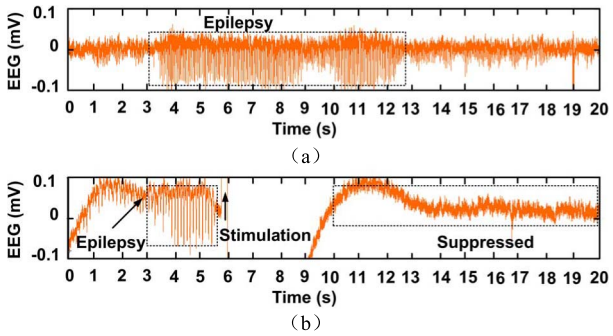


Fig. 11. Experimental results on EEG signals of the Long-Evans rat (a) without stimulation, and (b) with stimulation in the adaptive supply.

the EEG signals of the Long-Evans rat without and with the applied stimulation, respectively. In Fig. 11(a), the epileptic discharges are observed from 3.5 to 12.5 s. In Fig. 11(b), the intensive and rapid brain activities can be suppressed by stimulation in the adaptive supply.

Based on the animal experiment results, the functionalities of the proposed stimulator have been successfully verified.

D. Reliability Measurement Results

We performed reliability measurement experiments for up to 100 million biphasic stimulus cycles with ±3000-μA amplitude, 0.5-ms pulse width and 2.5-ms period. During each biphasic stimulus cycle, AHGS was turned on firstly to generate a 12.3-V output voltage. Then, the biphasic stimulation and power supply self-adjusting operation were activated. After one biphasic stimulus cycle was finished, AHGS was turned off until the next biphasic stimulus cycle began. The results showed that the performances of AHGS, HVC and the stimulator do not degrade.

E. Performance Comparison With Prior Works

Table 1 summarises the performances of the proposed high-voltage-tolerant stimulator relative to prior studies in the LV CMOS process. The use of the NMOS transistors with deep n-well layers made it possible to increase the operation voltage of the proposed stimulator to 12 V. In addition, the reliability measurement results have verified that the proposed stimulator is robust. The charge mismatch in this study is less than 0.3% and 1.7% under fixed and adaptive supplies, respectively. The system power efficiency is 56% at the 2400-μA stimulus current.

IV. Conclusion

A charge-balanced and high-voltage-tolerant stimulator was designed and successfully verified in a 0.18-μm 1.8-V/3.3-V CMOS process. It can be fully integrated with the microcontroller or the biomedical signal processor into an SoC chip fabricated by using the LV CMOS technology for enhancing integration and reducing the size. The experimental results have shown that the proposed dynamic power supply technique for current controlled stimulator can greatly improve the power efficiency. The reliability measurements and in vivo experiments have verified that the proposed stimulator is robust for inducing electrical stimulation in medical applications.

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