Improving Safe-Operating-Area of a 5-V n-Channel Large Array MOSFET in a 0.15-μm BCD Process

Karuna Nidhi, Ming-Dou Ker, *Fellow, IEEE*, Tingyou Lin, and Jian-Hsing Lee

***Abstract*— The safe-operating-area (SOA) of large array device (LAD) is one of the most important factors affecting the device reliability. In this paper, the improvement of the electrical-SOA (E-SOA) and the thermal-SOA (T-SOA) by using an optional implantation layer for 5-V n-channel large array MOSFET has been investigated in a 0.15-μm bipolar-CMOS-DMOS process. Experimental results showed that the secondary breakdown current (It2) is improved by 5 times, and a significant improvement is also observed in the E-SOA and the T-SOA boundary as compared to the original device. In addition, the impact of inserting additional layout pick-ups into the multiple-finger layout of large array MOSFET to the E-SOA, It2, and trigger voltage is also practically investigated in silicon for the LAD with a total width of 12 000 μm.**

***Index Terms*— Electrical-SOA (E-SOA), large array device (LAD), safe-operating-area (SOA), thermal-SOA (T-SOA), transmission line pulsing (TLP).**

I. Introduction

IN THE last few decades, as the demand increased for advance smart power with portable devices and system, it caused an excess need for development of low-voltage and low-power techniques, which meets modern IC design requirements. Low-voltage power MOSFETs with high avalanche capability and low specific ON-resistance are needed for automobile electric power steering, microprocessors, dc to dc converters, lights, battery charging, and other energy consuming applications [1]–[3]. However, continuously scaling in technologies and enhancement of device functions of designed circuit, plenty of works had been aimed in achieving the highest breakdown voltage (BV), lowest ON-resistance, and widest the safe-operating-area (SOA) possible for a given device size. The impact of the device size and related tradeoffs with the BV and specific ON resistance is the most important factor for improving the SOA performances [4]–[8]. The boundary of SOA is under control of the device engineer, but due to the thermal and the electrical mechanism of the device, its determination is not easy to handle. Under typical applications, depending on the time scale of applied stress, either the electrical or the thermal effects will dominate, which can lead to device failure. The way of characterizing the SOA limit does not depend on single safe-operating range but in many different curves those depend on device's geometry and their operating conditions. The shape of these ranges majorly depends on parameters such as the device area A, the pulse time t_{pulse}, the junction temperature T_J, and the ambient temperature T_A. Fig. 1 shows the reduction in the SOA boundary, which often occurs in a typical power MOS transistor due to the electrical and the thermal instability for shorter and longer pulse widths, respectively [4]–[13]. The degradation in the SOA boundary due to the electrical and the thermal behavior of the device is likely to be minimized by the process optimizations and proper layout modifications. Large array devices (LADs) due to their high current driving ability play an important role and have been widely used in the semiconductor industries to achieve high avalanche capability. LADs are usually defined as the device size more

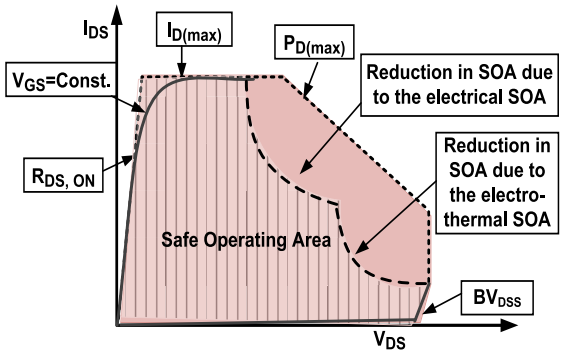

Fig. 1. Reduction in SOA due to the E-SOA and the T-SOA for shorter and longer pulse widths, respectively.

Manuscript received April 12, 2018; revised May 9, 2018; accepted May 16, 2018. Date of publication May 30, 2018; date of current version June 19, 2018. This work was supported by the Ministry of Science and Technology, Taiwan, under Contract MOST 107-2622-8-009-006-TE1. The review of this paper was arranged by Editor B. Zhang. *(Corresponding author: Ming-Dou Ker.)*

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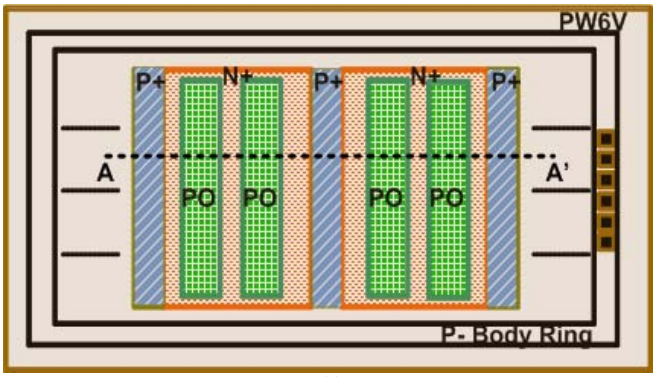
Digital Object Identifier 10.1109/TED.2018.2838545



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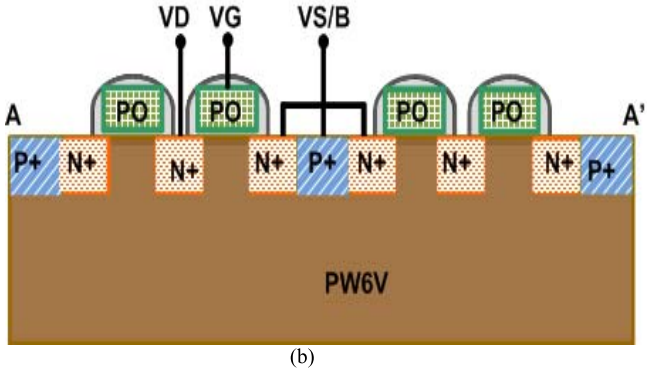
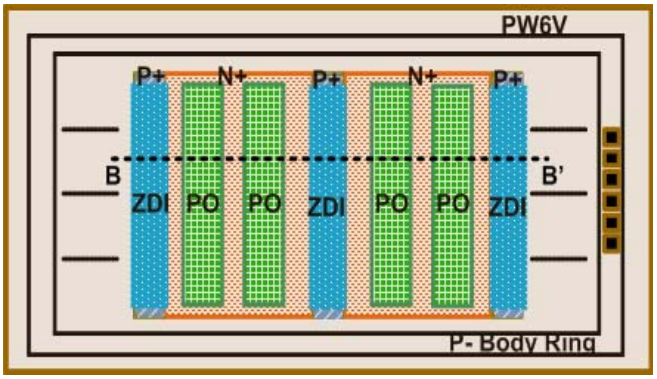


(b)

Fig. 2. (a) Layout top view and (b) cross-sectional view along the A–A′ line for the original device, in which P+ body pickup is inserted after every two fingers.



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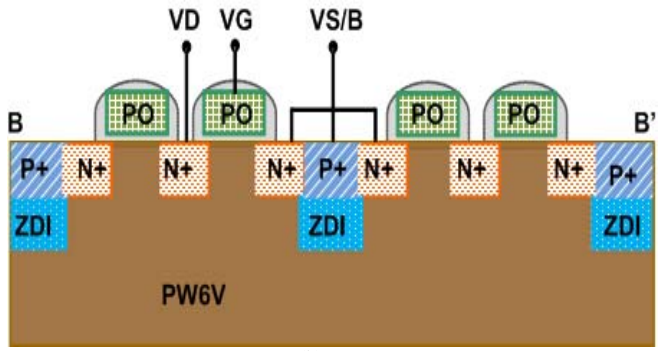


(b)

Fig. 3. (a) Layout top view and (b) cross-sectional view along the B–B′ line with an additional implantation (ZDI) in the original device, in which P+ body pickup is inserted after every two fingers.

than 5000 μm, designed by multifinger style to carry huge amount of current to drive large output loading [12]–[16].

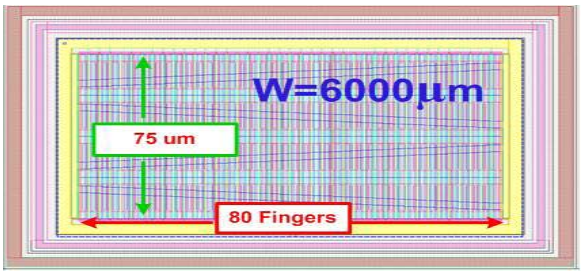
Recently, several different approaches have been reported to improve and optimize the SOA performance of LAD HVMOSFETs which is uttered most important for designers dealing with the high-voltage IC's applications. Several self-protection solutions have been proposed such as improving the device robustness by layout techniques [14]–[17], use of RESURFs and field plate techniques [18]–[20], process optimizations [21]–[23], or embedding SCR structures into LAD [23], [24]. However, unlikely to HVMOSFETs, a very few low-voltage studies were found for the SOA either it for the electrical or the thermal instability, especially for low voltages (lower than 10 V) devices. An optimization of low-voltage n-channel laterally diffused metal oxide semiconductor was reported by the 2-D-modeling technique with trap density simulation to achieve required electrical and lifetime SOA [25]. An analytical model was proposed for the thermal instability of a low-voltage power MOS and its SOA was reported in pulse operation mode [26]. The electrical-SOA (E-SOA) of low voltage was published for silicon carbide nMOS transistor [27]. Apart from these, a simple and useful layout scheme was shown to achieve the uniform current distribution for multifinger silicided gate grounded LV nMOS [28]. The most important need for the SOA in LV devices is for switching applications, as external switch should protect the circuit to be turned OFF by having over current, over voltage, and over temperature protections.

In this paper, 5-V n-channel low-voltage LAD in a 0.15-μm bipolar-CMOS-DMOS (BCD) process is studied. It was found to have poor SOA boundary for the original device. A significant improvement is noticed in the E-SOA and the thermal-SOA (T-SOA) as compared to original device after using an additional implantation at body area. The impact of layout pick-ups over trigger voltage (Vt1), secondary breakdown current (It2), and the E-SOA is also studied.

II. Device Structure and DC Characteristics

The LV MOS studied in this paper is fabricated in a 0.15-μm BCD process. Layout top view of n-channel 5-V (NCH) LV MOS device is shown in Fig. 2(a). The original device without additional layer is labeled as NCH. All n-channel LAD device structures have P+ guard ring surrounding the whole NCH device to define the (substrate) body potential. Due to P+ guard ring, the parasitic n-p-n bipolar junction transistors (BJTs) with different substrate resistances (R_{SUB}) will substantially affect the turn-ON uniformity in LADs. To improve the It2, the additional body pick-up structures of "two fingers per pickup" are inserted into source region of NCH LAD, which will effectively balance the R_{SUB} between parasitic BJTs. The cross-sectional view along the A–A′ region is shown in Fig. 2(b).

Without modifying the original structure, to study the impact on the SOA due to an additional p-type Boron implantation, named as zener diode implant (ZDI) implantation at the P+ body area, the layout top view, and the device cross-sectional view along the B–B′ region with additional ZDI



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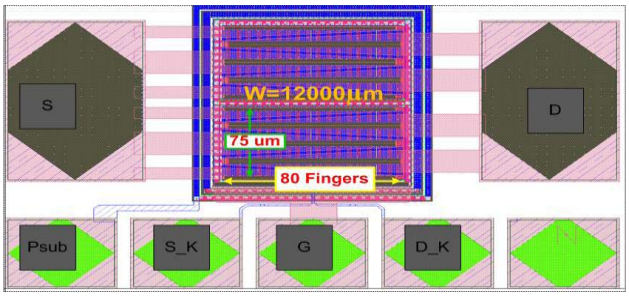


(b)

Fig. 4. Layouts of the test devices with (a) $W = 6000\ \mu$m and (b) $W = 12\,000\ \mu$m, shown with pads.

TABLE I
COMPARISON OF DC CHARACTERISTICS

Device	BV (V)	V_{th} (V)	R_{onsp}(mΩ-mm^2)		
			With Metal routing	Without Metal routing	SPICE model
NCH	10	0.75	2.54	2.26	2.2
NCH_ZDI	10	0.76	2.56	2.27	2.2

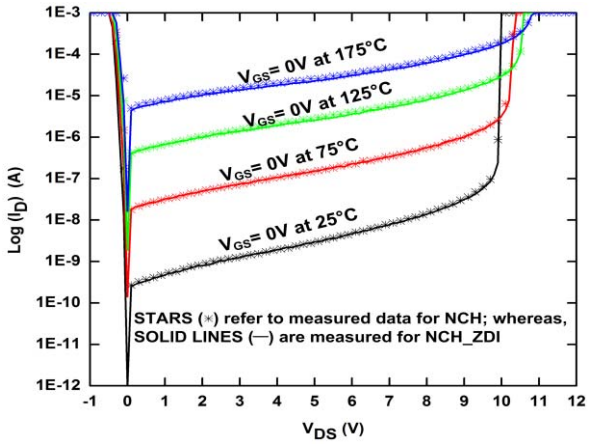


Fig. 5. Measured log drain current (Log I_D) versus drain voltage (V_{DS}) at different temperatures under $W = 12\,000\ \mu$m.

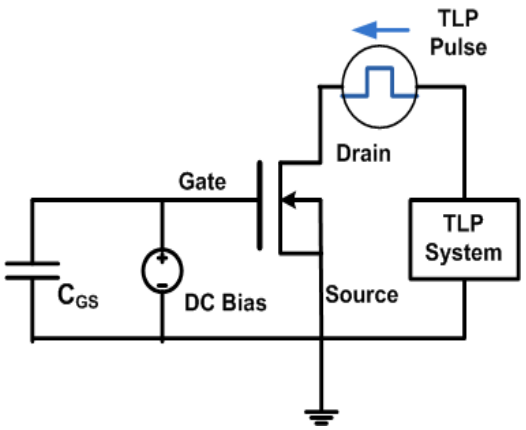


Fig. 6. TLP setup for measuring the E-SOA curves and It2.

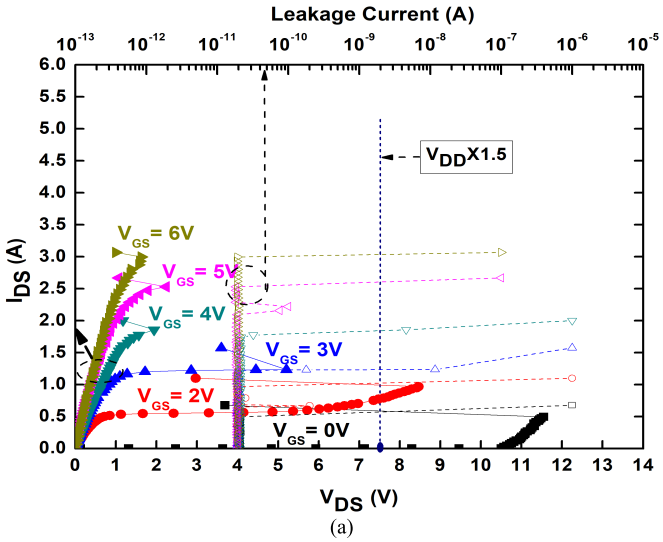
implantation layer are shown in Fig. 3(a) and (b), respectively. ZDI layer is an optional layer provided by foundry. The device with the additional layer is labeled as NCH_ZDI.

To emulate the high current driving capability of output array in power applications, LAD structures were drawn in this paper. Its layout is drawn in multifinger layout style with a total effective width (W) of 6000 μm (80 fingers) and 12 000 μm (2 $\times$ 80 fingers) is shown in Fig. 4(a) and (b), respectively. Large area bipolar transistors may have a nonuniform current distribution due to the resistance of the base layer. To have the better uniform current distribution, source and drain diffusion fingers are kept smooth to avoid current crowding and overheating effect in the device. Each device width and the channel length are kept the same in the layout for all studied devices, i.e., 75 and 0.6 μm, respectively.

DC characteristics including BV, threshold voltage (V_{th}), and specific ON-resistance ($R_{ON,sp}$) of LAD must be examined carefully to achieve the optimal performances and to prevent the failures during their operations. The dc parameters are extracted from both devices (NCH and NCH_ZDI) by Agilent B1500A semiconductor device parameter analyzer. Fig. 5 shows Log (I_D) versus V_{DS} curves comparison for both devices at $V_{GS} = 0$ V (OFF-state mode) under different temperatures. Drain currents are almost the same for both devices in dc IV measurement under high temperatures. Table I shows the comparison of dc behaviors between NCH and NCH_ZDI of 12 000 μm. The specific ON-resistance is calculated with and without metal routing using Kelvin measurement (four wires measurement) and compared with SPICE model. The dc data comparisons show that both devices share similar kind of structure and ZDI implantation will not affect the device basic dc performances.

III. ELECTRICAL-SOA OF NCH AND NCH_ZDI

To analyze the impact of additional ZDI layer to device ruggedness under normal circuit operations, the E-SOA needs to be determined. The E-SOA is defined as the boundary region in the I_{DS}–V_{DS} plane for which the intrinsic bipolar transistor is triggered only by avalanche current. The electrical voltage is applied under very short stress pulses, i.e., in nanosecond pulses, so the device has no time to generate heat. A transmission line pulsing (TLP) can be used for generating such pulses. In this paper, the TLP pulse with a 100-ns pulsewidth and 10-ns rise/fall time is used for the E-SOA characterization. The TLP setup is shown in Fig. 6, where the gate is externally biased by a power supply to provide a fixed gate bias. A decoupling capacitor C_{GS} of 4.7 nF is placed between the source and the gate to stabilize the gate voltage



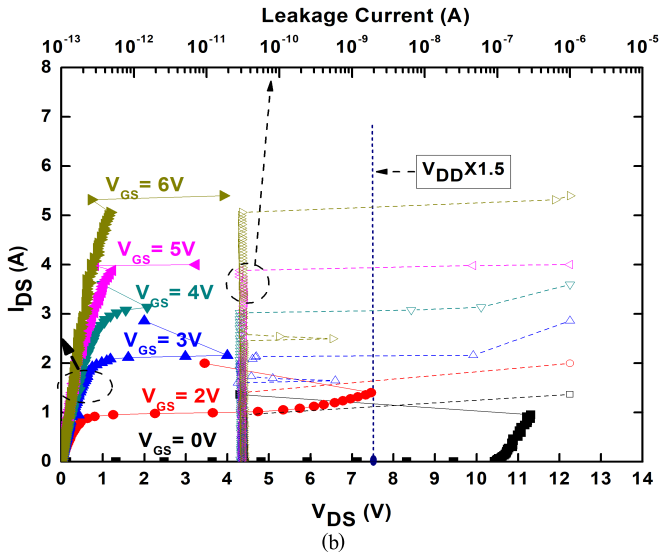
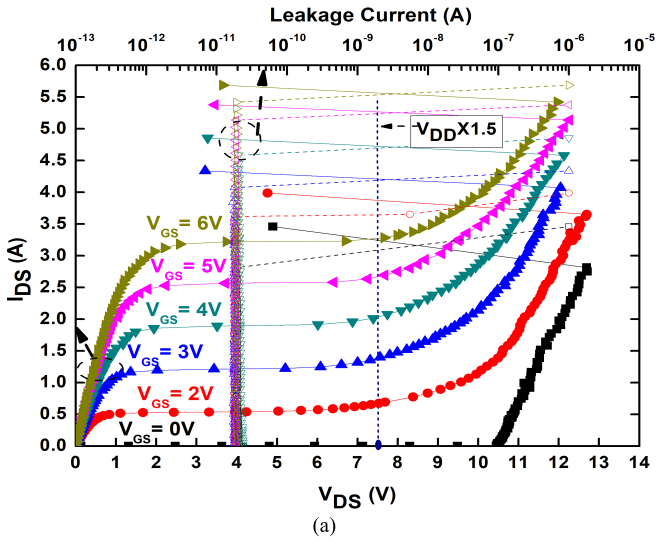


Fig. 7. E-SOA curves of NCH for different gate bias voltages (V_{GS}) under (a) $W = 6000\ \mu$m and (b) $W = 12\,000\ \mu$m. The leakage current is measured in off-state condition after every step of the TLP measurement.



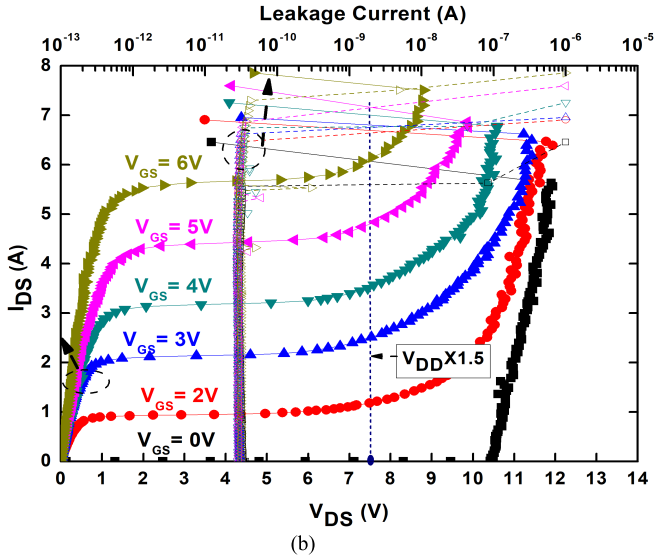


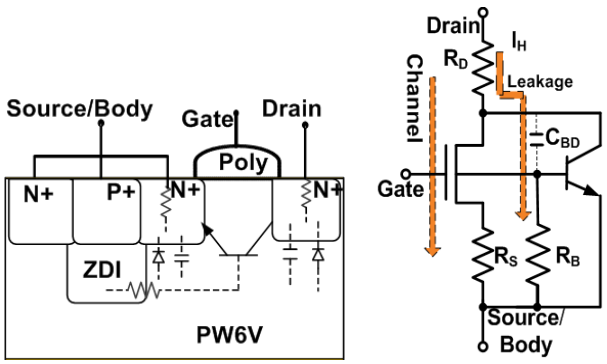
Fig. 8. E-SOA curves of NCH_ZDI for different gate bias voltages (V_{GS}) under (a) $W = 6000\ \mu$m and (b) $W = 12\,000\ \mu$m. The leakage current is measured in off-state condition after every step of the TLP measurement.

during TLP pulsing [29]–[31]. The TLP system is used to provide pulses to stress the device under test until the parasitic BJT enters into snapback area.

The E-SOA curves for the original 5-V LV (NCH) LAD are extracted on wafer, where TLP with 100-ns positive pulse was used to stress on drain of the device until it snaps back. To verify the device behavior during E-SOA measurement, the leakage current is measured after each increasing stress pulse. TLP setup was done in such a way that after each increasing stress pulse, the device leakage is measured in its OFF-state condition ($V_{GS} = 0$ V). When the leakage current reaches a set criterion value, the device is defined as failed. The failure criterion of the E-SOA tests is 1-μA leakage current under 5-V drain bias voltage. The resulting E-SOA curves for different gate bias voltages under 6000 and 12 000 μm are shown in Fig. 7(a) and (b), respectively. The E-SOA characteristics of this NCH device are poor and it failed immediately under higher V_{GS}. At higher V_{GS} under high V_{DS}, the high field region will be shifted near the drain contact to cause a negative resistance known as "snapback" occurred due to electrical failure. It is hard to observe the snapback curves in LAD structure because such a structure failed immediately once device enters into snapback region. This is often termed as secondary breakdown of LAD MOSFET.

Fig. 8(a) and (b) shows the E-SOA curves of NCH_ZDI under 6000 and 12 000 μm, respectively. From the E-SOA plots for NCH and NCH_ZDI as shown in Figs. 7 and 8, it is clear that adding ZDI implantation in P+ body area is an effective way to improve the E-SOA boundary almost by 5 times as comparing to the original device without degradation on the driving current.

The device cross-sectional view is shown in Fig. 9(a) during TLP measurement. The n-p-n BJT is formed including N+ source and drain, and p-well body without the optional ZDI layer. During the TLP mode, the channel path and the leakage path are shown in equivalent circuit model in Fig. 9(b), where



(a) (b)

Fig. 9. (a) Device cross-sectional view during TLP measurement. (b) Equivalent circuit model.

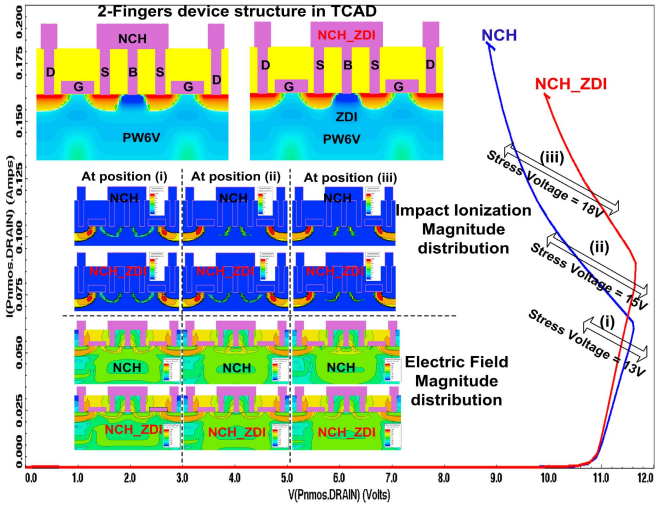


Fig. 10. Comparison on TCAD simulation results of NCH and NCH_ZDI under two fingers, including device structure, impact ionization, and the electric field distribution at different positions marked on TLP curve. (i) Before snapback. (ii) NCH snapback. (iii) NCH_ZDI snapback.

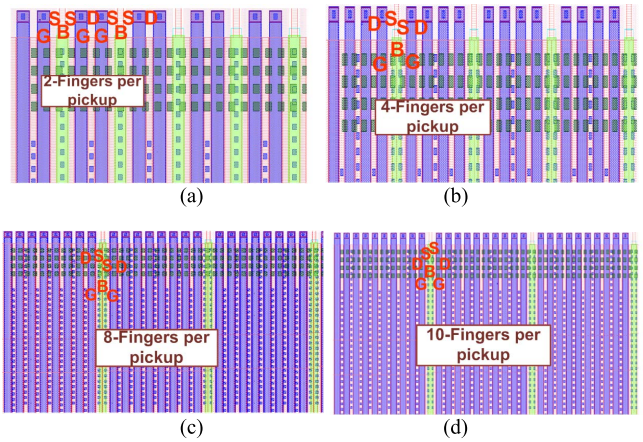


Fig. 11. Layout diagrams showing NCH devices with an additional P+ pickup is used after every (a) two, (b) four, (c) eight, and (d) 10 fingers in source of NCH. All tested NCH and NCH_DIO devices have the same effective device dimension of 12 000 μm (2 $\times$ 80 fingers with each finger width of 75 μm).

R_D, R_S, and R_B are the drain, the source, and the body (parasitic) resistors of MOS, respectively. C_{BD} is the body-drain capacitor and I_H is the hole current that can forward bias the BJT base–emitter junction through R_B to trigger on the intrinsic BJT. The combination of capacitance (C_{BD}), R_B, impact ionization, and the hole current will produce sufficient voltage across the body-drain capacitor and the body resistance to turn ON the intrinsic n-p-n BJT.

The major source of the current at I_H from TLP pulse is avalanche generated holes

$$I_H \approx I_{\mathrm{AV}} \tag{1}$$

where I_{AV} is the avalanche current generated by holes.

These strong paths cause maximum flow of current to induce damage on the device during TLP measurement. In this case, the device will exhibit low impedance, negative resistance, and without gate control. From Ohm's law, reducing the R_B can decrease the voltage drop on the resistor to prevent the BJT to turn ON. So, in order to suppress bipolar from turning on, a p-type layer (ZDI) at the P+ body area will reduce the parasitic resistance due to higher doping concentration than that of p-well. The early snapback to low voltage is attributed to the electric field localization at P+/PW6V diffused junction in case of NCH while adding ZDI implantation in bulk region improves the onset of snapback due to reduction in base resistance and eventually leads to higher It2 in device NCH_ZDI.

To understand the mechanism in the test results, a 2-D device simulation with Taurus Medici is performed for NCH and NCH_ZDI under two fingers structure. Fig. 10 shows the distribution of impact ionization and the electric field at positions, (i), (ii), and (iii), as marked on TLP curve for different stress voltages of 13, 15, and 18 V, respectively. At the position (i), when both devices are in safe region, i.e., no snapback, both devices have almost similar distribution of impact ionization, the electric field, and the total current. At the position (ii), during NCH device has snapback but NCH_ZDI is still in safe region, it shows that the electric field and impact ionization have nonuniform distribution around source-body area for NCH device as comparing to NCH_ZDI. Such kind of distributions indicate that at the stress voltage of 15 V, the current density is higher than PW6V doping concentration, and the localized electric field can result into impact ionization. The generated holes are drifted toward the source side and p-well. The hole current starts to flow in the base of BJT as voltage drop across base resistance that switches to base current and corresponding collector current. Once the hole current is large enough, the source-body injection becomes forward biased. On the other hand, ZDI doping concentration is much higher than that of p-well (PW6V), which will add extra resistance for holes and prevent the BJT to turn ON. At the position (iii), impact ionization process builds up and generates holes at higher stress voltage in case of NCH_ZDI. The device suffers snapback when impact ionization distribution becomes more around body with increase in current. The TLP comparison for two fingers devices showed that the NCH_ZDI device achieves higher

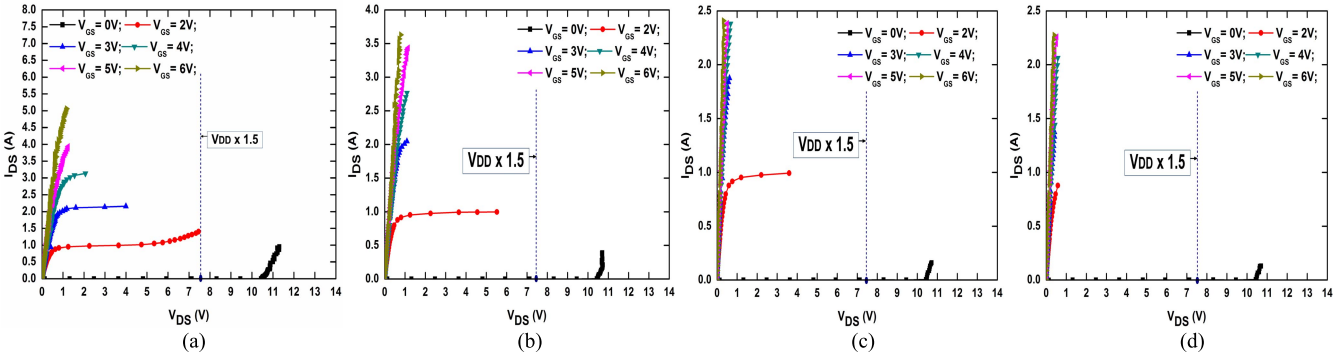


Fig. 12. Measured E-SOA curves for NCH devices with (a) two, (b) four, (c) eight, and (d) 10 fingers per P+ pickup under the same effective dimension of 12 000 μm.

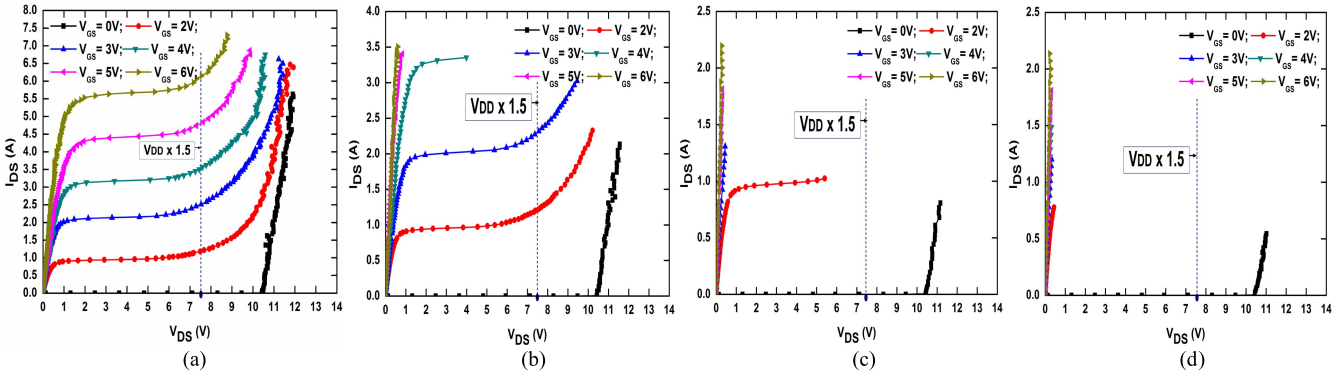


Fig. 13. Measured E-SOA curves for NCH_ZDI devices with (a) two, (b) four, (c) eight, and (d) 10 fingers per P+ pickup under the same effective dimension of 12 000 μm.

It2 as comparing to NCH, while their trigger voltages (Vt1) are the same.

To overcome the nonuniform turn-ON problem (caused by unequal substrate resistance among the center and side fingers) by inserting pickups was proposed in multifingered structures, so that each finger could have an equal equivalent substrate resistance [14], [16], [32]–[34]. To clarify the effect of additional layout pickups to the E-SOA of LV n-channel LAD MOSFET, different number of fingers per pickup were inserted into NCH and NCH_ZDI devices. Layout top views of NCH with additional pickup are used after every two, four, eight, and 10 fingers as shown in Fig. 11(a)–(d), respectively. All tested NCH and NCH_ZDI devices have the same effective device dimension of 12 000 μm with single device length is 75 μm and the same layout style, except for the arrangement of fingers per additional pickup.

The E-SOA curves for an additional pickup after every two, four, eight, and 10 fingers of NCH LAD structure are shown in Fig. 12(a)–(d), respectively. The Vt1 of all devices are almost the same. From Fig. 12, it can be observed that nearer the pickups in LAD structures, better the TLP measured E-SOA boundary for the device. The same trend is observed for the similar structure with an optional implantation in NCH_ZDI, as shown in Fig. 13(a)–(d). The E-SOA curves without additional pickup is not drawn in this paper because of poor E-SOA performance (more poorer than using a pickup after every 10 fingers).

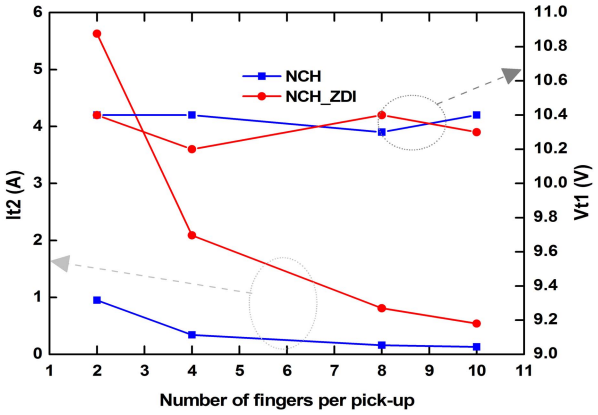


Fig. 14. Measured relation between It2, Vt1, and the number of fingers per pickup for NCH and NCH_ZDI devices under $W = 12\,000$ μm.

The variation in the It2 with respect to number of fingers per pickup gives design flexibility with LAD structure, especially in the case with an optional implantation device (NCH_ZDI). Fig. 14 shows the measured relation between It2, Vt1, and the number of fingers per pickup for NCH and NCH_ZDI devices under $W = 12\,000$ μm. From these experimental results, it is clear that inserting additional layout pickups results in significant improvement on It2 and the E-SOA boundary without affecting the Vt1 of n-channel low-voltage LADs in the 0.15-μm technology.

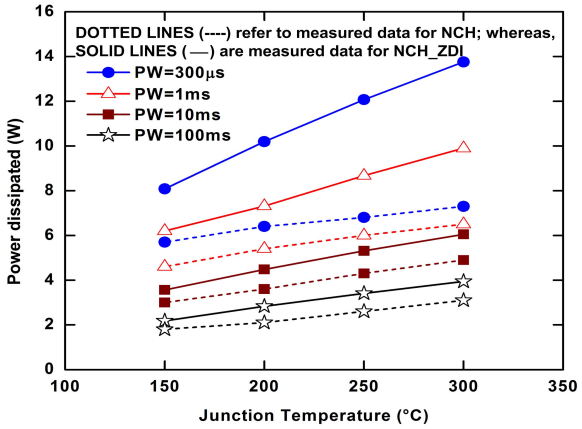


Fig. 15. Junction temperature as a function of maximum power dissipation for NCH and NCH_ZDI are compared for different pulse widths under $W = 12\,000\ \mu$m.

IV. Thermal-SOA of NCH and NCH_ZDI

The basic principle of the thermal analysis is similar to that in the electrical domain. The T-SOA boundary is defined by the device being on verge of the thermal runaway due to triggering of the intrinsic bipolar only by the thermal generation current for long stress pulses. Once applying long pulses to the device, the generation of heat will take place because of the internal power dissipation leading to the thermal trigger of bipolar. A MOSFET (or generally a system) is considered to be thermally unstable in case the power generation rises faster than the power dissipation over temperature [3]–[7], [9]–[13]. Self-heating in the device will increase the junction temperature and lead to the device failure. The concept of the junction temperature is based on the electrical and the thermal properties of materials, thermal resistance, and the heat flow. The specified thermal resistance is used to calculate the device junction temperature as a function of power dissipation under a given ambient temperature is expressed as

$$P_{D\,\max} = \frac{T_J - T_A}{R_{\theta \mathrm{JA}}} \tag{2}$$

where

$$R_{\theta \mathrm{JA}} \approx R_{\theta \mathrm{JC}} + R_{\theta \mathrm{CA}} \tag{3}$$

where P_{Dmax} is maximum the power dissipation (W), T_J is the absolute junction temperature (°C), T_A is the ambient temperature (°C), $R_{\theta \mathrm{JA}}$ is the thermal coefficient between the junction and the ambient (°C/W), $R_{\theta \mathrm{JC}}$ is the thermal coefficient from silicon junction to the case (°C/W), and $R_{\theta \mathrm{CA}}$ is the thermal coefficient from the case to the ambient air (°C/W).

The performance of the T-SOA is strongly dependent on package type, device size, and device layout. In this paper, a well-known test procedure from JEDEC is followed to evaluate the thermal runaway performance for LAD having total effective width (W) of 12 000 μm (2 × 80 fingers) as shown in Fig. 4(b), using TESEC-9424-KT under SOP-8 package which can be considered as the worst case package type for power applications [35]. The T-SOA for LAD is characterized by

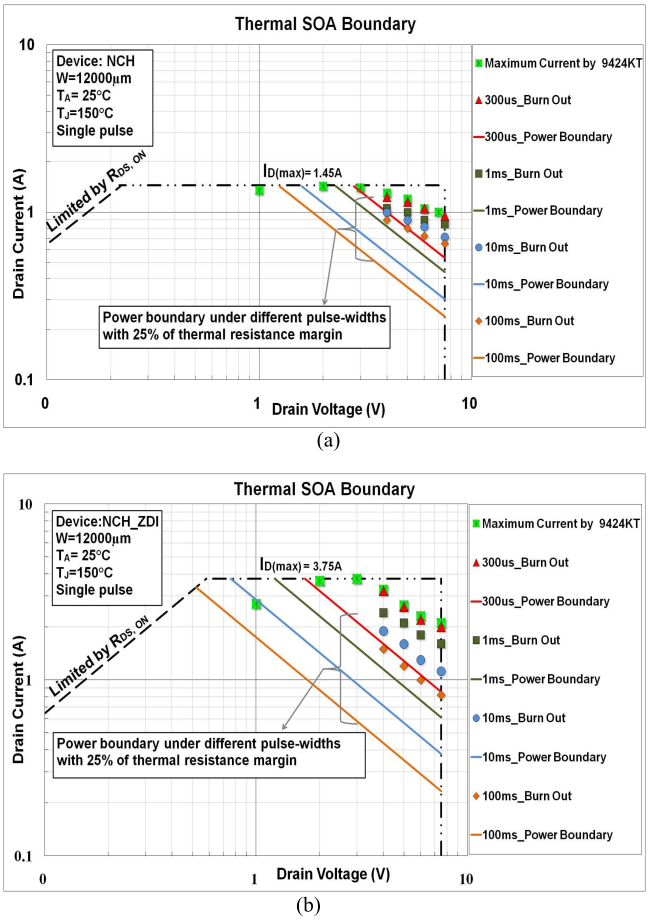


Fig. 16. Calculated T-SOA boundary at different pulse widths from device burn-out condition with 25% of thermal resistance margin under $W = 12\,000\ \mu$m for (a) NCH and (b) NCH_ZDI.

applying different power pulse widths (≥300 μs), the device will heat up, and eventually will trigger the parasitic bipolar transistor to cause the thermal runaway failure. The junction temperature as a function of power dissipated for NCH and NCH_ZDI under different pulse widths is shown in Fig. 15. The device using ZDI implant can dissipate more power than the original device under different pulse widths. The differences in power dissipation between NCH and NCH_ZDI become lower at the pulse widths of 10 and 100 ms, as comparing to that of 300 μs and 1 ms, because of the thermal impedance limitation of SOP-8 package type.

The power boundary in the T-SOA plot is calculated from the device burned-out condition with the additional thermal resistance margin of 25% and limited for the maximum junction temperature of 150 °C, which gives a wide flexibility to designer for their applications. It is defined as the maximum power of the device that is allowed to generate and to reach a stable junction temperature (150 °C) in thermal equilibrium and ambient temperature (25 °C). The calculated T-SOA boundary for NCH and NCH_ZDI is drawn for $V_{\mathrm{DS}} = 1.5 \times V_{\mathrm{DD}} = 7.5$ V under $W = 12\,000\ \mu$m, as shown in Fig. 16(a) and (b), respectively. The maximum drain currents are 1.43 and 3.75 A under the pulsewidth of 300 μs for NCH and NCH_ZDI, respectively. Fig. 15 shows that the device

using ZDI implantation is thermally more balanced and more stable at the junction temperature equal to 150 °C. When ON-state operation of the device is longer than hundreds of microseconds, the I_{DS}–V_{DS} is mainly limited by the thermal effects. Additional electrical contribution from the hole current will reduce the critical temperature of catastrophic bipolar triggering at higher V_{DS} condition. The thermal aspects of transistors are dominated by the properties of silicon, no major difference is observed between different structures of the same area with identical layout.

V. Conclusion

The improvement of the E-SOA and the T-SOA by using an optional implantation layer (ZDI) at the P+ body area of a 5-V n-channel large array MOSFET has been investigated in a 0.15-μm BCD process. Measurement results verified that the It2 is improved by more than 5 times, as well as the E-SOA in-compare to original device without affecting their dc performances. In addition, the impact of inserting additional layout pickups results in significant improvement on It2 and the E-SOA boundary while the Vt1 remains the same for the LAD layout with a total width of 12 000 μm. The T-SOA boundary is also compared and shows improvement by the additional layout pickups.

Acknowledgment

The authors would like to thank C.-L. Tu, S.-C. Huang, and Y.-N. Jou for their valuable technical suggestions. They would also like to thank Vanguard International Semiconductor Corporation, Hsinchu, Taiwan, for the chip fabrication and measurement support.

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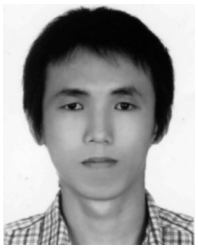

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