A Fully Integrated 16-Channel Closed-Loop Neural-Prosthetic CMOS SoC With Wireless Power and Bidirectional Data Telemetry for Real-Time Efficient Human Epileptic Seizure Control

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***Abstract*— A 16-channel closed-loop neuromodulation system-on-chip (SoC) for human epileptic seizure control is proposed and designed. In the proposed SoC, a 16-channel neural-signal acquisition unit (NSAU), a biosignal processor (BSP), a 16-channel high-voltage-tolerant stimulator (HVTS), and wireless power and bidirectional data telemetry are designed. In the NSAU, the input protection circuit is used to prevent MOSFET from overstressing by the high-voltage stimulations. Hence, NSAUs can share electrodes with stimulators. The auto-reset chopper-stabilized capacitive-coupled instrumentation amplifiers (AR-CSCCIAs) are designed with the chopper-stabilized technique with a new offset reduction loop. The measured input-referred noise is 2.09 μV_{rms} and the noise-efficiency factor (NEF) is 3.78. The entropy-and-spectrum seizure detection algorithm is implemented in the BSP with 0.76-s seizure detection latency and 97.8% detection accuracy. When the seizure onset is detected by the BSP, the HVTS with adaptive supply control delivers 0.5–3-mA biphasic current stimulation to suppress the seizure onset. The proposed SoC is powered wirelessly, and the bidirectional data telemetry is realized through the same pair of coils in 13.56 MHz. The downlink data rate is 211 Kb/s with the binary phase-shift keying (BPSK) modulation and a new BPSK demodulator. The uplink data rate is 106 Kb/s with the load-shift keying (LSK) modulation. The proposed SoC is fabricated in a 0.18-μm CMOS technology and occupies 25 mm^2. Electrical tests have been performed to characterize the SoC performance. In vivo animal experiments using mini-pigs have been performed to successfully verify the closed-loop neuromodulation functions on epileptic seizure suppression.**

***Index Terms*— Closed-loop seizure control, low-noise neural-signal amplifier, neuromodulation system-on-chip (SoC), wireless bidirectional data telemetry, wireless power transmission.**

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I. Introduction

EPILEPSY, the common neurological disorder, afflicts about 1% of the world's population. It is characterized by recurrent seizures that occur after an episode of abnormal electrical activities in the brain. Epileptic seizures may cause a brief lapse of attention, unnatural posturing, or severe and prolonged convulsions. The unexpected seizures impact the quality of life of patients and their families.

Currently, the common treatment for epilepsy is medication. However, around 30% of epileptic patients are still drug resistant or have intolerable adverse effects. For these patients, the resection surgery of the seizure onset region in the brain might be beneficial. However, the risks of neurologic deficits

after the surgery, such as memory impairment, visual field loss, or movement malfunctions, are always of great concern.

Electrical neuromodulation on the central nervous system for drug-resistant epileptic patients has been attempted, and the preliminary results have shown that it could be a promising solution (see [1], [2]). There are two types of neuromodulation systems, namely, open-loop and closed-loop systems. In open-loop neuromodulation systems, continuous electrical stimulation is delivered to the brain, leading to a higher power dissipation which decreases the battery lifetime of the implanted devices.

On the other hand, the emerging closed-loop or responsive neuromodulation systems for epilepsy deliver electrical impulses to a selected brain region in response to the detected epileptic or pre-epileptic activities [3]–[7]. This is a more promising treatment for epilepsy because it can immediately and accurately detect epileptic activities and suppress seizures on the right brain region to achieve a higher treatment efficacy, less power dissipation, and longer battery lifetime.

As shown in clinical data [8], up to 3-mA electrical stimulation on the cortical surface at the seizure onset site is required to control human epileptic seizures. Recently, implantable medical devices (IMDs) with closed-loop electrical stimulation and wireless power/data telemetry for seizure control have been reported [4]–[6] as a potential and efficient clinical treatment. The closed-loop neural-prosthetic system with seizure detection achieves 0.8-s detection latency [4]. However, since the system is designed for rats, the stimulation current is only 30 μA. In [5], the stimulation current is up to 1 mA. In [6], the stimulation current is up to 1.35 mA; both are not enough for humans. Moreover, there are two frequency bands used in the implanted system for power and data transmission. The large antenna area could be an issue for the implanted system. In [7], the wireless power and data telemetry is not integrated into the SoC. The stimulation current is up to 1 mA, still not enough for humans.

The wireless power and bidirectional data telemetry is required in IMDs. So far, many structures have been reported [9]–[12]. Among them, wireless power and only uplink data telemetry has been proposed and realized in one pair of coils [9] or two pairs of coils [10]. In [11], only data telemetry is implemented on the chip with one pair of coils, while power telemetry has not been integrated on the same chip. In [12], only downlink telemetry is integrated with power telemetry in one pair of coils. However, the data rate is about only a few kilobits per second (b/s). In many medical applications, one pair of coils is preferred to fit the device size limit. Bidirectional data telemetry with the high data rate is required to transmit biosignals out and send data in to parameterize the implants through external control units.

A 16-channel closed-loop seizure control CMOS system-on-chip (SoC) for human epileptic seizure control [13] is presented in this paper. In this system, each channel (electrode) can sense electrocorticography (ECoG) and stimulate tissue independently. According to the clinician's experience, 16 channels (electrodes) can cover the possible seizure onset zone. Up to 3-mA biphasic stimulation current is designed to be delivered to the tissue. An input protection circuit in the front-end preamplifier sharing the same electrode with the stimulator is designed to protect the transistors from overstressing by high stimulation voltage [14], [15]. In [15], only the neural-signal acquisition unit (NSAU) is described. However, this paper presents the whole system including SoC and the wireless power and bidirectional data telemetry. The wireless power and bidirectional data telemetry circuits are designed to achieve high transmitted power with high power conversion efficiency (PCE) for the implantable SoC as well as to obtain high uplink and downlink data rates through the same pair of high-Q coils in the ISM band (13.56 MHz). In the wireless power transfer, a new $2\times/3\times$ active rectifier with 2- and 3-V output voltages and delay compensation is proposed to enhance the PCE. In the wireless data telemetry, a new binary phase-shift keying (BPSK) demodulator is proposed to demodulate the downlink BPSK data, and a load-shift keying (LSK) modulator is designed to transmit the ECoG data to the external device through the high-Q coils. The proposed closed-loop seizure control SoC achieves a high seizure detection accuracy of 97.8% within 0.76 s of detection latency as verified on the animal *in vivo* experiments of mini-pigs.

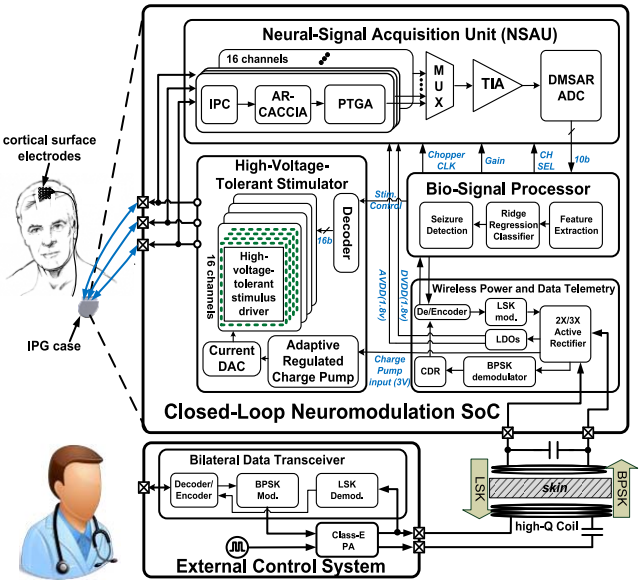

Fig. 1. Block diagram of the proposed closed-loop seizure control SoC and the external control system.

The paper is organized as follows. Section II describes the system architecture of the proposed implantable closed-loop seizure control SoC. In Section III, the circuit design and implementation details of each block are presented. The experimental results including both electrical measurement and animal tests are given in Section IV. Finally, the conclusion is drawn in Section V.

II. System Architecture

Fig. 1 shows the architecture of the overall microsystem including the closed-loop seizure control SoC in the implantable pulse generator (IPG) case, a pair of high-Q coils, and the chip of the external control system. In the SoC, an NSAU, a biosignal processor (BSP), a high-voltage-tolerant

stimulator (HVTS), and a wireless power and data telemetry unit are integrated. The signal processing flow is described as follows. The ECoG signals are sensed through the electrodes on the cortical surface and sent to the NSAU in the SoC. The sensed ECoG signals are amplified and processed by the auto-reset chopper-stabilized capacitive-coupled instrumentation amplifiers (AR-CSCCIAs), the programmable transconductance gain amplifiers (PTGAs), the multiplexer (MUX), and the transimpedance amplifier (TIA) [15]. Then, the signals are digitized by the delta-modulated successive approximation register analog-to-digital converter (SAR ADC) [16] and further processed by the BSP to extract both entropy and power spectral density in specific frequency bands for seizure detection. Once the seizure is detected, the BSP sends a stimulation control signal to activate the HVTS in order to generate biphasic stimulation currents to suppress abnormal brain activities. Moreover, the BSP also resets the memory. Thus, each seizure detection result is independent, which can avoid the instability of the closed-loop system. To achieve a constant stimulation current over a wide impedance range of electrode–tissue interface, the adaptive regulated charge pump, the current digital-to-analog converter (DAC), and high-voltage-tolerant stimulus drivers are used [17]. The adaptive regulated charge pump generates a high voltage up to 12 V without gate reliability issues in the low-voltage CMOS process. The output voltage is regulated by the pulse frequency modulation (PFM) feedback. The maximum output stimulation current is 3 mA. The control clock of each charge pump stage has a phase shift from each other, which can reduce the maximum peak current from the 3-V supply voltage provided by the $2\times/3\times$ active rectifier. The adaptive supply voltage control technique is used in the adaptive charge pump, which can reduce the conduction loss on a high-voltage-tolerant stimulus driver.

The external control system consists of a bidirectional data transceiver and a class-E power amplifier (PA). The detection and stimulation parameters in the BPSK form and the power of SoC are transmitted from the external control system to the SoC wirelessly. The BPSK data are demodulated by the BPSK demodulator, whereas the power is regulated by the $2\times/3\times$ active rectifier and the low-dropout regulators (LDOs). The seizure detection result and the recorded ECoG in the LSK form are transmitted back from the LSK modulator of SoC to the external control system through the same coil.

III. Circuit Design

The circuit implementation can be divided into four different parts: NSAU, BSP, 16-channel HVTS, and wireless power and data telemetry unit.

A. Neural-Signal Acquisition Unit

As shown in Fig. 2, the 16-channel NSAU consists of 16 input protection circuits, AR-CSCCIAs, PTGAs, a MUX, a TIA, a 10-bit delta-modulated SAR ADC, a ripple reduction loop (RRL) global control, and a clock controller [14], [15]. The ECoG signals sensed from the electrodes through the input protection circuit are amplified by the AR-CSCCIA with 45-dB gain and the PTGA with a programmable gain

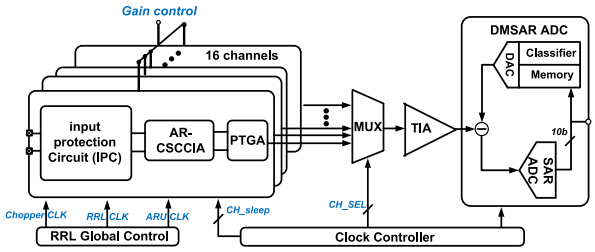

Fig. 2. Structure of the NSAU [14], [15].

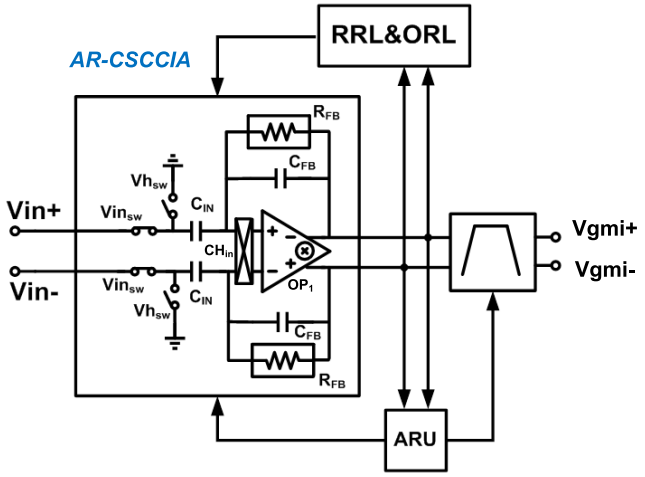

Fig. 3. Architecture of the AR-CSCCIA [14], [15].

of 5/15/25 dB for patient-specific ECoG signal acquisition. The PTGA also converts differential voltage ECoG signals into single-ended current signals for the MUX so that the fast channel selection on current signals can be achieved in the MUX. The TIA is used to convert input current signals into voltage signals and drive the capacitor array of delta-modulated SAR ADC. Since the channel multiplexing frequency is 32 kHz, the TIA output should be settled down before SAR ADC sampling, which means that the maximum settling time is 7.8125 μs. Considering the linearity and dynamic range, the current-based topology is better than the voltage topology. The PTGA is designed by using the source degeneration circuit [15]. Since the signal paths among PTGA, MUX, and TIA are of current signals with low impedance, high slew rate, high dynamic range, high channel selection rate, and short transient time of PTGA can be achieved.

In the proposed closed-loop seizure control system, the NSAU, which senses the ECoG signal, has to share the same electrode with the HVTS, which delivers the constant current stimulation to suppress the seizure onset. During the stimulation, the gate-oxide overstressing caused by the high voltage generated by the HVTS on the MOS devices in the NSAU should be avoided. To prevent this overstressing, an input protection circuit is designed by using high-voltage-tolerant switches and self-adaption bias circuits [14], [15].

Fig. 3 shows the architecture of the AR-CSCCIA, which is composed of an operational amplifier (OP_1), an RRL, an offset reduction loop (ORL), an auto-reset unit (ARU), and a bandpass filter (BPF). To filter out the flicker noise while amplifying the ECoG signal, the chopper modulation

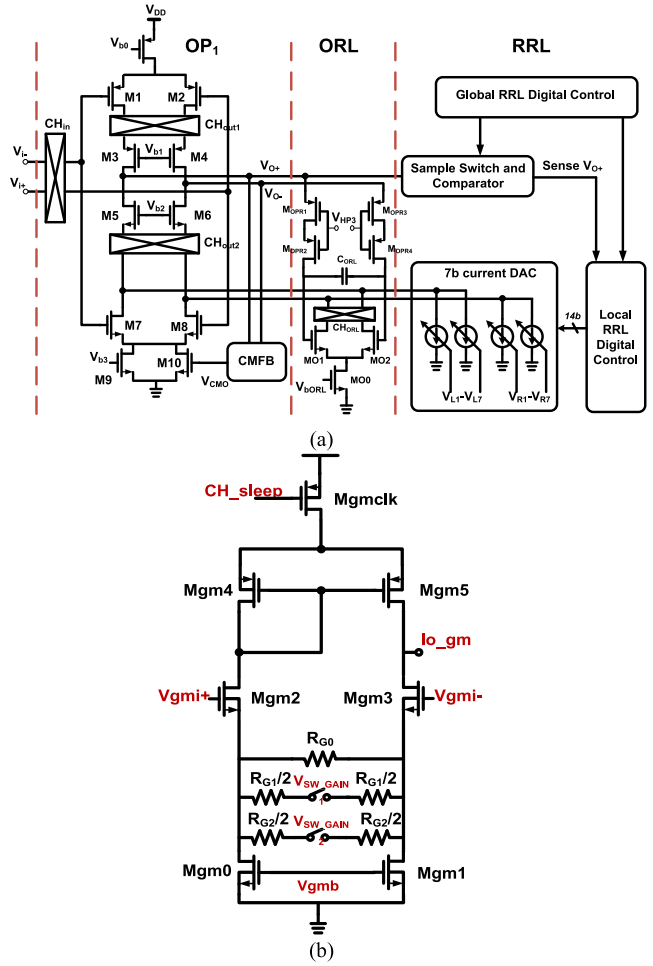

Fig. 4. (a) Schematic of the AR-CSCCIA. (b) Schematic of PTGA [15].

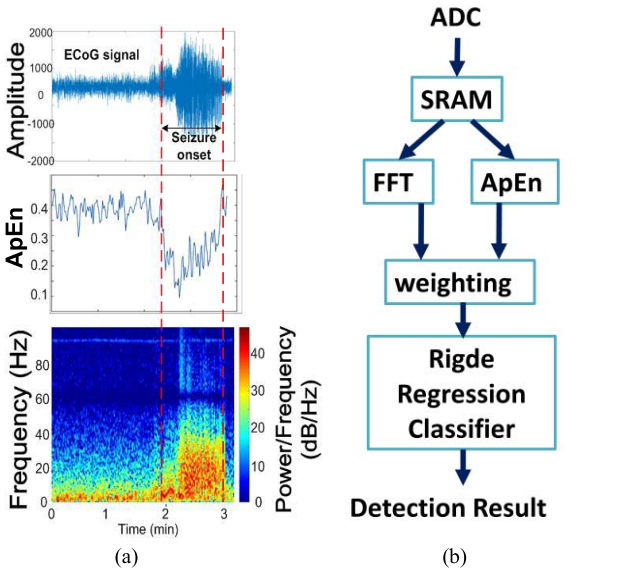

Fig. 5. (a) ApEn and spectrum features in seizure onset waveforms of human. (b) Seizure detection algorithm.

technique [18] is used. The input modulator CH_{in} is placed after the input capacitors C_{IN} to achieve high input impedance and good electrode dc offset rejection capability. Since the signal is demodulated back to the baseband before reaching the output, the output dominate pole and the bandwidth (BW) of OP_1 can be designed as small as that of the amplifier without chopper modulation.

Fig. 4(a) shows the schematic of AR-CSCCIA [14], [15]. The inverter-based cascode OP amplifier OP_1 uses both PMOS and NMOS transistors as input pairs to form the inverter-based cascode structure and achieve a better noise-efficiency factor (NEF). The RRL and the ORL are designed to reduce the chopper-induced artifacts of chopper ripple and input-referred offset, respectively [15]. Without the ORL, the offset of AR-CSCCIS caused by the mismatches of input chopper switches and parasitic capacitors at the virtual ground nodes of OP_1 would be amplified by chopper modulation. Then, the output offset voltage might cause the undesired gain degradation and dc operating point shift of the PTGA. Because of the stimulation artifacts and interfaces, the AR-CSCCIA may be saturated and recovered slowly. To improve this situation, an ARU is added in the AR-CSCCIA by comparing the output voltage of the AR-CSCCIA with the preset voltages. Once the output voltage exceeds the preset margin, the gate voltage of the pseudoresistors R_{FB} in Fig. 3 is shorted to ground to provide a fast reset path. With the ARU, the stimulation artifact is settled down in 9 ms.

A source degeneration architecture is used in the design of PTGA as given in [15]. The circuit is shown in Fig. 4(b). When the channel is deselected, the power control gate is turned off (CH_sleep = 1.8 V) to save the power dissipation of the deselected PTGA. When the channel is selected and the power control gate is turned on, the transit time is designed to obtain the output with low distortion. Since the interface between the PTGA and the TIA is at low impedance, it can achieve a high slew rate, low transit time, and small output swing. The small output swing benefit to the linearity of the amplifier [19]. Note that the mismatch issue of PTGA and TIA is less significant because the preceding AR-CSCCIA has the high enough gain of 45 dB.

The NSAU provides a three-step gain (50, 60, and 70 dB) for patient-specific signal scaling. The high-pass corner is at 0.59 Hz and the low-pass corner is at 117 Hz. The NEF of AR-CSCCIA is 3.78.

B. Biosignal Processor

A complex analysis such as the approximate entropy (ApEn) has proven to work well on distinguishing from electroencephalography (EEG) signals during wakefulness and seizures [20]. The ApEn is a measurement that quantifies both regularity and predictability over time-series data. The time-series signals containing many repetitive patterns have a relatively smaller ApEn. Conversely, the less predictable process has a higher ApEn. Because of the fact that the periodic signal components of seizures reduce the complexity levels and the ApEn significantly; the ApEn is utilized to analyze the complexity of ECoG signals. Fig. 5(a) shows the ApEn value versus the time. It can be seen from Fig. 5(a) that during the seizure onset of human, the ApEn value is nearly zero.

However, only the feature of the ApEn value for the seizure detection cannot achieve enough accuracy because artifacts

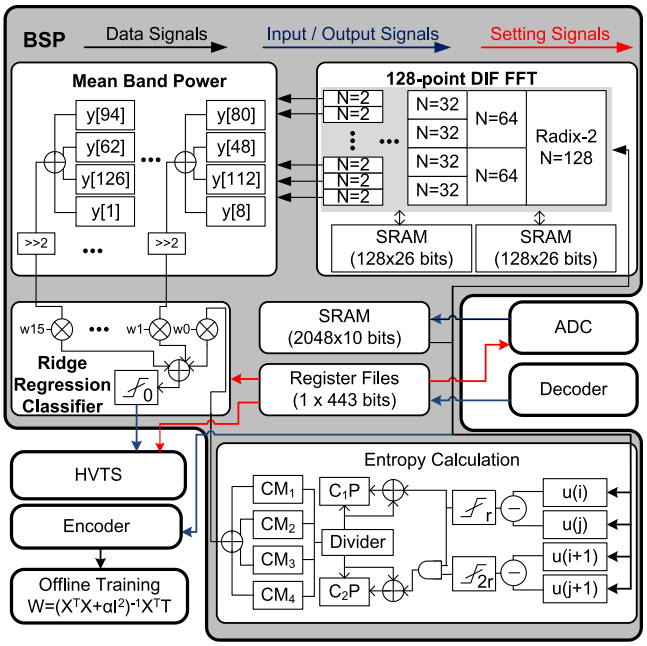

Fig. 6. Hardware implementation of the BSP.

and slow wave sleep waveforms may have lower ApEn values. The ECoG spectral analysis based on short-term Fourier-transform shows that the seizure has a large spectral power in 7–9- and 14–18-Hz bands as observed in the epilepsy experiments of rats [21]. However, the human epilepsy is much more complex than the rat epilepsy. The power spectral density in frequency bands from 4 to 64 Hz shows significant changes during the human epileptic seizure onset. Thus, the average power spectral densities over the 4-Hz intervals are calculated in the 4–64-Hz band as the 15 features. As shown in Fig. 5(a), the band power distribution of 4–64 Hz is obvious during the seizure onset of a human. Thus, the 15 features of average band power spectral density can be extracted. The decimation-in-frequency (DIF) fast Fourier transform (FFT) is used for the hardware implementation to calculate the power of specific frequency bands. In the calculation of the overall feature of power spectral density, the multiple outputs of FFT in the specific frequency bands are multiplied by weighting factors and summed up together.

The seizure detection algorithm is shown in Fig. 5(b) where the extracted features of ApEn and power spectral density from FFT are fed into the ridge regression classifier (RRC). The RRC method finds the best fitting linear model that minimizes the mean square error between the system output and the desired output. Since the output of the linear model is the weighted sum of input features, it is suitable for hardware implementation with reduced computational cost.

Fig. 6 shows the hardware implementation diagram of BSP where the 128-point DIF FFT and mean band power are used to calculate the power spectral density. The entropy calculation is used to calculate the ApEn. The power spectral density and ApEn are then processed by the RRC. The RRC determines the seizure onset channel within 0.36-ms calculation time.

The training of the regression classifier was performed in an offline computer by using the recorded ECoG data of

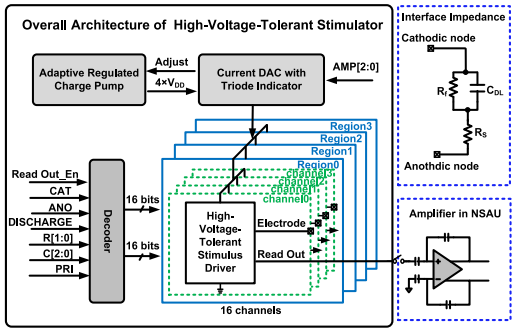

Fig. 7. Architecture of the HVTS [17].

five patients to extract the 16 weights and the threshold of the regression classifier. Then, different recorded ECoG data of the five patients were used in the testing stage. The accuracy, sensitivity, and specificity were obtained through the average of the results from the five patients. The accuracy, sensitivity, and specificity are 97.8%, 96.0%, and 100%, respectively.

C. High-Voltage-Tolerant Stimulator

Fig. 7 shows the architecture of 16-channel HVTS, which consists of a three-stage adaptive regulated charge pump, a current DAC with the triode indicator, a decoder, and the 16-channel high-voltage-tolerant stimulus drivers. The biphasic stimulation current pulses are adjustable from 0.5 to 3 mA. The structures of an adaptive regulated charge pump and a high-voltage-tolerant stimulus driver are shown in Fig. 8. In the adaptive regulated charge pump, the output voltage is proportional to the output clock frequency of the four-phase clock generator. It uses the PFM feedback to generate the regulated output voltage of $4 \times V_{\mathrm{DD}}$. The PFM feedback consists of a four-phase clock generator, voltage-controlled oscillator (VCO), and an error amplifier. By applying a phase-shift clock control scheme, the control clock of each charge pump stage has a phase shift different from each other. This can decrease the peak current from supply and enhance the transient response of the wireless power telemetry.

To integrate with other circuits in the SoC and decrease the mask cost, the HVTS is implemented in the 180-nm low-voltage process. The problems of gate-oxide overstressing, hot-carrier effect, and other reliability issues should be considered [22]. The high-voltage-tolerant stimulus driver is designed to solve both reliability and safety issues.

As shown in Fig. 8, the transistors M_{B1}–M_{B6} act as a self-adaption bias circuit to keep the voltages across each MOS device in the stacked structures within 3.3 V under $4 \times V_{\mathrm{DD}}$ (12-V) power supply. The output of the regulated charge pump is driven by the "adjust" signal. A triode indicator is used to control the regulated charge pump that provides an adaptive power supply at the $4 \times V_{\mathrm{DD}}$ node to ensure M_{C3} and M_{C4} operated in the saturation region during constant current stimulation. Since the voltage on the double-layer capacitor of the electrode is increased gradually during constant current stimulation, the voltage drop across the transistors M_{C3} and M_{C4} becomes less than 0.8 V. Once the cascode transistors (M_{C3} and M_{C4}) are out of the saturation region, the triode indicator generates an "adjust" signal to the

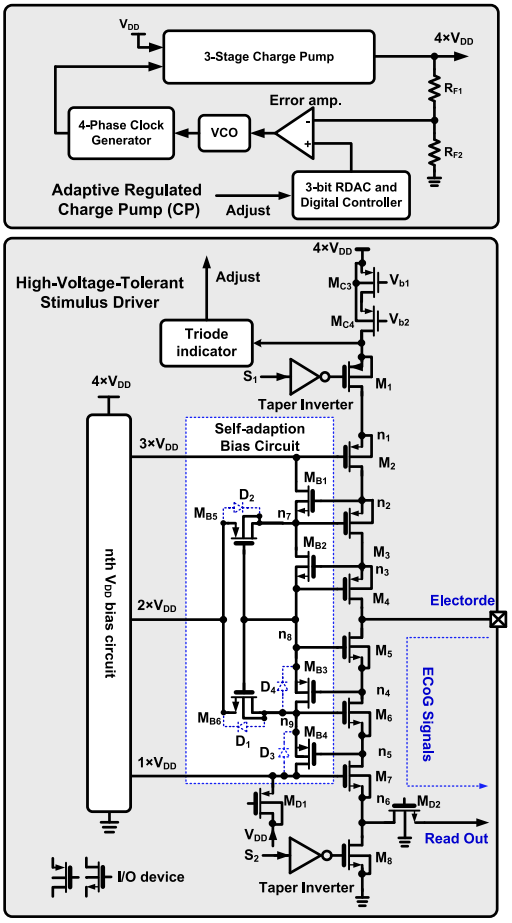

Fig. 8. Structures of an adaptive regulated charge pump and a high-voltage-tolerant stimulus driver [17].

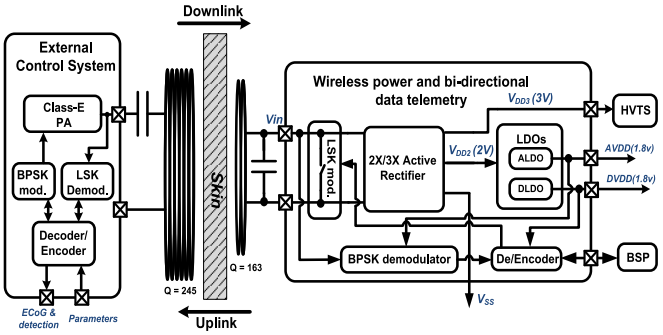

Fig. 9. Architecture of wireless power and bidirectional data telemetry.

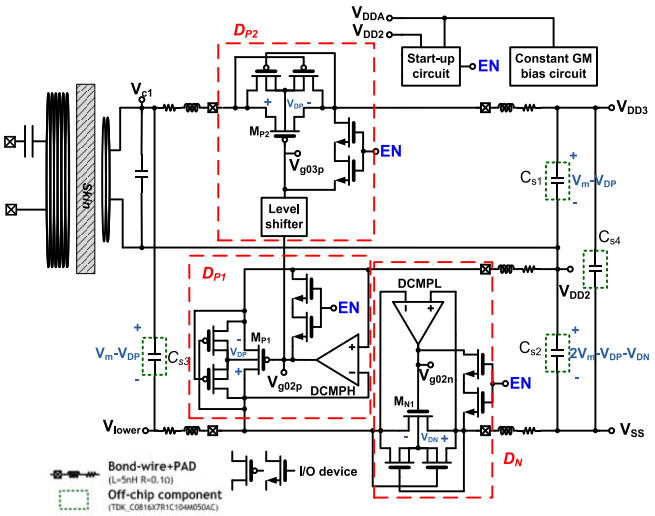

Fig. 10. Circuit structure of 2×/3× active rectifier.

regulated charge pump, which increases the supply voltage at 0.5-V steps promptly to keep both M_{C3} and M_{C4} in saturation and maintain a constant stimulation current.

D. Wireless Power and Bidirectional Data Telemetry

It is important for the implanted SoC to have a maximum power efficiency to reduce the power dissipation and keep the device temperature variation below 2 °C [23]. Due to the maximum 3-mA stimulation current, about 90% of power dissipates on the HVTS during the stimulation period. In order to get the highest power efficiency, minimizing the number of charge pump stages of the HVTS can increase the power efficiency because the higher number of charge pump stages leads to the lower efficiency. Therefore, a new architecture of active rectifier that can provide both 2- and 3-V output voltages is adopted [13]. By using 3 V as the input, the number of charge pump stages can be effectively reduced and its power efficiency can be increased.

Fig. 9 shows the architecture of wireless power and bidirectional data telemetry that consists of a 2×/3× active rectifier, two LDOs, a BPSK demodulator, an LSK modulator, and a de/encoder. The received ac signal in the secondary coil is regulated by the 2×/3× active rectifier with delay compensation. The regulated 2 V is connected to analog low-dropout regulator (ALDO) and digital low-dropout regulator for the analog and digital power supply, respectively. The regulated 3 V provides the input voltage of HVTS.

The circuit structure of the 2×/3× active rectifier is shown in Fig. 10, which consists of a start-up circuit, an NMOS active diode, two PMOS active diodes, two delay-compensated comparators (delay-compensated comparator high-side (DCMPH) and delay-compensated comparator low-side) with delay compensation control, a level shifter, and off-chip filtering capacitors.

To explain the operation of the 2×/3× active rectifier, three diodes D_{P1}, D_{P2}, and D_N are used to represent MOS active diodes as shown in Fig. 10. The forward dropout voltage of diode D_N ($D_{P1,P2}$) is $V_{\rm DN}$ ($V_{\rm DP}$). The sinusoidal input voltage of the secondary coil has a peak input amplitude of V_m. When $V_{\rm lower} > V_{\rm DP} + V_{\rm DD2}$, the diode D_{P2} turns on and the current flows from V_{C1} to $V_{\rm DD3}$ to charge the capacitor C_{S1} to $V_m - V_{\rm DP}$. At the same time, the diode D_{P1} turns on and charges the capacitor C_{S3} to $V_m - V_{\rm DP}$. The diodes turn on until V_{C1} decreases below $V_{\rm DD3} + V_{\rm DP}$. When $V_{\rm SS} > [V_{C1} - (V_m - V_{\rm DP})] + V_{\rm DN}$, the diode D_N turns on and starts to charge the capacitor C_{S2} to $2V_m - V_{\rm DP} - V_{\rm DN}$. It stops charging until $V_{\rm SS} < [V_{C1} - (V_m - V_{\rm DP})] + V_{\rm DN}$. Finally, the output voltages are $2V_m - V_{\rm DP} - V_{\rm DN}$ at the node $V_{\rm DD2}$ and $3V_m - 2V_{\rm DP} - V_{\rm DN}$ at the node $V_{\rm DD3}$. Thus, the functions of 2×/3× output voltages can be achieved.

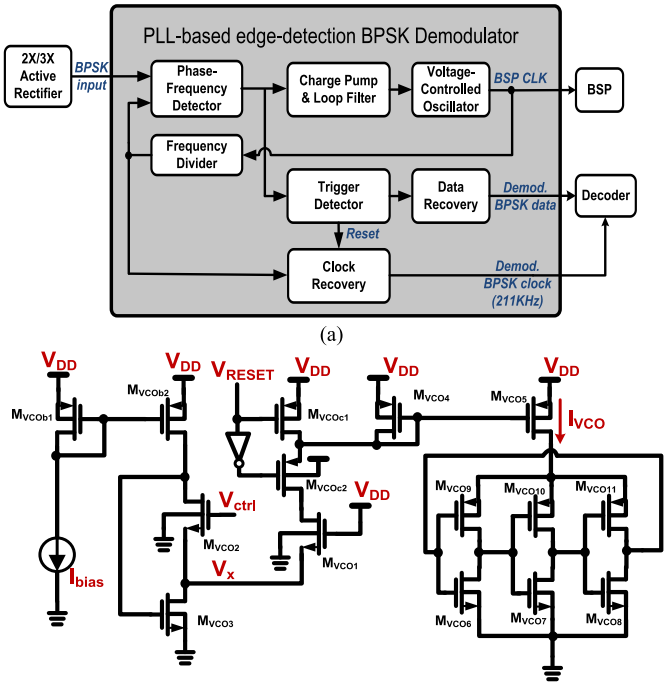

Fig. 11. (a) Block diagram of PLL-based edge-detection BPSK demodulator. (b) Schematic of the VCO in the proposed PLL-based edge-detection BPSK demodulator.

In Fig. 10, the voltage level of the output voltage V_{g02p} of DCMPH is from 0 V to V_{DD2} (2 V). Since the I/O device can handle 3.3 V in the 0.18-μm CMOS technology, a simple level shifter can be designed by using I/O devices to convert the voltage level from V_{DD2} to V_{DD3} (3 V) without device overstress issue. It converts the voltage level and enhances the driving ability to drive the large input capacitance of power transistor M_{P2}.

To minimize the device size for implantation, only one pair of coils for both wireless power and bidirectional data telemetry is adopted in the proposed implanted SoC. The high-Q coils are used to achieve a high wireless PCE since the energy can be stored at the specific frequency of 13.56 MHz. The inductances and Q values of TX and RX coils are significantly increased by the permeability of the ferrite core. Thus, the efficiency can also be increased. The resonant inductive link with ferrite core achieves 76.3% power transfer efficiency as reported in [24].

Since the pair of coils has high-Q values of 245 in primary and 163 in secondary, the data channel capacity is decreased. Therefore, the uplink and downlink data rates are designed to 106 and 211 Kb/s, respectively. When a downlink BPSK data transition occurs, the secondary coil requires a few cycles to invert its phase. Under this situation, the edge of the BPSK signal is not significant and the conventional edge-detection BPSK demodulators [25], [26] cannot be applied. Thus, the phase-locked loop (PLL)-based edge-detection BPSK demodulator is proposed [13] as shown in Fig. 11(a), where a PLL is used to lock the carrier frequency. The source switching topology [27] is used in the charge pump to guarantee a lower charge sharing when the switch is turned on. The loop-BW of PLL is designed at 900 KHz to optimize phase noise performance. In Fig. 11(a), the phase frequency detector can sense the phase change and generate phase difference signals when the data change. A trigger detector is designed to detect the output of the phase frequency detector and generate a trigger signal when the phase difference signals exceed a preset threshold. The data recovery is composed of a D flip-flop which inverts the current data when a trigger signal is generated. The output of data recovery is sent to the decoder. The clock recovery is composed of a divided-by-64 frequency divider. The input of the clock recovery is the carrier signal (13.56 MHz) and its output generates a clock frequency of 211 KHz. Due to the change of carrier frequency during the data transition, the clock recovery requires a reset signal, which is the trigger signal from the trigger detector, to prevent non-synchronization of data and clock.

Fig. 11(b) shows the schematic of VCO in the proposed PLL-based edge-detection BPSK demodulator. M_{VCO6}–M_{VCO11} are the inverter chain for oscillating. To eliminate the process-variation-induced frequency shift which causes the trigger detector failed to detect the data edges, a current control unit composed of M_{VCO1}–M_{VCO3} is designed to convert the input control voltage V_{ctrl} to the current I_{VCO} supplied to the VCO to control its output frequency. When the control voltage V_{ctrl} is fed from the loop filter, V_x in Fig. 11(b) can be written as

$$V_X = V_{ctrl} - V_{th} - \sqrt{\frac{2I_{bias}}{\beta_{MVCO2}}} \tag{1}$$

where I_{bias} is the constant bias current of the VCO, $\beta_{MVCO2} = \mu Cox(W/L)$, and μ, Cox, W, L, and V_{th} are the mobility, gate capacitance density, width, length, and threshold voltage of the MOS device M_{VCO2}, respectively. Since the bias current I_{bias} is a constant value, V_x is linearly proportional to V_{ctrl}. Thus, the current I_{VCO} fed to the inverter chain can be expressed as

$$I_{VCO} = \frac{1}{2}\beta_{MVCO1}\left(V_{DD} - V_{ctrl} + \sqrt{\left(\frac{2I_{bias}}{\beta_{MVCO2}}\right)}\right)^2. \tag{2}$$

It can be seen from (2) that the current is not sensitive to V_{th} which can reduce the process variations. The trancon-ductance G_m and the VCO gain K_{VCO} of the VCO can be expressed as

$$G_m = \beta_{MVCO1}\left(V_{DD} - V_{ctrl} + \sqrt{\frac{2I_{bias}}{\beta_{MVCO2}}}\right) \tag{3}$$

$$K_{VCO} = \frac{G_m}{2NC_{out}V_{sw}} \tag{4}$$

where N is the stage number of the inverter chain, C_{out} is the output capacitance of each stage in the inverter chain, and V_{sw} is the output signal swing of VCO. It can be seen from (3) and (4) that G_m and K_{VCO} are not affected by the variations of V_{th}.

The LSK modulation is adopted to transmit the recorded ECoG signals and the seizure detection results as the uplink data to the external control system for monitoring purposes. The data are transmitted by changing the loading of the

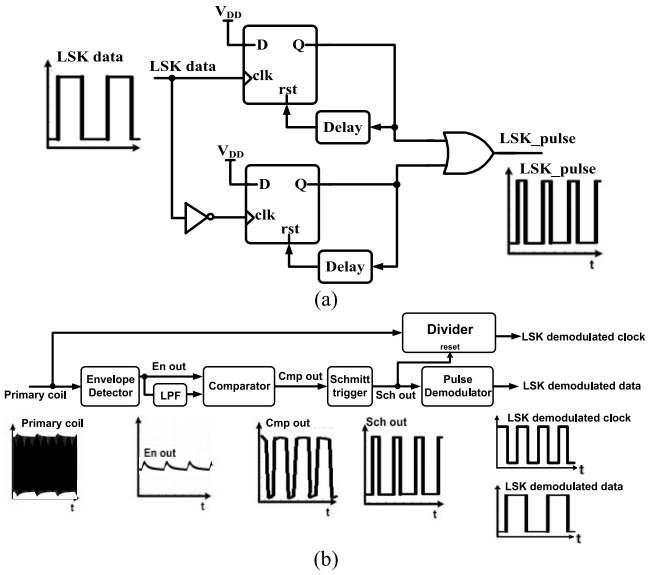

Fig. 12. Block diagram of (a) LSK modulator and (b) LSK demodulator.

secondary coil, which causes the amplitude change on the primary coil [28]. Since the loading change of secondary coil by the LSK modulator decreases the wireless power transfer efficiency, the pulse modulation is used in this design to maintain high wireless PCE when the LSK data are transmitted [29]. Fig. 12(a) shows the block diagram of the LSK modulator which consists of two D flip-flops and an OR gate. The LSK modulator sends a short pulse only when the LSK data change. Fig. 12(b) shows the block diagram of the LSK demodulator which consists of an envelope detector, a low-pass filter (LPF), a comparator, a Schmitt trigger, and a pulse demodulator. The envelope of the signal on the primary coil is detected by the envelope detector. The comparator compares the output of the envelope detector with its dc level extracted by the LPF to amplify the output of the envelope detector. Then, the pulse demodulator is used to demodulate the uplink data for the external control system. To synchronize the transmitted uplink data in receiver end at the bit level, the divided-by-128 divider is used to divide the primary coil signal at 13.56 MHz and generate a clock at 106 KHz for LSK demodulation. To eliminate the frequency drift due to the amplitude changes of the primary coil signal caused by LSK data transmission, the reset signal of a divider is connected to the output of the Schmitt trigger to maintain the LSK data synchronization.

IV. Experimental Results

The proposed closed-loop seizure control SoC and the chip of an external control system were designed and fabricated in the 0.18-μm CMOS technology. The chip of the external chip (implanted SoC) occupies 12.26 mm^2 (25 mm^2) including the electrostatic discharge pads as shown in Fig. 13. Each circuit was tested separately and the function of the whole system was verified in both electrical and animal tests.

A. Electrical Tests

The measured input-referred noise $V_{n,\mathrm{rms}}$ of the fabricated AR-CSCCIA is shown in Fig. 14. The inputs of AR-CSCCIA

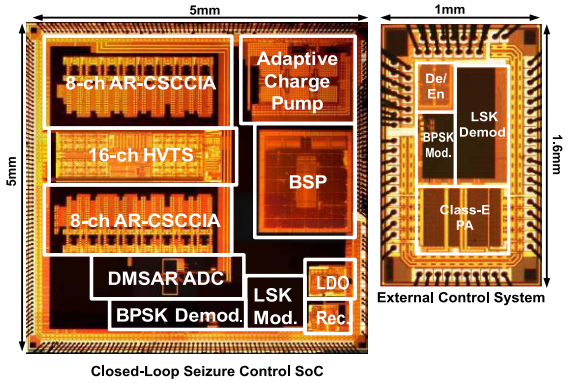

Fig. 13. Chip micrographs of the proposed closed-loop seizure control SoC and the external control system.

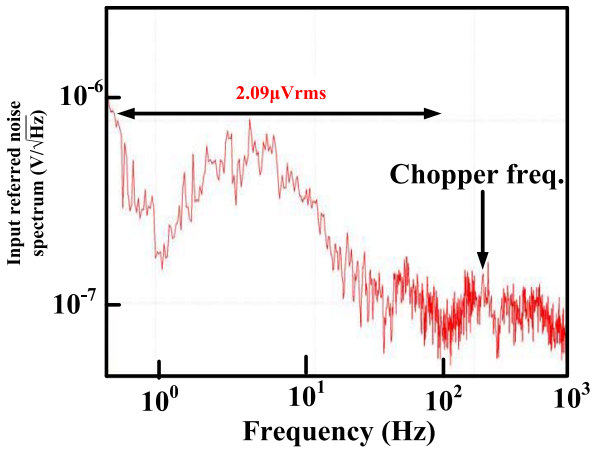

Fig. 14. Measured input-referred noise of the fabricated AR-CSCCIA.

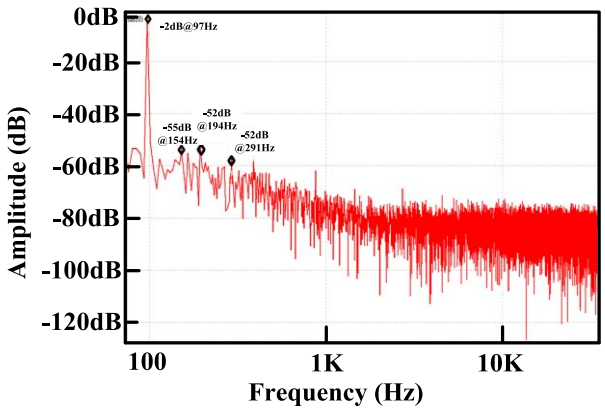

Fig. 15. Measured spectrum analysis of the fabricated NSAU.

are grounded, while the output is analyzed by a dynamic signal analyzer. The measured output noise is divided by the gain of AR-CSCCIA (45 dB) to obtain the input-referred noise. With the chopper modulation, the input-referred noise of AR-CSCCIA is only 2.09 μV_{rms} integrated into the BW of 0.5–117 Hz when the SoC is wirelessly powered. The NEF of the NSAU is 3.78. The measured spurious-free dynamic range (SFDR) of the fabricated NSAU is 50 dB, as shown in Fig. 15. The measured SNDR is 48.7 dB and the effective number of bits (ENOB) of the SoC is 7.8 bit.

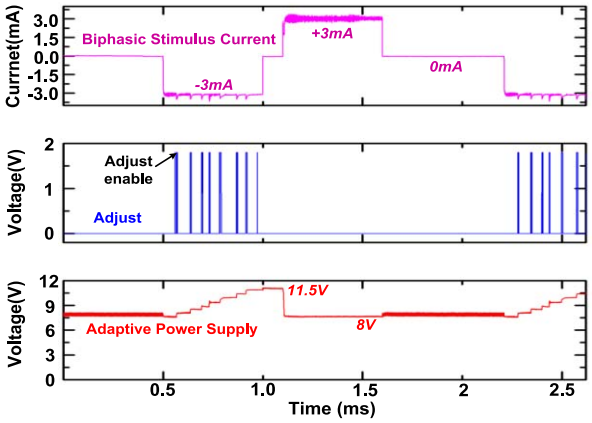

Fig. 16. Measurement results of the fabricated HVTS with adaptive supply voltage control.

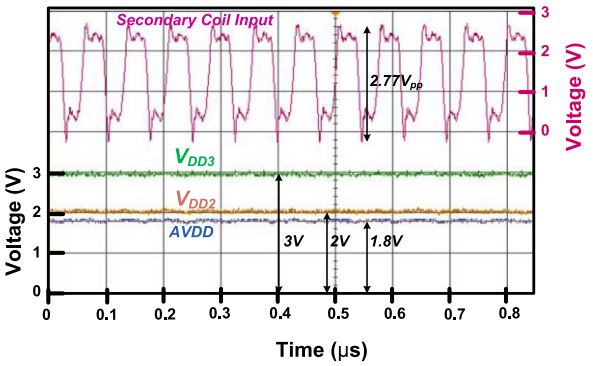

Fig. 17. Measurement results of the fabricated 2×/3× active rectifier and LDOs.

Fig. 16 shows the measured biphasic stimulus current at 3 mA and the corresponding measured adaptive power supply voltage with the measured "adjust" signal of the fabricated HVTS as shown in Figs. 7 and 8. It can be seen from Fig. 16 that the adaptive power supply can be pumped and stepped up from 8 to 11.5 V following the "adjust" signal generated by the triode indicator. Since the voltage on the double-layer capacitor of the electrode is increased gradually during constant current stimulation, using the adaptive power supply can decrease the conduction loss of the high-voltage-tolerant stimulus driver and increase the power efficiency of HVTS to 54% from the original 37% with a fixed $4 \times V_{DD}$ of 12 V, both under the stimulus current of 3 mA. The overshoot current is about 0.2 mA, which is within the safe stimulation range.

Fig. 17 shows the measured secondary coil input waveforms, rectifier output voltages V_{DD3} and V_{DD2}, and the output voltage AVDD of the fabricated 2×/3× active rectifier and ALDO, as shown in Figs. 9 and 10. It can be seen from Fig. 17 that 3 V (V_{DD3}) and 2 V (V_{DD2}) can be generated by the active rectifier, whereas 1.8 V (AVDD) can be generated by the ALDO to provide a stable supply voltage for the analog circuits of SoC. The measured PCE of 2×/3× active rectifier is 80.8% and the measured ripples of V_{DD3}, V_{DD2}, and AVDD are 50.4, 40.2, and 39.2 mV_{pp}, respectively.

For the data transmission, the downlink data in BPSK form as demodulated by the proposed PLL-based edge-detection

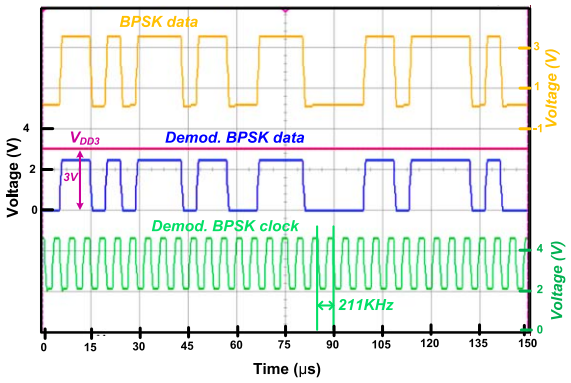

Fig. 18. Measurement results of the fabricated PLL-based edge-detection BPSK demodulator.

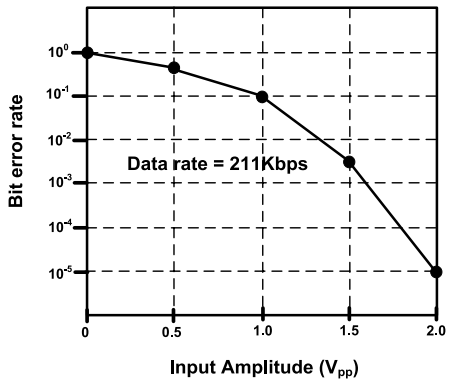

Fig. 19. Measured bit error rate of the fabricated PLL-based edge-detection BPSK demodulator.

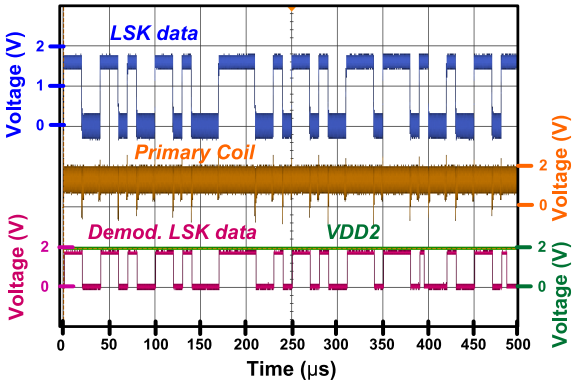

Fig. 20. Measurement results of demodulated data from the fabricated LSK demodulator and the voltage waveforms on the primary coil.

BPSK demodulator are shown in Fig. 18 where the generated 3 V by the 2×/3× active rectifier is also shown. This verifies the capability of simultaneous downlink data and power transmission. The measured PCE of the 2×/3× active rectifier during BPSK data transmission is 76.7% at 1 cm distance. When the input amplitude of the 2×/3× active rectifier is 2 V, the measured bit error rate of the fabricated PLL-based edge-detection BPSK demodulator is 10^{-5}, as shown in Fig. 19.

The measured uplink data in LSK form as demodulated by the proposed LSK demodulator are shown in Fig. 20. The uplink data rate is 106 Kb/s and the measured bit error rate is 10^{-4}. Since the neural signal in the uplink data is below 100 Hz, the bit error rate of 10^{-4} under 106 Kb/s is acceptable according to [30]. When the LSK data change,

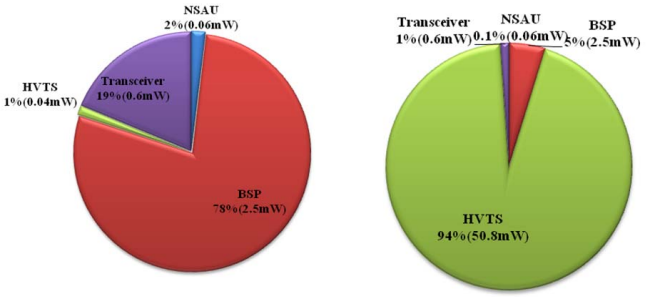

Fig. 21. Measured power dissipation pie chart of the seizure control SoC. (a) Seizure control SoC operated in standby mode. (b) Seizure control SoC operated in stimulation mode.

TABLE I

PERFORMANCE SUMMARY OF THE PROPOSED CLOSED-LOOP SEIZURE CONTROL SOC

	JSSC'14 [4]	JSSC'16 [5]	JSSC'17 [6]	This Work
Process	TSMC 0.18μm	IBM 0.13μm	IBM 0.13μm	TSMC 0.18μm
# of channels	8	64	64	16
Input referred noise (μV_{rms}) (Bandwidth)	5.23 (0.1-7KHz)	4.2 (1-5KHz)	1.13 (0.01-500Hz)	2.09 (0.59-117Hz)
NEF	1.77	6.9	2.86	3.78
Accuracy	92%	88-96%	75% (sensitivity)	97.76%
Latency	0.8s	n.a	n.a	0.76s
BSP Efficiency	77.91μJ/ (feature ext. + classification)	n.a	n.a	62.5μJ/ (feature ext. + classification)
Charge pump stage (PCE)	5 (38%)	No	No	3 (54%)
Stimulation current	30μA biphasic	10-1000μA biphasic	10-1350μA biphasic	500-3000μA biphasic
Adaptive stimulation control	Yes	No	No	Yes
Power dissipation	2.8mW (standby)	2.17mW (UWB) 5.8mW (FSK)	1.07mW (delay-based UWB) 5.44mW (VCO-based UWB)	3.12mW (standby) 54mW (stimulation)
Wireless transmission (carrier frequency)	Dual-band (13.56M, 400MHz)	Quad-band (1.5M, 916.4M, <1G, 3.1-10G)	Dual-band (1.5M, 3.1-10G)	Single-band (13.56MHz)
Downlink data rate (energy per bit)	4Mbps (0.07 nJ/b)	n.a	n.a	211Kbps (1.027 nJ/b)
Uplink data rate (energy per bit)	1Mbps (0.16 nJ/b)	1.2Mbps (3.08 nJ/b) 10Mbps (0.01 nJ/b) 10Mbps (2.22 pJ/b)	10Mbps (0.01 nJ/b) 46Mbps (0.08 pJ/b)	105Kbps (0.14 nJ/b)
Power transfer efficiency	~8.3% (Overall) * 84.8% (Only rectifier)	40% (overall)	n.a	48% (overall)

* Using external buffer as power transmitter

the amplitude on the primary coil increases and the proposed LSK demodulator can demodulate the LSK data. The PCE during LSK data transmission is 63.8%. The energy-per-bit of BPSK demodulator and LSK modulator are 1.027 and 0.14 nJ/b with 211 and 106 Kb/s, respectively.

The total power consumption of the proposed SoC is 3.12 mW in the standby mode and 54 mW in the stimulation mode. The pie charts of power dissipation in these two modes are shown in Fig. 21.

The performance summary of the proposed SoC is given in Table I where comparisons with that of [4]–[6] are also listed.

In the neural recording system [4]–[6], the low-frequency flicker noise is dominant. When the amplifier BW is increased, the low-frequency noise has a lower contribution to the total input-referred noise. Since the signal BW of [4] is designed

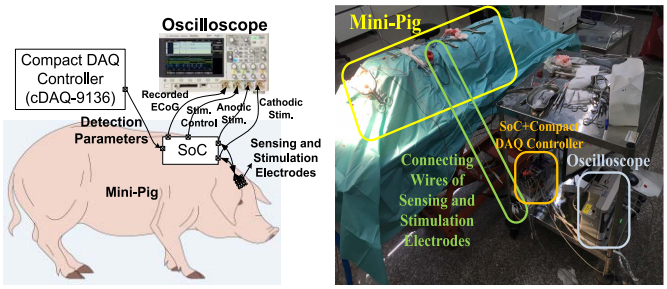

Fig. 22. (a) Animal measurement setup of the SoC with a compact DAQ controller on a mini-pig and (b) its real picture.

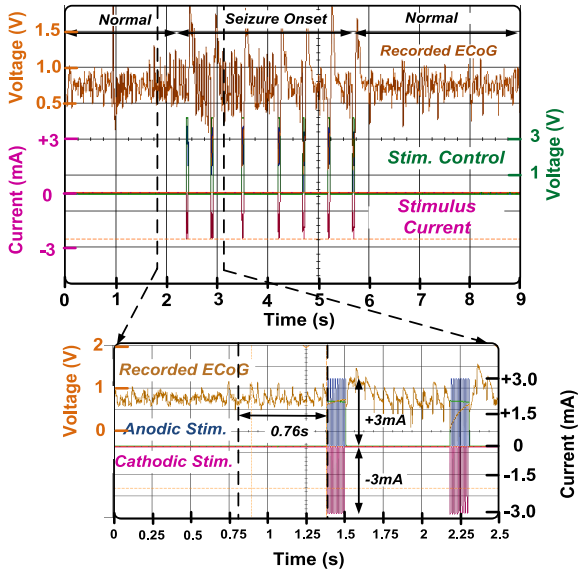

Fig. 23. Measurement results of an animal experiment.

from 0.1 Hz to 7 KHz which is larger than that in this paper, the NEF of [4] is lower. It can be seen from the comparison that the proposed SoC achieves the highest detection accuracy, programmable stimulation currents, and overall PCE calculated from the input of primary coil to the output of the 2×/3× active rectifier under the maximum average loading currents of 3 mA (2×) and 16 mA (3×), while only one pair of coils is used for wireless power and bidirectional data telemetry.

B. Animal Test

The function of the fabricated closed-loop seizure control SoC in the 0.18-μm CMOS technology was verified with the *in vivo* animal tests of mini-pigs. Fig. 22(a) shows the animal measurement setup of the SoC with a compact DAQ controller on a mini-pig, where the mini-pig was implanted with 16-channel planar electrodes on the cortical surface. The seizure onset of mini-pigs was induced by injecting penicillin. The SoC was parameterized by a compact DAQ controller through an input pad. The recorded ECoG by the NSAU, the stimulation control signal by the BSP, and anodic and cathodic simulation current waveforms by the HVTS were connected to the oscilloscope through output pads. The real picture of mini-pig measurement setup is shown in Fig. 22(b). Fig. 23 shows the waveforms of recorded ECoG,

the stimulation control signal, and the generated stimulus currents. It can be seen that the seizure onset is detected and the stimulus current of 3 mA is delivered to the electrode within 0.76 s. After the stimulation, the seizures are suppressed and the measured ECoG is recovered to the normal state. The closed-loop function of the proposed closed-loop seizure control SoC is verified successfully.

V. Conclusion

The 16-channel closed-loop neuromodulation SoC for human epileptic seizure control is designed and fabricated. In the SoC, a 16-channel NSAU, a BSP, a 16-channel HVTS, and a wireless power and bidirectional data telemetry are integrated. Through *in vivo* animal tests in mini-pigs, the closed-loop function of SoC has been verified successfully. The measured seizure detection latency is 0.76 s with the accuracy of 97.8%. Up to 3-mA biphasic current stimulation can be delivered through electrodes to suppress the epileptic seizures. The closed-loop seizure control SoC has been demonstrated to be a feasible solution for treating human epilepsy.

Acknowledgment

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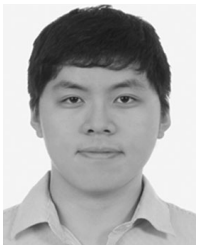

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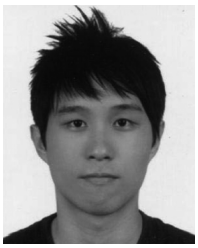

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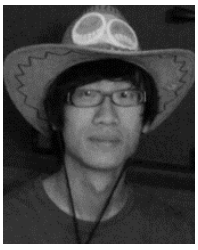

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