On-Chip HBM and HMM ESD Protection Design for RF Applications in 40-nm CMOS Process

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***Abstract*— On-chip electrostatic discharge (ESD) protection device with large dimension can sustain high-ESD current, but the parasitic capacitance of the ESD protection device will increase the difficulty of impedance matching and degrade the bandwidth for broadband radio frequency (RF) applications. The traditional distributed ESD protection circuit can achieve good impedance matching, but it has a worse ESD robustness because of larger resistance caused by the input inductor. In this paper, a new distributed ESD protection structure with the stacked diodes with embedded silicon-controlled rectifier is proposed to attain good ESD robustness without degrading the RF performance. The proposed ESD protection circuit has been successfully verified in a 40-nm, 2.5-V CMOS process to sustain a human-metal model of 5 kV. The proposed ESD protection circuit is suitable to protect the broadband RF circuits in advanced nanoscale CMOS technology.**

***Index Terms*— Distributed electrostatic discharge (ESD) protection, ESD, radio frequency (RF), silicon-controlled rectifier (SCR).**

I. Introduction

With the development of CMOS technology, improving the high-frequency characteristics and quality of reliability in radio frequency (RF) ICs has been the ultimate goal of the IC industry [1]. The electrostatic discharge (ESD) protection ability has become one of the important concerns on the reliability of IC products. Unfortunately, devices in nanoscale CMOS technology are very sensitive to ESD events due to the lower gate oxide breakdown and junction breakdown voltages [2], [3], but the commercial IC products still need to pass the required ESD specification, such as 1 kV in the human-body model (HBM) [4], [5] or more. For the RF IC applications, the major concern of ESD protection design is the parasitic effect of the ESD protection circuit. It will strongly degrade the bandwidth in normal RF operation [6]. Therefore, the ESD protection circuit should be designed to achieve the desired RF performance as well as sustain good ESD robustness.

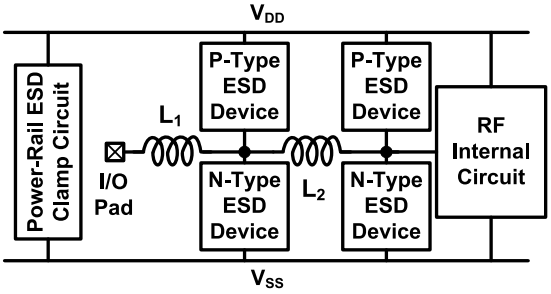

Fig. 1. Traditional distributed ESD protection circuit with ESD devices in two stages for RF applications [6]–[8].

Several ESD protection designs have been reported to improve the impedance matching and to achieve the requested ESD robustness for RF circuits [7], [8]. Fig. 1 shows a traditional distributed ESD protection circuit, which is composed of two inductors (L_1 and L_2) and two stages of ESD protection devices [9]–[11]. However, some characteristics of this structure during ESD stress condition should be further optimized for RF applications. First, the inductor (L_1) connected to I/O pad will cause a higher turn-ON resistance and clamp voltage during the ESD stress condition, even though this structure has a good broadband RF performance. Second, the metal width of the inductor (L_1) should be widened to enhance the current handling capability. It will enlarge the footprint in the layout. Third, the ESD protection device of the diode has a higher parasitic capacitance [12], [13], which will result in a weaker ESD protection ability than silicon-controlled rectifier (SCR) under the same value of parasitic capacitance. Consequently, a modified scheme of the distributed network to further optimize ESD protection ability and RF performance is needed.

Recently, a new test method, human-metal model (HMM) [14], using the system-level ESD gun to directly zap the I/O ports of the stand-alone devices or circuit module is adopted by some industrial companies. Compared with the HBM, the system-level ESD gun has a higher storage capacitor and a lower discharge resistor. It creates more than 5× ESD peak current that can cause serious damage to the I/O pins [15]–[18]. Therefore, the HMM test method will

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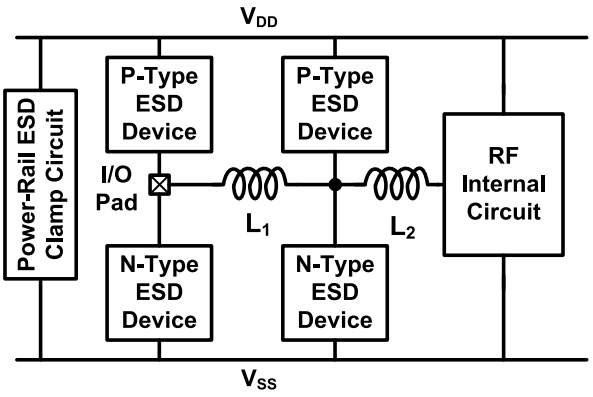

Fig. 2. New proposed distributed ESD protection circuit with ESD devices in two stages for RF applications.

increase the difficulty of on-chip ESD protection design for RF applications.

The purpose of this paper is to investigate the characteristic of the distributed structure during a high-ESD current condition. A new ESD protection circuit with the stacked diodes with embedded SCR (SDSCR) [19]–[21] for RF applications is proposed and fabricated in 40-nm 2.5-V CMOS process. The ESD protection devices of the first stage are put under the I/O pad to reduce layout area and can discharge the ESD current immediately. In detail, the specifications in this paper of input return loss (S_{11}) and insertion loss (S_{21}) are -9 and -3 dB, respectively, during the operating frequency from 0.1 to 10 GHz. In addition to the traditional ESD test method, this paper performed the HMM test method on the test circuits. As compared with the traditional distributed ESD protection circuit, this newly proposed protection circuit has achieved lower turn-ON resistance, good ESD robustness, and required RF performance. It is more desirable than the traditional distributed ESD protection circuit under high-ESD current stress.

II. New Distributed ESD Protection Design

A. Circuits Implementation

In the traditional distributed ESD protection circuit, the inductors have been utilized to compensate the effect of the parasitic capacitances generated by ESD protection devices. Following this concept, the new proposed distributed ESD protection circuit that consists of two inductors (L_1 and L_2) and two stages of ESD protection devices is presented in Fig. 2. Inductors L_1 and L_2 are used to match the input impedance. Furthermore, L_2 that has small size can limit the ESD current to avoid gate oxide damage to the internal circuit. In ESD protection devices, several studies have noted that SDSCR has good ESD robustness and low-parasitic effect [19]–[21]. Accordingly, the proposed circuit has replaced the ESD protection diode with the p-type SDSCR and the n-type SDSCR. Considering the HMM issue, the ESD protection devices are designed to be under the I/O pad. Thus, it can quickly conduct the ESD current to the protection devices by via. In addition,

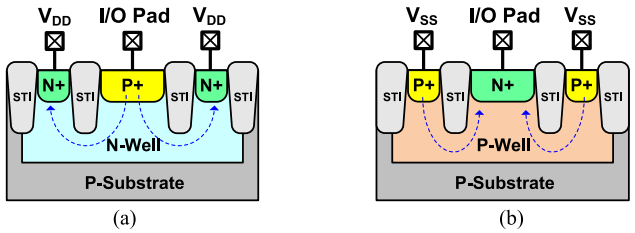

Fig. 3. Device cross-sectional view of (a) p+/n-well diode and (b) n+/p-well diode.

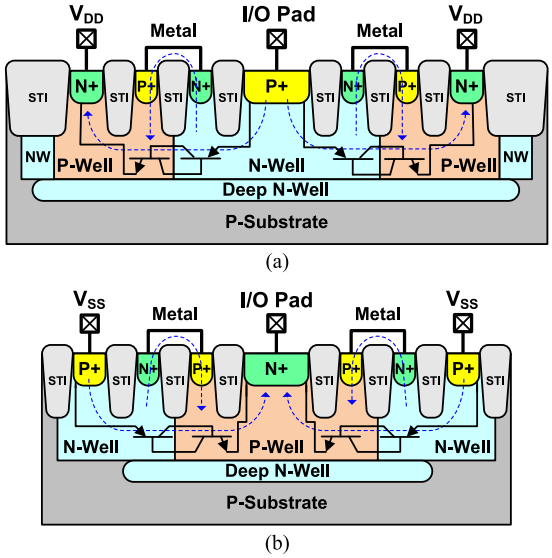

Fig. 4. Device cross-sectional views of (a) p-type SDSCR and (b) n-type SDSCR.

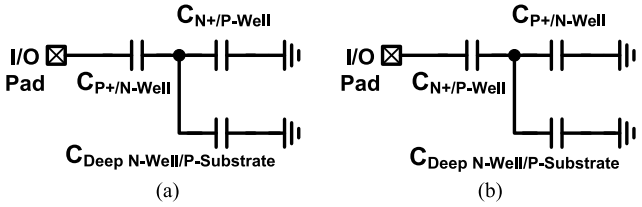

Fig. 5. Simplified model of (a) p-type SDSCR and (b) n-type SDSCR.

this design can also reduce the turn-ON resistance of the ESD protection device to get better ESD protection ability.

To investigate the influence of the ESD protection device on the traditional and the proposed distributed ESD protection circuit, the ESD protection devices in each design are realized with two types of devices, traditional diode and SDSCR. The traditional p+/n-well diode, n+/p-well diode, p-type SDSCR, and n-type SDSCR are shown in Figs. 3 and 4. The equivalent circuit of SCR is made up of a p-n-p bipolar junction transistor (BJT) and an n-p-n BJT. The layout is drawn in stripe style, and the width is selected as 30 μm per finger. The layout area of p+/n-well is equal to that of n+/p-well in each ESD device layout. The simplified model of SDSCR that consists of the junction capacitances is shown in Fig. 5, where the junction capacitance of p-well/n-well is neglected because of the short circuit by metal. The capacitance of the diode seen on the I/O pad is about 1.4× as large as that of the SDSCR. Estimated by

TABLE I
DESIGN PARAMETERS OF THE ESD PROTECTION CIRCUITS

Design parameters	Traditional distributed ESD protection circuit	Proposed distributed ESD protection circuit
C_{Pad} (fF)	100	100
C_{ESD1} (fF)	240	240
C_{ESD2} (fF)	240	360
L_1 (pH)	360	700
L_2 (pH)	360	170

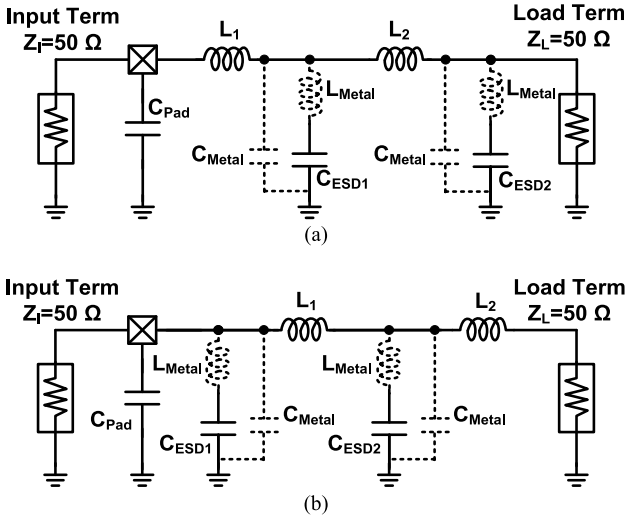

Fig. 6. Equivalent RF circuit models of (a) traditional distributed ESD protection circuit in two stages and (b) new proposed distributed ESD protection circuit in two stages.

the foundry's data, the parasitic capacitance of the diode and the SDSCR is about 30 and 20 fF, respectively, in each finger with a width of 30 μm. According to the previous report [22], the capacitance of the first stage ESD protection device (C_{ESD1}) is assumed to be 240 fF, which is sufficient to achieve the HMM ESD test level of 4 kV. To meet the first stage capacitance of 240 fF, the number of fingers for the diode and SDSCR is designed as four and six, respectively. In other words, the total width of the diode and SDSCR is 120 μm (30 μm × 4 fingers) and 180 μm (30 μm × 6 fingers), respectively.

B. Circuits Simulation

Starting with a standard 50-Ω system, which is commonly found in RF systems, the equivalent RF circuit models of these two different ESD protection circuits are shown in Fig. 6(a) and (b). A signal source with 50-Ω impedance (Z_I) drives the input node of the ESD protection circuits, and a 50-Ω output load (Z_L) is connected to the output node of ESD protection circuits. Each ESD protection device is modeled as capacitances (C_{ESDx}). All the design parameters for simulation are listed in Table I. The capacitance of pad is 100 fF from the foundry's data. Moreover, the layout effect of metal routing is

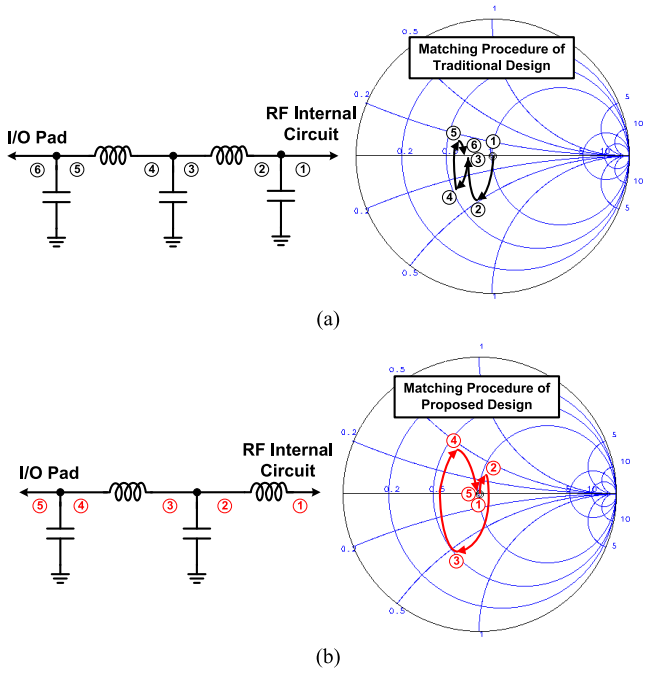

Fig. 7. Matching procedures of (a) traditional distributed ESD protection circuit and (b) new proposed distributed ESD protection circuit in Smith chart.

extracted by an electromagnetic simulation tool to modify the simulated RF characteristics.

In order to meet the desired specifications of S_{11} and S_{21}, the way by using the inductor to compensate the parasitic capacitances has been adopted in this paper. Following the matching step shown in Fig. 7(a), the compensated inductors (L_1 and L_2) in the traditional distributed ESD protection circuit are both selected as 360 pH because the capacitance of the second stage (C_{ESD2}+C_{Metal}) is the same as that of the first stage (C_{ESD1}+C_{Metal}). In the proposed circuit, the capacitance value of the first stage is contributed by C_{Pad}, C_{ESD1}, and C_{Metal}. This capacitance value is fixed in the matching step to meet good ESD specification. By adding the inductors of L_1 and L_2, the matching procedure is modified as that shown in Fig. 7(b). To meet the center point of 50-Ω output load in Smith chart, the inductors L_1 and L_2, which can limit the ESD current and compensate the parasitic capacitances, are selected as 700 and 170 pH, respectively. In addition, the capacitance value of the second stage (C_{ESD2}) is selected as 360 fF. Fig. 8 shows the S-parameter simulation results with layout effect in the frequency range of 0.1–10 GHz. The return loss and insertion loss of the traditional circuit and the proposed circuit can both achieve the desired specifications.

III. EXPERIMENTAL RESULTS OF ESD TEST CELLS

In order to reduce the parasitic capacitance, the top metal (metal7 in the given process) is used for the routing to I/O pad, and the bottom metal is used for the routing to V_{DD} and V_{SS} pads. Each inductor is composed of two metal layers (top metal and aluminum). To sustain high-ESD current, the width of inductor's metal is selected as 12 μm, which is the maximum value of the top metal in this process. The width

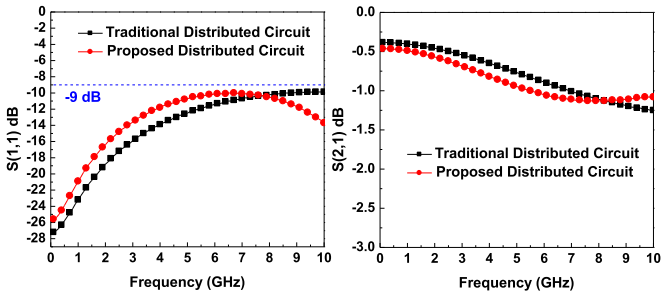

Fig. 8. Simulation results with layout effect on the RF performance of (a) S_{11}-parameters and (b) S_{21}-parameters for the traditional circuit and the proposed circuit.

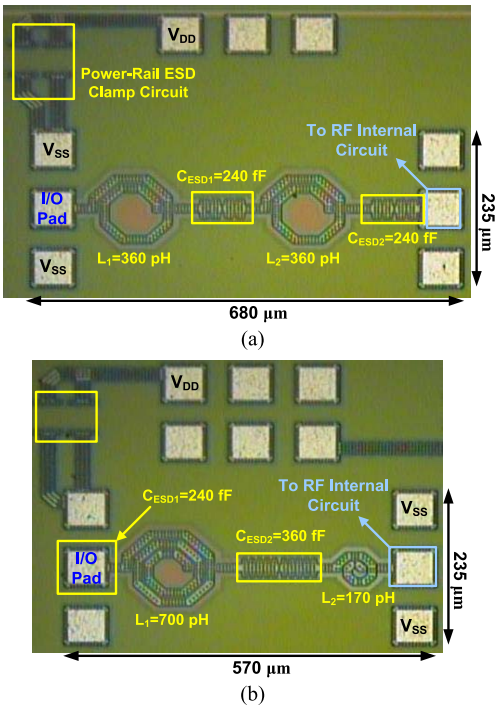

Fig. 9. Chip micrographs of (a) traditional circuit and (b) proposed circuit.

of other metal layers (metal1 to metal6) is also limited in advanced process. In addition, a special layout skill of stacking multiple metal layers has been proposed in this paper to follow the foundry's design rule, without degrading the ESD robustness. Each ESD protection device utilizes four layers of metal (metal2 to metal5) for the metal routing to sustain high-ESD current. Fig. 9 shows the chip micrographs of the traditional circuits and the proposed circuits.

A. RF Performances

With the on-wafer and two-port S-parameter measurements, the RF characteristics of test circuits have been extracted. The voltage supply of V_{DD} is 2.5 V, and the input dc bias is 1.0 V. The source and load resistances to the fabricated ESD protection circuits are kept at 50 Ω. Fig. 10(a) and (b) shows the measured S_{11}- and S_{21}-parameters versus frequencies among the test circuits. During the operating frequency from 0.1 to 10 GHz, the maximum values of S_{11} in traditional circuit

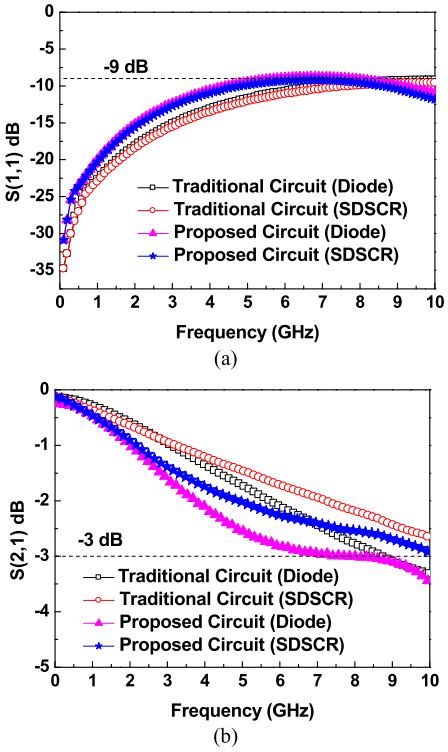

Fig. 10. Measurement results of (a) S_{11}-parameters and (b) S_{21}-parameters for the traditional and proposed circuits.

with the diodes and the SDSCRs are −9.2 and −9.6 dB, respectively. The maximum values of S_{11} in the proposed circuit with the diodes and the SDSCRs are −8.8 and −9.2 dB, respectively. The circuit with the traditional diode has a larger insertion loss than the one with the SDSCR, as predicted in the simulation results. In addition, the experimental results have a little difference with the simulation results. The reason is that the front-end parasitic effect is roughly estimated by using the junction and sidewall capacitances from the foundry's data. Moreover, the ESD device under the I/O pad has a large overlap area between back-end metal and front-end device, and it may cause some unpredictable parasitic effect that was not considered in the simulation results.

B. ESD Robustness

The HBM test method is typically used to verify the ESD robustness of the fabricated circuits. The ESD pulses are stressed to each test circuit under positive I/O-to-V_{DD} (PD mode), positive I/O-to-V_{SS} (PS mode), negative I/O-to-V_{DD} (ND mode), and negative I/O-to-V_{SS} (NS mode) ESD stress conditions. All the test circuit can sustain more than 8-kV HBM ESD level under each test condition. Furthermore, this paper also shows the HMM test method on the test circuits to investigate the robustness under ESD gun stress. The failure criterion is defined as the I–V characteristics of the circuit shifting more than 30% from its initial curve after ESD gun zapped at each ESD test level. The HBM and HMM test results of the test circuits under four modes of ESD test condition are summarized in Tables II and III. The ESD robustness of the test circuit is judged by the lowest level among the four modes

TABLE II
MEASURED RESULTS OF THE TRADITIONAL DISTRIBUTED ESD PROTECTION CIRCUITS

	Traditional distributed ESD protection circuit with the diodes				Traditional distributed ESD protection circuit with the SDSCRs			
First stage ESD device size (μm)	P+/N-Well Diode=120 N+/P-Well Diode=120				P-type SDSCR=180 N-Type SDSCR=180			
Second stage ESD device size (μm)	P+/N-Well Diode=120 N+/P-Well Diode=120				P-type SDSCR=180 N-type SDSCR=180			
Area (mm^2)	0.1598				0.1598			
L (pH)	L_1=360, L_2=360				L_1=360, L_2=360			
Mode	PD	PS	ND	NS	PD	PS	ND	NS
V_{t1} (V)	0.86	1.0	1.04	0.86	1.0	1.7	1.8	1.6
I_{t2} (A)	9.3	8.5	7.4	10	9.4	8.3	6.9	10
HBM (kV)	>8	>8	>8	>8	>8	>8	>8	>8
HMM (kV)	4.5	4	3.5	5	4.5	4	3.5	5
FOM (kV/dB* mm^2)	8.5	7.6	6.6	9.5	10.8	9.6	8.4	12
S-parameter (dB)	S_{11}= -9.2, S_{21}= -3.3 (from 0.1 to 10 GHz)				S_{11}= -9.6, S_{21}= -2.6 (from 0.1 to 10 GHz)			

TABLE III
MEASURED RESULTS OF THE PROPOSED DISTRIBUTED ESD PROTECTION CIRCUITS

	Proposed distributed ESD protection circuit with the diodes				Proposed distributed ESD protection circuit with the SDSCRs			
First stage ESD device size (μm)	P+/N-Well Diode=120 N+/P-Well Diode=120				P-Type SDSCR=180 N-Type SDSCR=180			
Second stage ESD device size (μm)	P+/N-Well Diode=180 N+/P-Well Diode=180				P-Type SDSCR=270 N-Type SDSCR=270			
Area (mm^2)	0.13395				0.13395			
L (pH)	L_1=700, L_2=170				L_1=700, L_2=170			
Mode	PD	PS	ND	NS	PD	PS	ND	NS
V_{t1} (V)	0.85	1.0	1.02	0.85	1.0	1.8	1.8	1.6
I_{t2} (A)	11.9	9.0	9.0	10.9	13.5	9.6	9.7	12.8
HBM (kV)	>8	>8	>8	>8	>8	>8	>8	>8
HMM (kV)	6	4.5	4.5	5.5	7	5	5	6.5
FOM (kV/dB* mm^2)	13.2	9.9	9.9	12.1	18.7	13.3	13.3	17.3
S-parameter (dB)	S_{11}= -8.8, S_{21}= -3.4 (from 0.1 to 10 GHz)				S_{11}= -9.2, S_{21}= -2.8 (from 0.1 to 10 GHz)			

of ESD test condition. Therefore, the HMM ESD robustness of the traditional circuit with diodes, the traditional circuit with SDSCRs, the proposed circuit with diodes, and the proposed circuit with SDSCRs is 3.5, 3.5, 4.5, and 5 kV, respectively.

C. Transmission-Line-Pulsing I–V Characteristics

A 100-ns transmission-line-pulsing (TLP) system with 10-ns rise time was used to investigate the circuit behavior during an ESD transient pulse [23]. The important parameters of TLP measurement I–V curve include trigger voltage (V_{t1}), holding voltage (V_h), and second breakdown current (I_{t2}). In order to analyze the performance of p-type and n-type devices, the comparisons of TLP I–V curves among all test circuits under PD and NS mode ESD test conditions are shown in Fig. 11. I_{t2} of the proposed circuit with SDSCRs is on the top, and the proposed circuit with diodes is the second. It is due to the small size of the diode under the same value of the parasitic capacitance, as compared with SCR. In Fig. 11, the holding voltage of traditional circuits is higher than that of the proposed circuits. It can be attributed to the inherent resistance of the input inductor. The input inductor also degrades the ESD robustness of traditional circuits. Since the failure point of traditional circuits was located on the input inductor rather than the ESD device, the leakage current has no significant difference after the TLP test. The optical micrographs will be shown in Section III-D. All the measurement results are listed in Tables II and III.

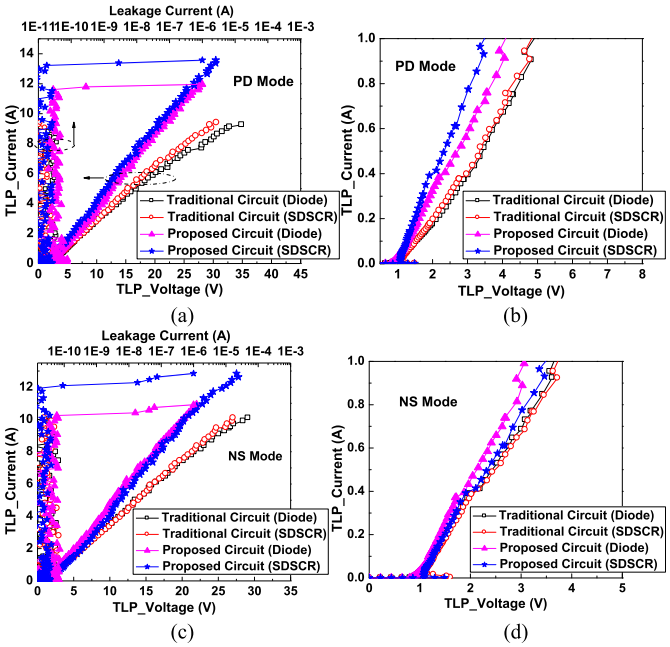

Fig. 11. TLP measured I–V characteristics of (a) PD mode, (b) zoomed-in view illustration of PD mode, (c) NS mode, and (d) zoomed-in view illustration of NS mode among the traditional circuits and the proposed circuits.

D. VF-TLP and Transient Overshoot Measurement

A very fast TLP (VF-TLP) system with pulsewidth of 5 ns and rising time of 200 ps is used to verify the performance of the ESD protection circuits during the charge-device

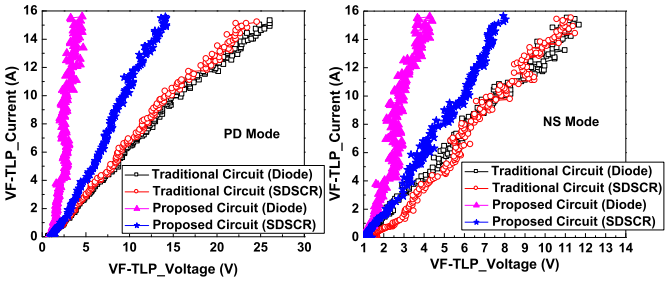

Fig. 12. VF-TLP measured *I–V* characteristics of (a) PD and (b) NS mode among the traditional circuits and the proposed circuits.

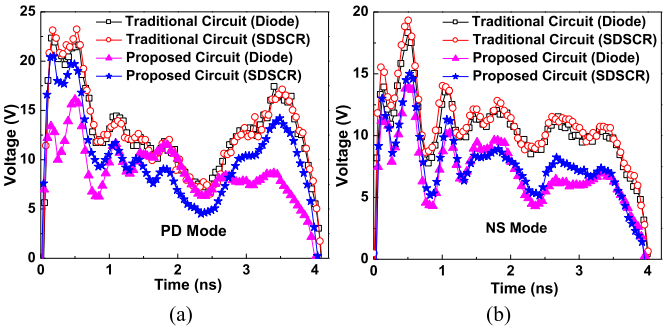

Fig. 13. VF-TLP transient voltage waveform of (a) PD and (b) NS mode among the traditional circuits and the proposed circuits under 5-A condition.

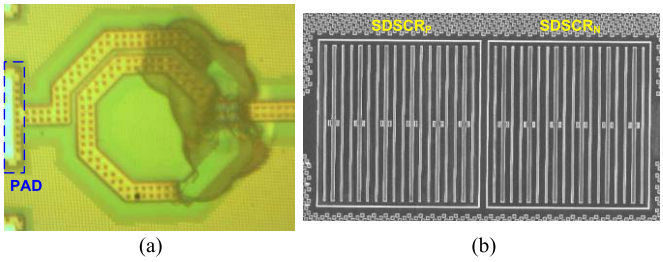

Fig. 14. (a) OM photograph and (b) SEM photograph of traditional circuits after 4.5-kV PS mode HMM stress.

model (CDM) ESD events. Fig. 12 shows the comparison of the VF-TLP *I–V* curves among all the test circuits under PD and NS mode ESD test conditions. As shown in Fig. 13, the transient voltage waveforms among the traditional circuits and the proposed circuits are measured under the 5-A VF-I_{t2} condition. Based on the measurement results, test circuits can overcome the zapping voltage of 900 V, which is a maximum pulse voltage supplied from the VF-TLP instrument. Moreover, the overshoot of the proposed circuits is lower than that of traditional circuits. The proposed circuit can provide more effective protection for the internal circuits against CDM events.

E. Failure Analysis

Fig. 14(a) shows the optical microscope (OM) photograph of traditional circuits after PS mode HMM ESD test of 4.5 kV. Despite using the maximum width of metal, the failure of traditional circuits is still located at the input inductor. The traditional circuits have the same phenomenon under each mode of HMM ESD test. The scanning electron microscope (SEM) experiment was used to further observe the certain failure point. The failure point of the traditional circuits was not found in Fig. 14(b). It means that the ESD level of the traditional circuits is dominated by the metal width of the input inductor. The OM photograph of the proposed circuits after PS mode HMM ESD test of 5.5 kV is shown in Fig. 15(a). The proposed circuit is intact under the microscope. In Fig. 15(b), the failure point of the proposed circuit is located at the p-type SDSCR of the first stage. The ESD robustness of the proposed circuit is significantly dependent on the size of the ESD protection device at the first stage. To conclude, the traditional distributed ESD protection circuit has a risk of metal damage as well as losing the protection ability during the high-current ESD test.

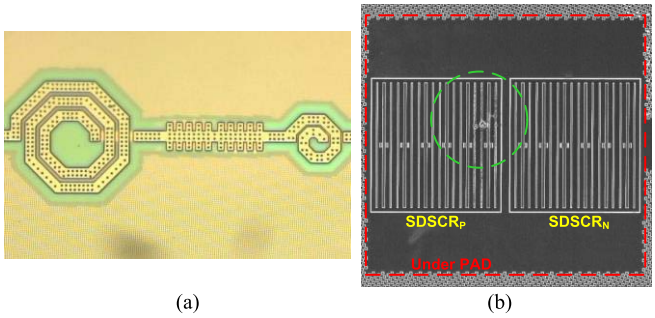

Fig. 15. (a) OM photograph and (b) SEM photograph of the proposed circuits after 5.5-kV PS mode HMM stress

F. Comparison

The important factors of ESD protection circuits for high-frequency applications include S-parameter and ESD robustness. The ESD protection circuits are wished to have required insertion loss under the normal circuit operating conditions, and high-ESD robustness during the ESD current discharging conditions. Obviously, the HBM level of each test circuit is all higher than 8 kV. It cannot use to verify the performance of test circuits. Therefore, the figure of merit (FOM) in this paper can be expressed as

$$\text{FOM} = \frac{\text{HMM}}{|S_{21}| \times A} \tag{1}$$

where A is the cell area of each test circuit. The FOM of the traditional circuit with diodes, the traditional circuit with SDSCRs, the proposed circuit with diodes, and the proposed circuit with SDSCRs is 6.6, 8.4, 9.9, and 13.3 kV/dB·mm^2, respectively. For good ESD protection ability and RF performance, it is desirable to have a high FOM. Unfortunately, the traditional circuits suffered a low-HMM level, and the proposed circuit with diodes has a bad RF performance. Consequently, the proposed circuit with SDSCRs can effectively sustain high-HMM level without degrading RF performance. The proposed circuit was implemented with a cell area of 570×235 μm^2 to save the chip area about 15%, as compared with the traditional circuit. Moreover, the inductor L_2 can be integrated into the internal matching network by using the codesign approach.

IV. Conclusion

For the limitation of back-end metal width in the advanced process, the traditional distributed ESD protection circuit has been demonstrated that it has a risk of metal damage as well as degrading the protection capability. A new distributed ESD protection circuit with the SDSCR for broadband RF applications is proposed in this paper. The ESD protection devices of the proposed circuit are put under the I/O pad to reduce layout area and can discharge the ESD current immediately. As compared with the traditional distributed ESD protection circuit, the experimental results in a 40-nm, 2.5-V CMOS process have successfully verified that the proposed distributed ESD protection circuit with the SDSCRs can effectively sustain the HMM stress of 5 kV without influencing the RF performance. By using the SDSCR, the return loss and insertion loss of the proposed circuit in the frequency range of 0.1–10 GHz are −9.2 and −2.8 dB, respectively. The layout area can efficiently reduce more than 15%. Therefore, the proposed circuit with the SDSCRs provides a good solution for broadband RF applications to sustain a high-ESD robustness.

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