An 82.9%-Efficiency Triple-Output Battery Management Unit for Implantable Neuron Stimulator in 180-nm Standard CMOS

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***Abstract*—This brief presents a high-efficiency battery management unit combining a single-inductor dual-output (SIDO) buck converter with two charge pumps (CPs) to provide three voltage levels (6 V, −6 V, and 2 V) for neuron stimulators in implantable medical devices. The stacked power stage in the buck converter mitigates the voltage stress issue in the power stage to manage 3.2–4.8 V battery voltage. By cascading a buck converter and CPs, the voltage across the CP power stage is reduced to generate 6 V and −6 V high voltage outputs without using high voltage devices. As a result, the proposed battery management could provide 6 V, −6 V, and 2 V output voltages from 3.2 to 4.8 V input voltage using a 180-nm standard CMOS process. The measurement results demonstrate that the proposed battery management achieved a peak efficiency of 82.9% with an available input voltage of 3.2–4.8 V.**

***Index Terms*—High voltage generator, BMU, buck converter, charge pump, overstress, transistors stacking, soft start-up.**

I. Introduction

RECENTLY, to cure neurological disorders, such as Parkinson's disease and epilepsy, implantable medical devices with stimulation function have been employed [1]–[2]. In these devices, implantable stimulators are widely utilized to deliver stimuli as electrical stimulation treatment. According to stimulus patterns, a pair of positive and negative stimulus pulses is defined as biphasic stimulation [3]–[4]. In monopolar architecture, we need both positive and negative voltage sources to generate the appropriate stimuli. To make the stimulator work, a battery management unit (BMU) to provide 2 V for the digital control circuits, and 6 V, −6 V for stimulation in the stimulator. Figure 1(a) shows the architecture of the implantable stimulation system, which includes a battery, a BMU, and an adaptive stimulator.

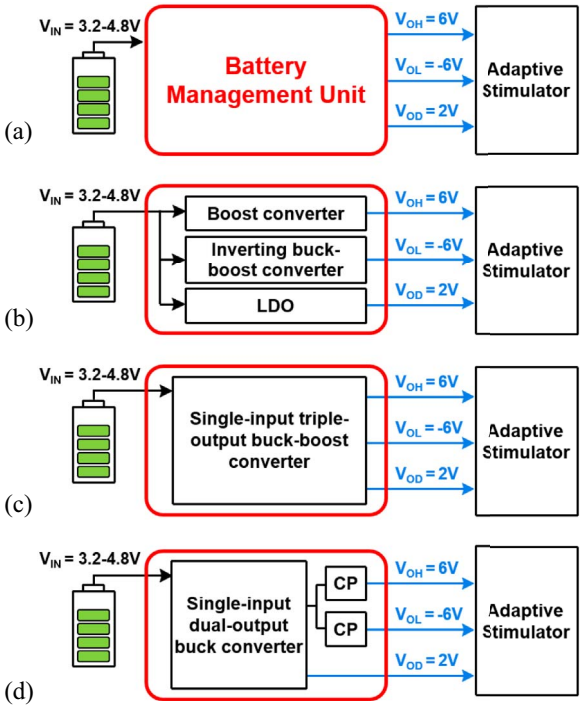

Fig. 1. Architecture of implantable medical device.

The lithium-ion battery is one of the most popular batteries applied in consumer electronics and implantable medical devices [5]. It is rechargeable and has a high energy density and low self-discharge. The battery voltage usually ranges from 3.2 V to 4.8 V. However, in this brief, the 180 nm standard process is chosen to obtain high performance and low power consumption in the digital control of the BMU and stimulator. Therefore, it is important to address the high voltage difference between the high input voltage and negative output voltage using standard 3.3 V I/O devices without any overstress issue.

Fig. 1 shows the possible system architectures of the BMU in implantable medical devices to provide three different DC levels for an adaptive stimulator. Figure 1(b) employs three DC-DC converters: a low dropout regulator (LDO) circuit for 2 V down-converted output, a boost converter for 6 V

Manuscript received February 25, 2019; accepted March 26, 2019. Date of publication April 9, 2019; date of current version April 30, 2019. This work was supported in part by the Ministry of Science and Technology, Taiwan, under Grant 108-2636-E-009-009, Grant 107-2622-8-009-009-TA, and Grant 107-2218-E-009-006, and in part by the "Center for Neuromodulation Medical Electronics Systems" from the Featured Areas Research Center Program within the framework of the Higher Education Sprout Project by the Ministry of Education in Taiwan. This brief was recommended by Associate Editor T. Fernando. *(Corresponding author: Po-Hung Chen.)*

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Digital Object Identifier 10.1109/TCSII.2019.2909813

up-converted positive output, and an inverting buck-boost converter for −6 V negative output. However, there are three main issues in this conventional approach: First, the LDO has a low conversion efficiency due to large voltage differences between the input and output. Second, two off-chip inductors, which are large and costly, are necessary in boost and inverting buck-boost converters. Third, overstress issues occur in all converters due to high output voltages. Figure 1(c) shows the alternative popular approach for multiple output design, which employs a single-inductor triple-output buck-boost converter to provide three different outputs. Compared to the approach in Fig. 1(b), the approach of Fig. 1(c) provides higher converter efficiency to generate 2 V output, which reduces the number of off-chip inductor to one by sharing the inductor. However, the overstress issue still exists, and reliability becomes the key concern.

In this brief, we propose a power management architecture (Fig. 1d) to address the high voltage differences between the input and output. The architecture comprises a single-inductor dual-output (SIDO) buck converter and two CPs, which eliminate the overstress issue caused by output voltages. The SIDO buck converter provides two outputs: a 2 V regulated voltage for the stimulator and the digital control circuits of the power management unit and 3 V semi-regulated internal voltages for the two CPs. The CPs convert the 3 V voltage to 6 V and −6 V using different topologies.

This brief is organized as follows. The system architecture and the design concept of the SIDO buck converter and CPs are presented in Section II. In Section III, the circuit design of function blocks is explained in detail. The measurement results and a comparison with similar systems are discussed in Section IV. Finally, a conclusion is presented in Section V.

II. System Architecture

Fig. 2 shows the block diagram of the proposed BMU system. It consists of a single-input dual-output buck converter, a single-stage positive charge pump (PCP), and a two-stage negative charge pump (NCP).

To avoid the transistor overstress issue in buck converter, a stacking topology is employed to share the voltage across each transistor [6]. The grounded transistor M_{N3} is added to reduce the voltage ringing at switch node V_{LX2}. This helps to clamp the lower bound of V_{LX2} to $-V_D$ to reduce the gate-source voltage across M_{P3} and M_{P4}. For the CP, since the voltage across the transistor is close to the input voltage, the overstress issue can be managed easily with the I/O device in a standard 0.18 μm CMOS process. Therefore, the proposed BMU can provide +6 V, −6 V, and +2 V output voltages without using high voltage process, which may limit the power conversion efficiency.

The buck converter core consists of six power transistors. By appropriately controlling the turn-on frequency of the transistors M_{P3} and M_{P4}, the output voltages V_{OM} and V_{OD} can be well controlled to 2 V and 3 V, respectively. The conversion efficiency of the CP greatly depends on the ratio between input and output voltage. The conversion efficiency is maximum when the CP operates in free-running mode without voltage regulation mechanism. Therefore, the regulation mechanism involves controlling the intermediate voltage V_{OM} to regulate 6 V output, instead of regulating both V_{OM} and 6 V output.

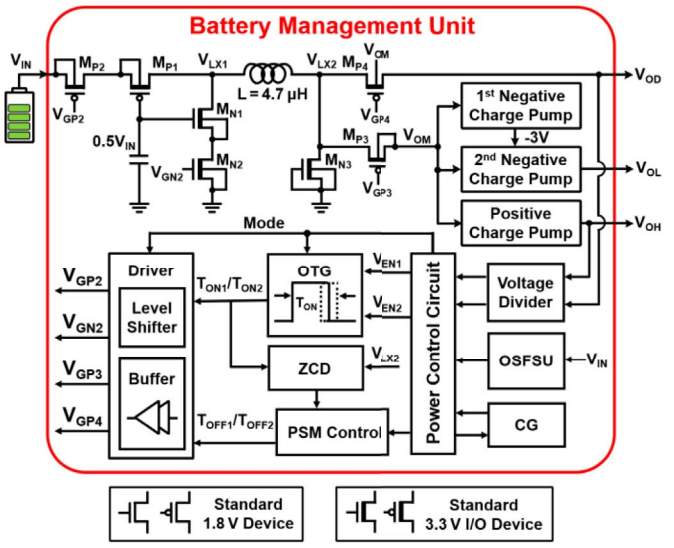

Fig. 2. Circuit diagram of the proposed BMU.

The feedback control circuits include a overstress-free start-up circuit (OSFSU) [7], clock generator (CG), on-time generator (OTG), zero-current detector (ZCD), and pulse-skip modulation (PSM) control. The OSFSU directly charges the output during the start-up period and generates short T_{ON} signals to limit the inductor current in the soft-start period. The CG and BGR provides the system clock frequency and reference voltage of the converter. The OTG and ZCD produce appropriate gate signals according to input and output voltage levels, which ensures the buck converter suffers less power losses under a variable input voltage [8], [9]. The control circuit monitors V_{OD} and V_{OH} by using sequential PSM mechanism [8]. To avoid cross-regulation, the buck converter delivers the power to V_{OD} and V_{OM} by detecting the rising and falling edge of system clock respectively.

III. Circuit Design

Fig. 3 shows the circuit schematic of OSFSU. OSFSU precharges V_{OD} and V_{OM} by using a LDO-like circuit with hysteresis-based control (HBC), which prevents the possible overstress in the battery management control circuit. When the battery is connected to the BMU, the biasing circuit activates and provides the bias current and voltage for the hysteresis comparator and level-shifter. The hysteresis comparator is realized by transistors M_{13} to M_{25}. To avoid the overstress issue, the diode-connected transistors M_{10} to M_{12} are employed to clamp V_{SU1} and V_{SU2} to around 2.4 V and 1.6 V, respectively. V_{SU2} is also the bias voltage of high-voltage (HV) level-shifter, which limits the lower bound of V_{SU3} to ∼2.4 V, to address overstress issue of M_{SUP}. During the beginning of the start-up period, V_{OD} is lower than V_{SU2}. Therefore, V_{SU3} is pulled down to charge output nodes V_{OD} and V_{OM} by the startup transistor M_{SUP}. When V_{OD} is charged to the preset level V_{SU2}, V_{SU3} becomes VIN and turn-off M_{SUP}. To limit the maximum inductor current during startup, the converter adds the soft-start mechanism. The soft-start mechanism

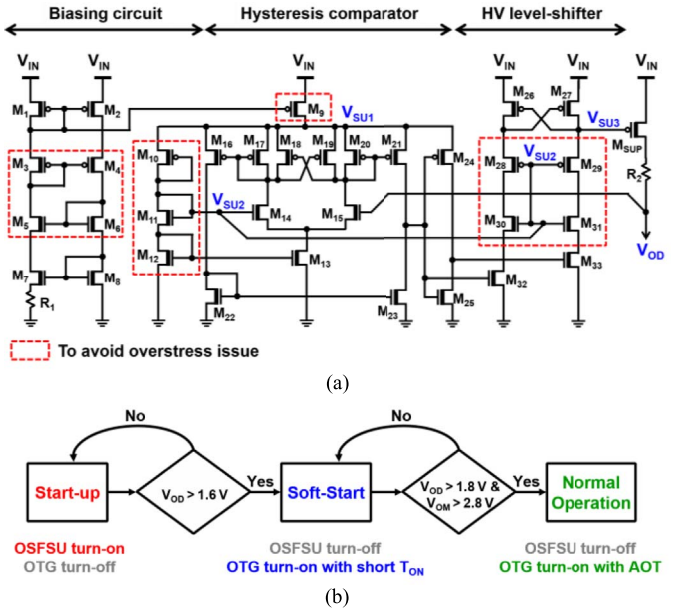

Fig. 3. (a) Circuit schematic of OSFSU (b) finite-state machine of PMU.

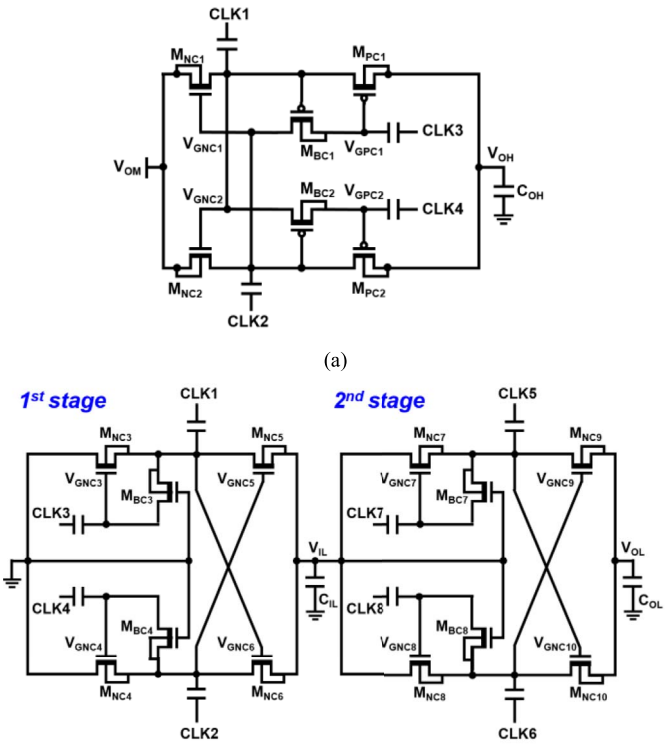

Fig. 4. Circuit schematic of (a) PCP and (b) NCP [13].

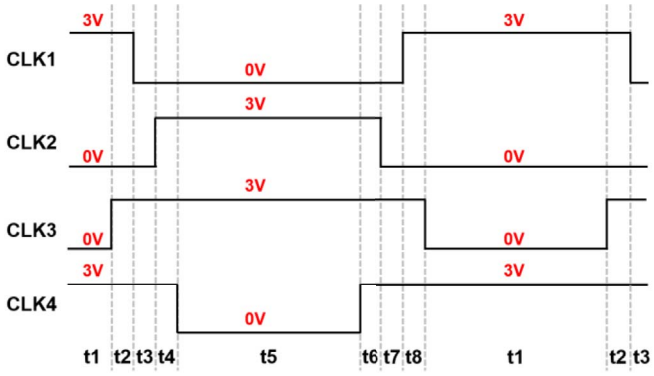

Fig. 5. Waveforms of CLK1 to CLK4.

reduces the on time provided to the power transistors during startup period to use relatively low power to charge output. The OTG provides the correct T_{ON} for high power efficiency and output power level when V_{OD} and V_{OM} become higher than 1.8 V and 2.8 V, respectively.

The circuit schematic of the PCP and NCP are shown in Fig. 4(a) and (b) respectively [13]. The PCP circuit involves two branches, and each branch is composed of two main transistors (M_{PC1}, M_{NC1}, or M_{PC2}, M_{NC2}) and one auxiliary transistor (M_{BC1} or M_{BC2}). The main transistors transfer power from the buck converter, and the auxiliary transistors and the four-phase clock (CLK1 to CLK4) control the appropriate switching of main transistors to suppress the return-back leakage current. The NCP circuit cascade two CP cells. The first stage of NCP use CLK1 to CLK4 to generate V_{IL} which is close to -3 V. The second stage are driven by CLK5 to CLK8 signals which are 90 degree phase shift of CLK1 to CLK4. By interleaving the first and second stages of NCP, we prevent the reverse leakage current from V_{OL} to V_{IL} can be minimized. Fig. 5 illustrates the waveform illustrating the operation.

Fig. 5 illustrates the operation principle of the PCP at different time intervals. During interval t1, the charge is transferred through the main transistor MPC1 and MNC2, and the node voltages V_{GPC2} and V_{GNC2} are two times VOM, while V_{GPC1} and V_{GNC1} equal VOM. To avoid the return-back leakage current, M_{BC1} and M_{PC1} turn off at interval t2 and M_{NC2} turns off at interval t3. In interval t4, MNC1 and M_{PC2} turn on and transfer the power from the storage capacitor to the output capacitor.

IV. Measurement Result

The proposed BMU, which includes the buck converter with OTG and ZCD, a single-stage PCP, a two-stage NCP, the OSFSU, and the CG, was fabricated in a 180 nm standard CMOS process. Fig. 6 shows the chip micrograph with a total chip area of 4.26 mm^2.

Fig. 7 shows the measured waveforms of the proposed BMU during the start-up period, soft-start period, and normal operation period. In the start-up period, V_{OM} and V_{OD} are charged by a start-up MOSFET and increase slowly. In the soft-start period, the buck converter operates with short T_{ON} to ensure that the inductor current (I_L) does not exceed the current limit value. In the normal operation period, the buck converter operates with a suitable T_{ON} and T_{OFF} and regulates two outputs at 2 V and around 3 V. The PCP and NCP start to operate whenever V_{OM} becomes higher than the preset voltage level (2.8 V) and regulate V_{OH} and V_{OL} at $+6$ V and -6 V, respectively.

Fig. 8 shows the measured load transient waveform of V_{OH}, V_{OL}, and V_{OD}at V_{IN} of 3.2 V. The output current of

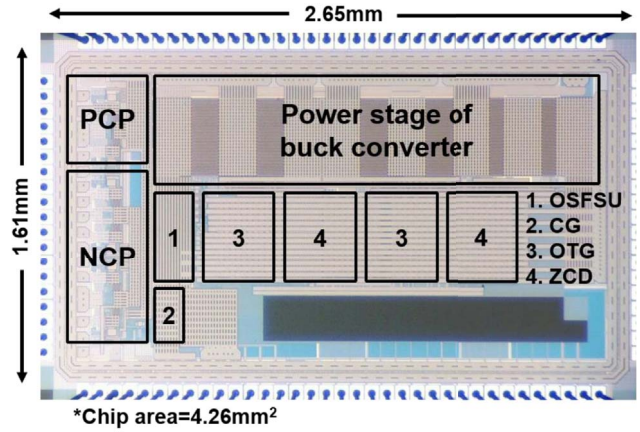

Fig. 6. Chip micrograph.

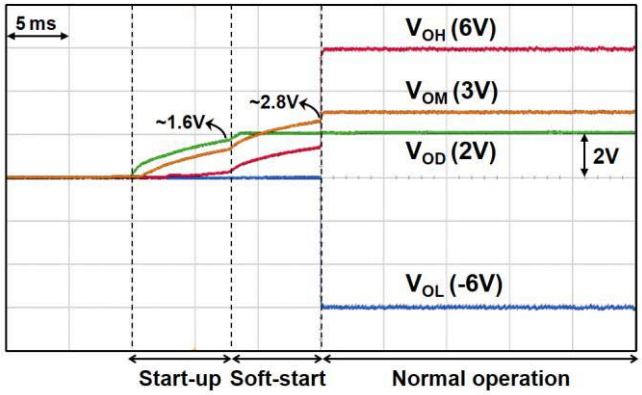

Fig. 7. Measured waveforms of the proposed battery management circuit.

V_{OH}, V_{OL}, and V_{OD} are I_{OH}, I_{OL}, and I_{OD}, respectively. Fig. 8(a) demonstrates that the cross-regulation between V_{OD} and V_{OM} in inductive buck converter is negligible by using sequential PSM control. Fig. 8(b) and Fig. 8(c) show the measured load transient waveforms of V_{OH} and V_{OL} when load current I_{OH} and I_{OL} change between 100 μA and 3mA. During I_{OH} load transient, the load regulation in V_{OH} is negligible since V_{OM} is well controlled by feedback circuits to regulate V_{OH}. On the other hand, since V_{OM} is slightly adjusted according to load current, 150 mV cross regulation is obtained in this case. During I_{OL} load transient, on the other hand, cross regulation is almost negligible and load regulation less than 200 mV is obtained due to the same reason.

The measured dependencies of the power conversion efficiency of the buck converter on output load current (I_{LOAD}) of V_{OM} under different input voltages are illustrated in Fig. 9 The buck converter achieves a peak efficiency of 96.7% at 12 mA load when V_{IN} is 3.2 V and can cover output loads ranging from 0.1 mA to 20 mA.

Fig. 10 shows the measured dependencies of buck converter's power conversion efficiency on the V_{OD} load current (I_{LOAD}) under different input voltages. The converter covers output loads ranging from 0.1 mA to 10 mA and achieves a peak efficiency of 84.5% at 10 mA load when V_{IN} is 4 V.

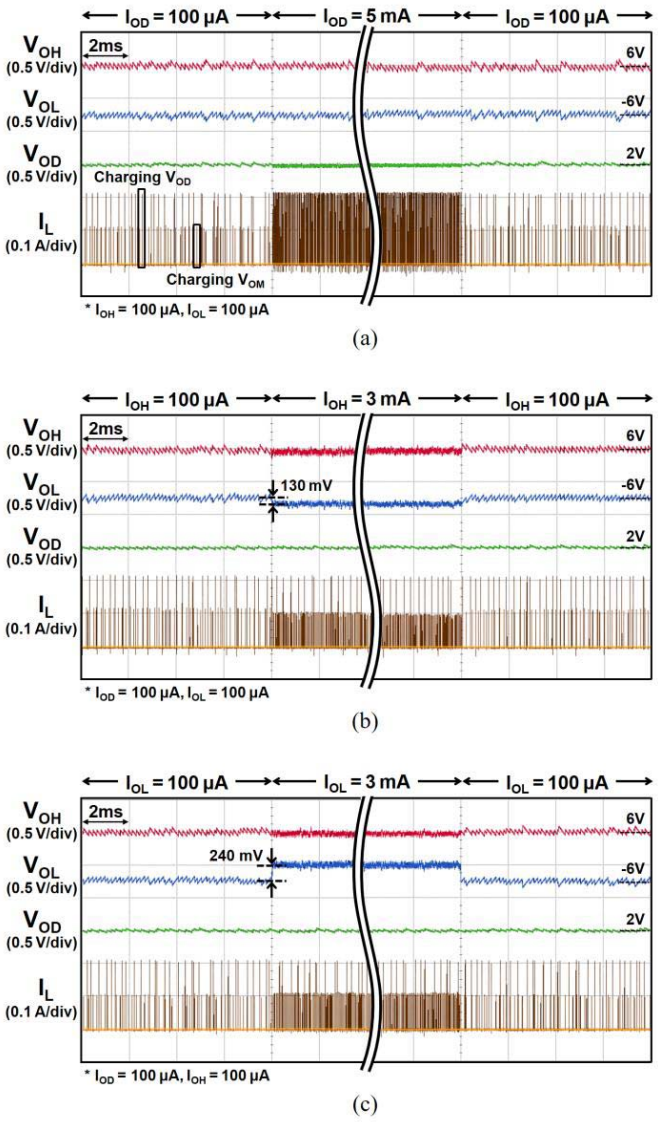

Fig. 8. Measured waveforms of load transient waveform of (a) V_{OD}, (b) V_{OH}, and (c) V_{OL}.

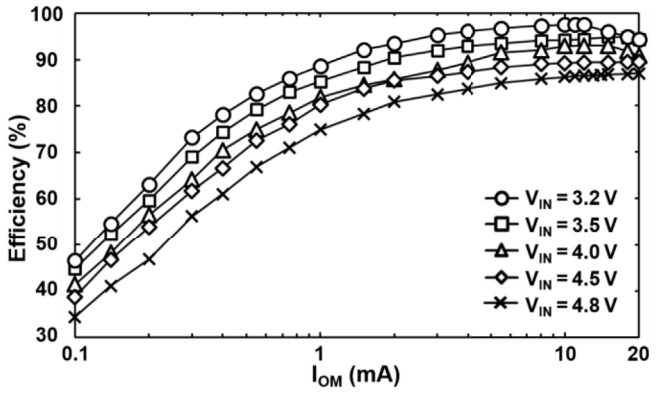

Fig. 9. Measured dependences of power conversion efficiency on output load.

Fig. 11 illustrates the measured dependencies of power conversion efficiency of the proposed BMU on the V_{OH} and V_{OL} output power (P_{OUT}) under different input voltages. The entire

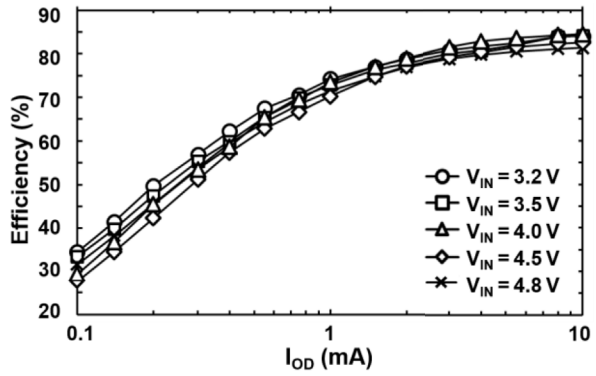

Fig. 10. Measured dependences of power conversion efficiency on output load.

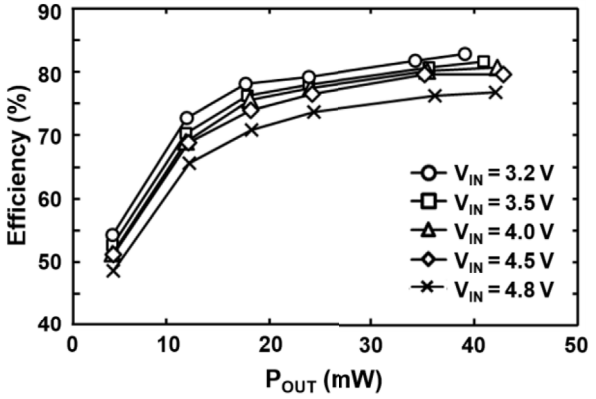

Fig. 11. Measured dependences of power conversion efficiency on output power.

TABLE I
COMPARISON WITH RECENTLY REPORTED VOLTAGE GENERATORS

		ICECS'16 [10]	A-SSCC'16 [11]	TCAS-II'17 [12]	BioCAS'18 [13]	This work
Technology		130 nm CMOS (Standard)	180 nm CMOS (HV)	130 nm CMOS (Standard)	180 nm CMOS (Standard)	180 nm CMOS (Standard)
Input voltage		1.2 V	0.02 V – 0.12 V	1.2V	1.8V & 3 V	3.2 V – 4.8 V
Number of outputs		4, bipolar	2, unipolar	2, unipolar	3, bipolar	3, bipolar
Output voltage		+ 10.6 V + 16.5 V - 9.4 V - 16.1 V	+ 4.2 V + 1.1 V	+ 2.4 V + 4.8 V	+ 9 V - 9 V - 2.7 V	+ 2 V + 6 V - 6 V
Maximum output power		< 0.5 mW	N/A	12 mW	49 mW	40 mW
Peak efficiency		69.94%	69 %	88.16%	66.34%	82.9%
Inductor (off-chip)		No	100 µH	No	No	4.7 µH
Pumping/Auxiliary capacitor	On-chip	80 pF	No	840 pF	1.6 nF	15 pF
	Off-chip	No	No	No	No	4 nF x 6
Decoupling capacitor	On-chip	N/A	No	400 pF	N/A	No
	Off-chip	N/A	100 µF x 1 1 µF x 2	No	No	10 µF x 2 1 µF x 1 10 nF x 3
Silicon area		0.24 mm^2	6.25 mm^2	1.44 mm^2	4.09 mm^2	4.26 mm^2
Verification		Simulation	Experimental	Experimental	Experimental	Experimental

BMU covers output powers ranging from 5 mW to 40 mW and achieves a peak efficiency of 82.9% at a 39 mW output power when V_{IN} is 3.2 V.

Table I shows a comparison with other state-of-the-art systems [10]–[13]. The proposed BMU manages 3.2 V to 4.8 V battery voltage using a 180 nm standard CMOS process and provides +2 V, +6 V, and −6 V regulated outputs using a SIDO buck converter and CPs. As a result, the proposed topology achieves a high conversion efficiency of 82.9% with 40 mW maximum output power.

V. CONCLUSION

In this brief, a BMU that employs a cascade of a SIDO buck converter and two CP circuits is presented for use in neuron stimulators. With the proposed topology, the BMU can be implemented in a 180 nm standard CMOS process while managing 3.2 V to 4.8 V battery inputs without overstress. The proposed circuit achieves a maximum conversion efficiency of 82.9% with 6 V, −6 V, 2 V regulated outputs.

ACKNOWLEDGMENT

The authors thank the National Chip Implementation Center (CIC) for chip fabrication.

REFERENCES

[1] C.-Y. Wu, C.-H. Cheng, and Z.-X. Chen, "A 16-channel CMOS chopper-stabilized analog front-end ECoG acquisition circuit for a closed-loop epileptic seizure control system," *IEEE Trans. Biomed. Circuits Syst.*, vol. 12, no. 3, pp. 543–553, Jun. 2018.

[2] C.-H. Cheng *et al.*, "A fully integrated closed-loop neuromodulation SoC with wireless power and bi-directional data telemetry for real-time human epileptic seizure control," in *Proc. Symp. VLSI Circuits*, Kyoto, Japan, 2017, pp. C44–C45.

[3] M. Sivaprakasam, W. Liu, G. Wang, J. D. Weiland, and M. S. Humayun, "Architecture tradeoffs in high-density microstimulators for retinal prosthesis," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 52, no. 12, pp. 2629–2641, Dec. 2005.

[4] C.-Y. Lin, Y.-J. Li, and M.-D. Ker, "High-voltage-tolerant stimulator with adaptive loading consideration for electronic epilepsy prosthetic SoC in a 0.18-μm CMOS process," in *Proc. 10th IEEE Int. NEWCAS Conf.*, Montreal, QC, Canada, 2012, pp. 125–128.

[5] V. Bobanac and H. Pandzic, "Lithium-ion batteries: Experimental research and application to battery swapping stations," in *Proc. IEEE Int. Energy Conf. (ENERGYCON)*, Limassol, Cyprus, 2018, pp. 1–6.

[6] S. Bandyopadhyay, Y. K. Ramadass, and A. P. Chandrakasan, "20uA to 100mA DC–DC converter with 2.8–4.2V battery supply for portable applications in 45nm CMOS," *IEEE J. Solid-State Circuits*, vol. 46, no. 12, pp. 2807–2820, Dec. 2011.

[7] P.-C. Liao, Y.-L. Chen, and P.-H. Chen, "A single-inductor dual-output (SIDO) DC–DC converter for implantable medical devices in 180nm standard CMOS process," in *Proc. IEEE Int. Conf. Electron. Circuits Syst. (ICECS)*, 2018, pp. 601–604.

[8] H.-H. Lee and P.-H. Chen, "A single-inductor dual-input dual-output (SIDIDO) power management with sequential pulse-skip modulation for battery/PV hybrid systems," in *Proc. IEEE Asian Solid-State Circuits Conf. (A-SSCC)*, Toyama, Japan, 2016, pp. 293–296.

[9] P.-H. Chen, C.-S. Wu, and K.-C. Lin, "A 50 nW-to-10 mW output power tri-mode digital buck converter with self-tracking zero current detection for photovoltaic energy harvesting," *IEEE J. Solid-State Circuits*, vol. 51, no. 2, pp. 523–532, Feb. 2016.

[10] A. H. Alameh, A. Bouchami, and F. Nabki, "A wide voltage range charge pump in 0.13 μm CMOS for biasing of MEMS resonators," in *Proc. IEEE Int. Conf. Electron. Circuits Syst. (ICECS)*, 2016, pp. 165–168.

[11] Y. Toyama, T. Ogawa, T. Ueno, and T. Itakura, "20 mV input, 4.2 V output SIDO boost converter with low-power controller and adaptive switch size selector for thermoelectric energy harvesting," in *Proc. IEEE Asian Solid-State Circuits Conf. (A-SSCC)*, Toyama, Japan, 2016, pp. 9–12.

[12] X. Yu, K. Moez, I.-C. Wey, M. Sawan, and J. Chen, "A fully integrated multistage cross-coupled voltage multiplier with no reversion power loss in a standard CMOS process," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 64, no. 7, pp. 737–741, Jul. 2017.

[13] S.-P. Lin and M.-D. Ker, "Design of multiple-charge-pump system for implantable biomedical applications," in *Proc. IEEE Biomed. Circuits Syst. Conf. (BioCAS)*, Cleveland, OH, USA, 2018, pp. 1–4.