Area-Efficient On-Chip Transient Detection Circuit for System-Level ESD Protection Against Transient-Induced Malfunction

Wen-Chieh Chen and Ming-Dou Ker, *Fellow, IEEE*

***Abstract*—A new on-chip transient detection circuit with superior area efficiency is proposed against the system malfunction resulting from system-level electrostatic discharge (ESD) events. With dual-latched structure, a better area efficiency can be achieved by the reduced time constant inquiry. The proposed transient detection circuit with a silicon area of 40 μm × 60 μm has been fabricated in a 0.18-μm CMOS process with 1.8-V devices. The detection sensitivity has been successfully verified under ±200 V system-level ESD tests. To achieve the "Class B" specification of IEC 61000-4-2 standard, the proposed transient detection circuit serves as a safety guard for the system. Through the hardware/firmware co-design, the auto-recovery procedure can be activated by the proposed transient detection circuit sending out a warning signal. With the proposed transient detection circuit co-works with the system program, the immunity level of microelectronic products against the electromagnetic compatibility (EMC) of ESD events can be effectively improved.**

***Index Terms*—Electrostatic discharge (ESD), system-level ESD, electromagnetic compatibility (EMC), transient detection circuit.**

I. Introduction

With the progress of CMOS technology development, the reliability issues of electromagnetic compatibility (EMC) have gained more attentions. Electrostatic discharge (ESD) events seriously threaten the silicon chips in microelectronic products due to the reduced physical dimension of transistors and the degraded noise margin of logic gates. In addition, with widely variety of applications, the environment complexity also has a significant impact on the reliability of microelectronic system [1]. Unfortunately, such electrical interferences are inevitable challenges in rigorous environments. For example, the explosive growth of wireless interfaces in IoT environments challenges the ESD protection design in IoT devices [2]. In this case, the microelectronic systems are extremely vulnerable to ESD-induced transient disturbances and easily frozen or upset.

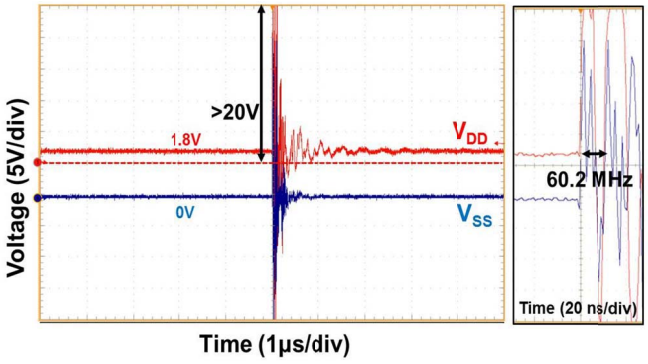

Fig. 1. The measured transient voltage waveforms on power line (V_{DD}) and ground line (V_{SS}) of a microelectronic system during +2 kV system-level ESD test. The fast ringing waveform is zoomed in the right-side figure.

During system-level ESD events, the induced high-voltage and fast electrical transients often couple randomly into power, ground, and input/output (IO) ports of CMOS ICs inside the microelectronic products. Besides, the current injection could also induce voltage fluctuations on power and ground lines due to parasitic inductance on coupling path. Fig. 1 shows the voltage perturbations on the power line (V_{DD}) and ground line (V_{SS}) in a microelectronic system under +2 kV system-level ESD test. The underdamped sinusoid of ESD stress oscillates seriously and ceases eventually. With the large noise on supply voltage, the system operation can easily be subjected and may suffer from frozen state or unexpected data loss after the interferences [3]. By classifying the response of the equipment under test (EUT), the IEC 61000-4-2 standard has specified the electromagnetic susceptibility (EMS) immunity criteria for the system-level ESD test, which is shown in Table I [4]. In order to fulfill the strict reliability requirements for IC industry, the microelectronic products are generally suggested to pass the criterion of "Class B."

Though the CMOS ICs passed the component-level ESD tests, the microelectronic system would still struggle with permanent damage or system malfunction from system-level ESD interferences [5]. Thus, on-board solutions for system-level protection often add discrete voltage-suppressing components or noise-bypassing components onto the printed circuit board (PCB) [6]. In addition, the on-chip protection design

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TABLE I
EVALUATION OF SYSTEM-LEVEL ESD TEST RESULTS [4]

CRITERION	CLASSIFICATION
CLASS A	Normal performance within limits specified by the manu-facturer, requestor or purchaser.
CLASS B	Temporary loss of function or degradation of performance which ceases after the disturbance ceases, and from which the equipment under test recovers its normal perfromance, without operator intervention. **(Automatic Recovery)**
CLASS C	Temporary loss of function or degradation of performance, the correction of which requires operator interventions. **(Manual Recovery)**
CLASS D	Loss of function or degradation of performance which is not recoverable, owing to damage to hardware or software, or loss of data.

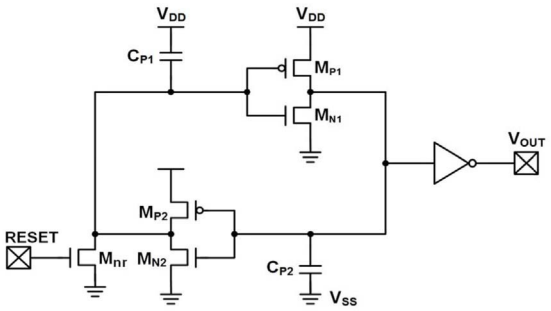

Fig. 2. Prior design of a transient detection circuit [10].

for system-level ESD has been investigated to reduce the area occupancy and improve ESD robustness of internal circuit in ICs [7], [8]. Although with these protection methods, ICs can survive from high current induced by system-level ESD, soft failures still easily occur with supply voltage fluctuation. To meet the specification of "Class B," transient detection circuits had been studied [9]–[12]. Once the transient detection circuit is aware of disturbances on power line or ground line, the warning signal is given out to perform recovery procedure of microelectronic system.

RC network is traditionally used in the transient detection circuit to identify the fast-electrical transients because of the quantitative time constant [11]. To rigorously monitor the noise on the power rails, numbers of transient detection circuit should be placed on the power rails spreading around the IC. With the pursuit of ICs area efficiency, regenerative feedback network was applied for time constant reduction in previous literatures to reduce the total area occupancy of transient detection circuits [13], [14]. The feedback network holds up the detection result, allowing the RC network to free from time-out.

Fig. 2 shows the prior design of a transient detection circuit. Two 0.5-pF coupling capacitors are added from the two output nodes of a latch to the power and ground, respectively. Once the disturbance occurs on the power/ground lines, with the help of the coupling capacitors, the latch changes its logic state from the initially stored state. Though the design dissipated the use of resistor, the two on-chip capacitors still occupy considerable area in silicon. Moreover, the detection sensitivity of $\pm$1.5kV still has a room for improvement.

In this work, a on-chip transient detection circuit is proposed. With the dual-latch structure, the required time constant can be greatly reduced for silicon area efficiency [15]. The proposed transient detection circuit has been investigated by HSPICE simulation and fabricated in a 0.18-μm CMOS process with 1.8-V devices. The detection ability has been successfully verified by system-level ESD tests.

II. NEW TRANSIENT DETECTION CIRCUIT

The proposed transient detection circuit is designed to detect and memorize the occurrences of the system-level ESD events. The initial output state of the transient detection circuit is logic "1" of 1.8-V voltage level. When the power lines undergo an EMI event due to system-level ESD, the output logic state of the proposed detection circuit will be transited to the logic "0" of 0-V voltage level.

A. Circuit Implementation

With an inspiration of [16], the proposed transient detection circuit is fully realized by MOSFETs, as illustrated in Fig. 3. The transient detection circuit contains two parts. One is a memory cell with a dual-latch structure and the other is a reset unit for initialization. The dual-latch structure is composed of two groups of cascoded NMOSFETs (M_{N1} + M_{N2} and M_{N3} + M_{N4}) and the other two groups of cascoded PMOSFETs (M_{P1} + M_{P2} and M_{P3} + M_{P4}). The gate terminals of the four NMOSFETs or PMOSFETs are individually connected to different internal nodes (A-D) to form a double-regenerative feedback network. The reset unit controlled by a "RESET" signal contains two diode-connected MOSFETs (M_{P5} and M_{N5}) and an inverter (M_{P6} + M_{N6}).

Under the normal power-on operation, the "RESET" signal of 1.8 V (V_{DD}) activates the reset operation. Thus, the node A is charged by M_{P5} to high voltage level of logic "1." With the operation of the inverter, the node D is defined to low voltage level of logic "0" by M_{N5}. Thanks to the dual-latch structure, the node B is consequently discharged by M_{N2} to 0 V (V_{SS}) of logic "0." Likewise, M_{P3} in conduction state charges the node C to 1.8 V (V_{DD}) of logic "1." Therefore, the output voltage (V_{OUT}) through a buffer is biased at 1.8 V (V_{DD}) of logic "1."

During system-level ESD events, the power and ground are subjected to random electromagnetic interferences. When the voltage on power line rapidly ramps up due to the system-level ESD stresses, the inverse logic states are stored in the four internal nodes due to the equivalent resistance and capacitance between power and ground. For example, to effectively detect the fast electrical transient, the dimensions of M_{N1} and M_{N4} are designed larger than M_{N2} and M_{N3}, respectively. Hence, the node A tends to low potential and the node B behaves conversely. Similarly, the dimensions of M_{P1} and M_{P4} are separately designed larger than M_{P2} and M_{P3} to pull up the node D and pull down the node C easily. To further analyze the circuit operation under the system-level ESD stresses, on perspective of the node D, M_{P1} with relatively large capacitance

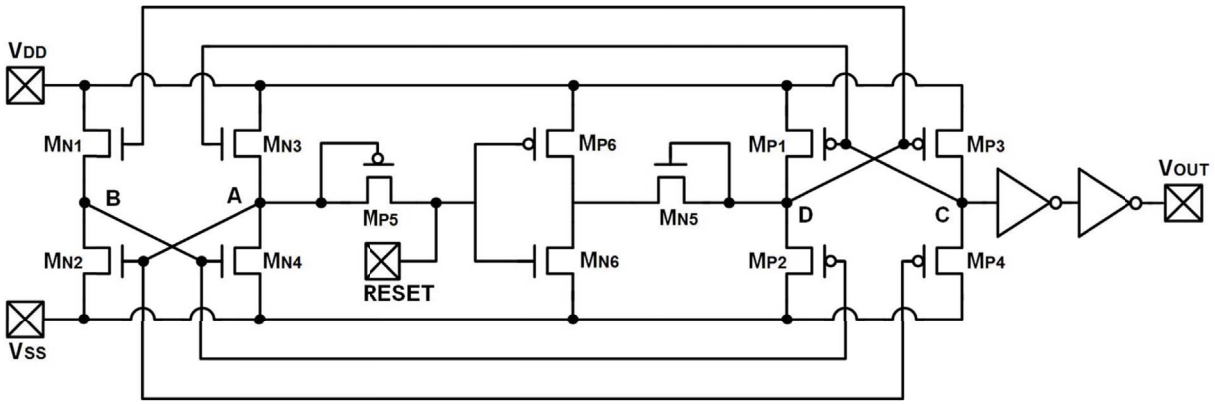

Fig. 3. The proposed area-efficient transient detection circuit realized with dual-latch structure.

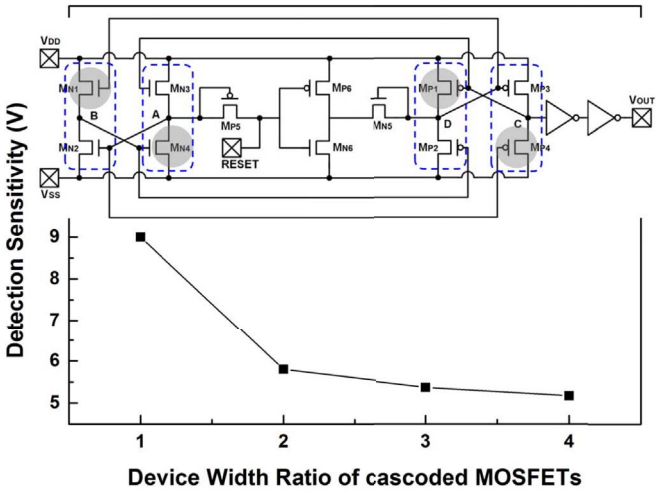

Fig. 4. The relation between ratio of device width of cascoded MOSFETs and the detection sensitivity.

immediately introduces ESD current to the node D. In addition to the large induced current on M_{P1}, the logic state can be easily converted to "1" due to M_{P2} in subthreshold state. With the dual-latch structure, the logic state at the rest of three internal nodes can be changed instantly once the node D is charged over the logic threshold voltage. Consequently, V_{OUT} can be transferred immediately to 0 V (V_{SS}) of logic "0" from 1.8 V (V_{DD}) of logic "1" after system-level ESD interferences and stably hold at logic "0" before the next reset cycle.

Fig. 4 plots the relation between the device width ratio of cascoded MOSFETs and the detection sensitivity which defined by the minimum amplitude of the simulated ESD stress. For each group of cascoded MOSFETs in blue dash block, the dimension of the MOSFET in gray area is chosen to be two times larger than the other MOSFET for the reasonable detection sensitivity. Table II lists the dimensions of devices used in the dual-latch structure of the proposed detection circuit. With the designed dimensions of the cascoded MOSFETs, the proposed transient detection circuit can efficiently detect and memorize the occurrences of ESD-induced fast electrical transient.

TABLE II
DEVICE DIMENSIONS IN THE DUAL-LATCH STRUCTURE

Devices	Width/Length (μm/μm)
M_{N1}, M_{N4}	2/0.18
M_{N2}, M_{N3}	1/0.18
M_{P1}, M_{P4}	6/0.18
M_{P2}, M_{P3}	3/0.18

B. HSPICE Simulation

The EMI characteristics induced from system-level ESD have been investigated [9]. To simulate the observed waveforms of the interferences in Fig. 1, the underdamped sinusoidal voltage source with damping frequency of 60 MHz and the calculated damping factor of 1×10^7 S^{-1} is used in the HSPICE simulation. Due to the routing placements of power lines and ground lines on PCB vary from design, EMI coupling paths to V_{DD} and V_{SS} pins are usually different. Therefore, in consideration of the complexity varies from different systems and environments, the 10 ns delay time between the two disturbances on power and ground is set in the simulation. Under the normal power-on operation, the initial dc voltages of V_{DD} and V_{SS} are set at 1.8 V and 0 V. The voltage amplitude of $+8$ V as the positive-going ESD transient is applied on V_{DD}. In addition, the voltage amplitude of $+2$ V is applied on V_{SS}. On the contrary, for negative-going ESD transient simulation, the voltage amplitude of -8 V is applied on V_{DD} and -2 V on V_{SS}.

Figs. 5(a) and 5(b) accordingly show the V_{DD}, V_{SS}, RESET, and V_{OUT} waveforms of the proposed transient detection circuit under the positive and negative system-level ESD tests. V_{OUT} is initially kept at 1.8 V (V_{DD}) and waits for disturbances induced on V_{DD} and V_{SS}. When the V_{DD} and V_{SS} are subjected to the system-level ESD stresses, the V_{OUT} is disturbed simultaneously with the corresponding positive or negative fast electrical transient. At the same time, the transient detection circuit is aware of the occurrence of the disturbance and changes the output logic state (V_{OUT}) right after the first peak of the transient. As a result, after the system-level ESD disturbance ceased, V_{DD} and V_{SS} finally recover to the stable voltage levels, V_{OUT} is transited to 0 V (V_{SS}) of logic

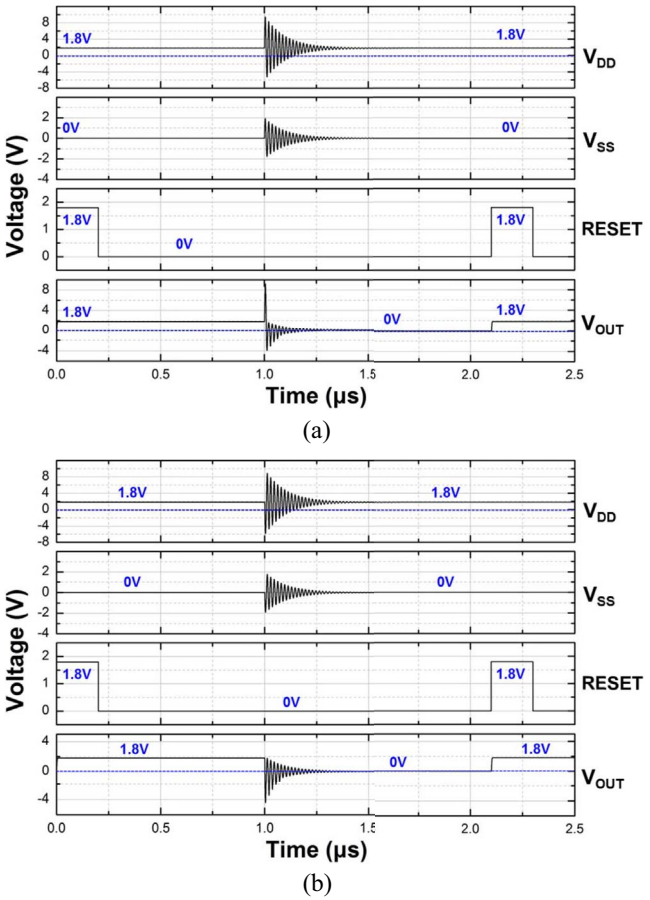

Fig. 5. Simulated voltage waveforms of the proposed transient detection circuit under (a) positive and (b) negative system-level ESD transient tests.

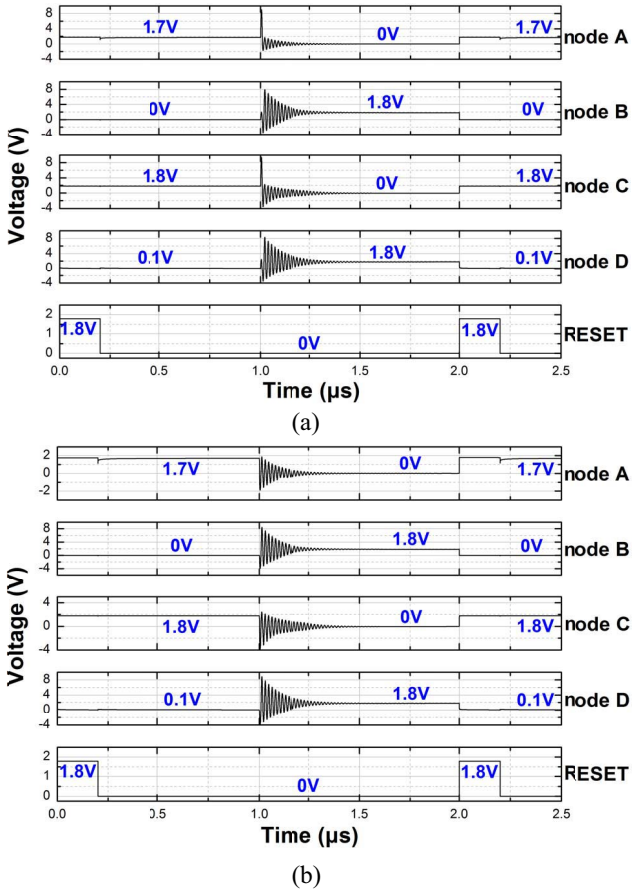

Fig. 6. The simulated waveforms of the four internal nodes and RESET signal under both positive and negative system-level ESD stresses.

"0" from 1.8 V (V_{DD}) of logic "1." After the detection, the RESET signal is sent to start the next detection period.

Figs. 6(a) and 6(b) describe the voltage change of the four initial nodes during the system-level ESD stress. At the initial state, the threshold voltage limits the voltage level at node A to 1.7 V due to subthreshold current in the dual-latch structure where NMOSFETs connected to V_{DD}. In the same way, the voltage level of node D is limited to 0.1 V as the PMOSFETs are connected to V_{SS}. Therefore, the voltage levels at node A and node D are surely able to keep M_{P4} and M_{N1} off.

Since the ESD-induced EMI is unpredictable, the damping frequency of the system-level ESD stresses is usually in the order of megahertz which decided by factors of the systems and environments. The detection sensitivity which is defined by the minimum detection amplitude is directly affected by the damping frequency for the rise time of the first oscillated cycle. Fig. 7 shows that the correlation of the detection sensitivity and the damping frequency. The proposed transient detection circuit is sensitive with the fast transient of the ESD stresses with damping frequency ranges from tens to hundreds of megahertz. The detection mechanism origins from the time difference between the rise time of induced fast transient and the RC time constant of the detection circuit. Thus, the detection sensitivity degrades when the damping frequency reduces.

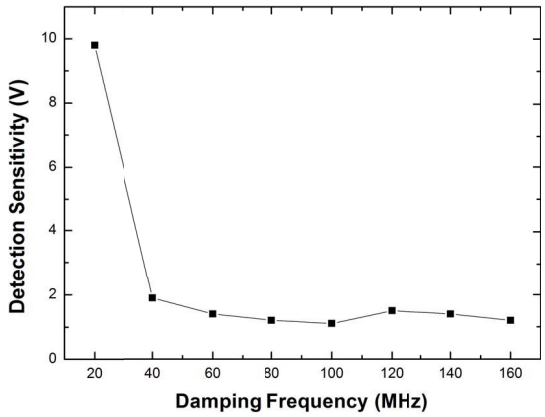

Fig. 7. The correlation between detection sensitivity and damping frequency of the simulated system-level ESD stresses.

III. Experimental Results

The proposed transient detection circuit had been fabricated in a 0.18-μm CMOS process with 1.8 V devices. The microphotograph of the test chip is shown in Fig. 8, where the occupied silicon area is 40 μm × 60 μm. The system-level ESD test with indirect contact-discharge mode is performed to verify the function of the proposed transient detection circuit.

The measurement setup referenced from the IEC 61000-4-2 standard is illustrated in Fig. 9 [4]. The voltage waveforms

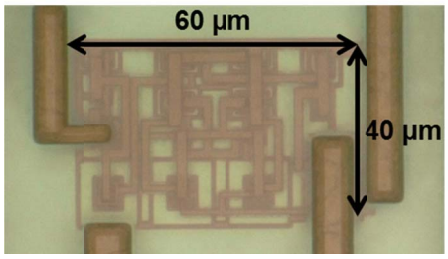

Fig. 8. The microphotography of the proposed transient detection circuit fabricated in a 0.18-μm CMOS process.

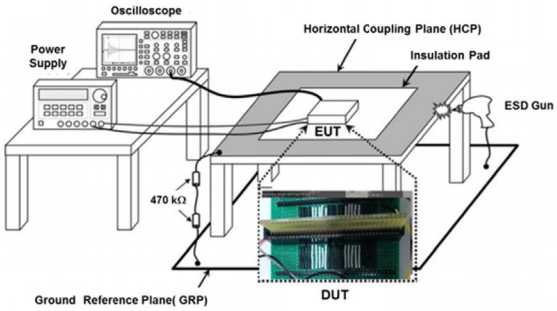

Fig. 9. Measurement environment of the system-level ESD tests.

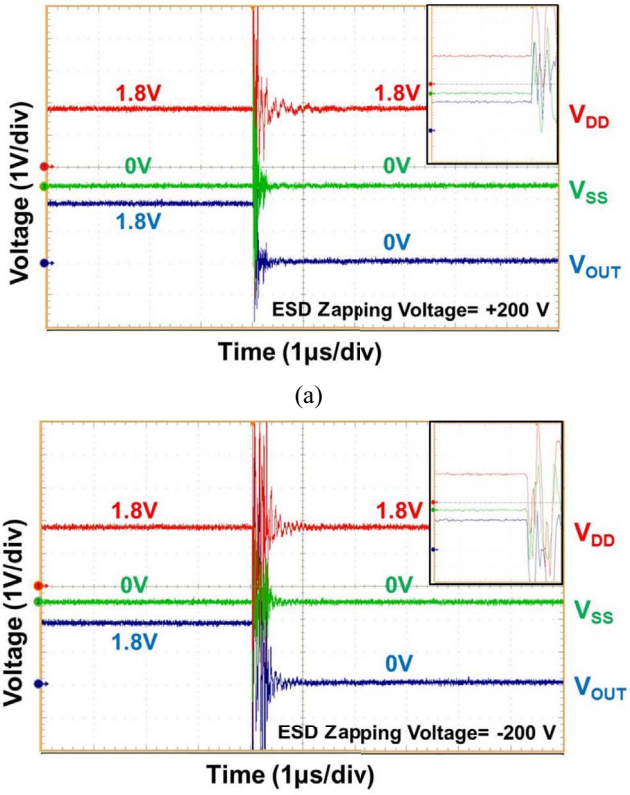

Fig. 10. The measured V_{DD}, V_{SS}, and V_{OUT} waveforms under (a) +200 V and (b) −200 V system-level ESD tests.

of V_{DD}, V_{SS}, and V_{OUT} are monitored simultaneously by a digital oscilloscope. A wooden table stands on the ground reference plane (GRP). The EUT is isolated from the horizontal coupling plane (HCP) by an insulation pad. The HCP 85is connected to the GRP with two 470-kΩ resistors in series. The ESD gun serves as a system-level ESD generator, whose discharge return cable should be connected to the GRP.

According to the standard, the indirect contact-discharge mode typically performed at the edge of the HCP, as shown in Fig. 9. The electrical transients from ESD gun couple through HCP into the power pins of the CMOS ICs inside the EUT. A 16-nA standby current is observed due to the voltage levels of the node A and node D.

The measured V_{DD}, V_{SS}, and V_{OUT} waveforms under positive and negative system-level ESD tests are presented in Figs. 10(a) and 10(b), respectively. V_{DD} and V_{SS} are set at 1.8 V and 0 V by the power supply. V_{OUT} is initialized to 1.8 V under normal operating condition. The minimum zapping voltage supported by the ESD gun of ±200 V is applied on the proposed transient detection circuit. The transient responses of V_{DD}, V_{SS}, and V_{OUT} under the +200 V ESD tests are shown in Fig. 10(a). As a system-level ESD event occurs, both V_{DD} and V_{SS} are disturbed by the injection of fast transient noises. The potential on V_{DD}, V_{SS}, and V_{OUT} ramp up simultaneously. After the system-level ESD ceased, the voltage levels on V_{DD} and V_{SS} recover to 1.8 V and 0 V, respectively. However, the potential on V_{OUT} is transited to 0 V from 1.8 V, which means that the output logic state is converted to logic "0" from logic "1." In the expectation, under an ESD zapping voltage of −200 V, the voltage levels of V_{DD}, V_{SS} and V_{OUT} rapidly decrease, as shown in Fig. 10(b). The voltage levels of V_{DD} and V_{SS} finally turn back to the initial bias, whereas V_{OUT} is changed and retain at 0 V. The measurement results indicate that, the proposed on-chip transient detection circuit can successfully identify and record the occurrences of system-level ESD events. The detection sensitivity of the proposed circuit is proven to be at least ±200 V, which is sufficiently support the minimum test level of ±2 kV defined in the IEC 61000-4-2. The comparisons of this work among the prior arts are listed in Table III.

IV. System Application

In order to achieve the criterion "Class B," auto-recovery without user intervention, the proposed transient detection circuit is co-designed with firmware. The flowchart of firmware operation co-worked with the proposed transient detection circuit is depicted in Fig. 11. During the power-on reset operation, the output of the transient detection circuit is initialized to logic "1." After that, the transient detection circuit guards against the system-level ESD interruption. The detection result (V_{OUT}) of the on-chip detection circuit is temporarily stored as an index for firmware to check the safety of the microelectronic system. The reset operation proceeds to normal operation if the safety index is "1."

Once a system-level ESD event occurs, with the function of the detection circuit, the safety index will be changed to logic "0" and followed by reset procedure. Additionally, a feedback signal will also conduct the reset procedure to initialize the transient detection circuit. Therefore, the normal operation can be performed again without any operator intervention. During

TABLE III
COMPARISON OF THIS WORK WITH PRIOR ARTS

	[9]	[10]	[11]	[12]	This work
Technology	**0.13-μm**	**0.13-μm**	**0.18-μm**	**0.18-μm**	**0.18-μm**
Detection Method	**Coupling Capacitor + Feedback Network**	**Coupling Capacitor + Feedback Network**	**RC-based**	**CR-based + Feedback Network**	**Double Feedback Network**
Reset Signal	**Yes**	**Yes**	**Yes**	**No**	**Yes**
Coupling Method	**Contact discharged**	**Indirect contact-discharged**	**Indirect contact-discharged**	**Indirect contact-discharged**	**Indirect contact-discharged**
Detection Sensitivity (Minimum zapping voltage)	**±3000 V**	**±1500 V**	**±200 V**	**± 200 V**	**±200 V**
Silicon Area	**N/A**	**~0.0054 mm^2**	**0.085 mm^2**	**0.01 mm^2**	**0.0024 mm^2**

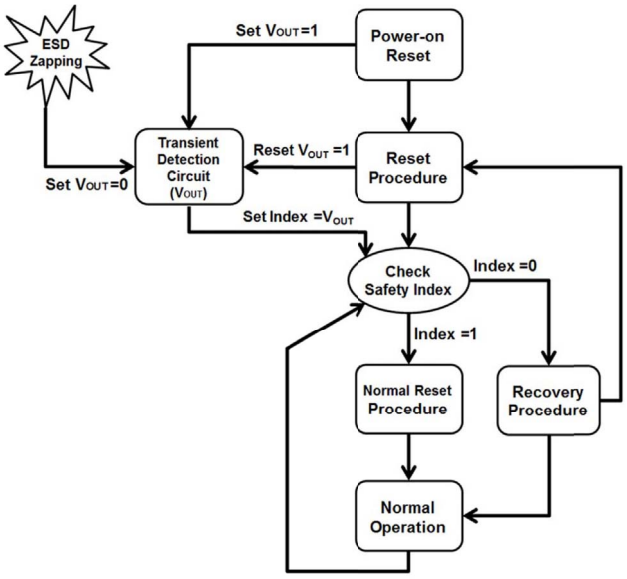

Fig. 11. The application flowchart of hardware/firmware co-design for system-level ESD protection with the proposed transient detection circuit.

the normal operation, the safety index should be checked frequently. Applying this hardware/firmware co-design flowchart, the Class-B specification of auto recovery in IEC 61000-4-2 standard can be successfully met for the microelectronic products. As a result, the system-level ESD robustness of microelectronic products can be improved.

V. CONCLUSION

An area-efficient on-chip transient detection circuit for micro-electronic systems against system-level ESD has been proposed and verified in a 0.18-μm CMOS process. The measurement results have successfully demonstrated that the detection circuit manages to detect the disturbances on V_{DD} and V_{SS} under ±200V system-level ESD tests. Moreover, the dual-latch structure in the proposed transient detection circuit achieves better silicon area efficiency. With hardware/firmware co-design between the detection circuit and system program, the auto-recovery procedure can be executed for the "Class B" criterion. For recent applications with increasing complexity, the proposed solution is beneficial to protect the microelectronic system against transient-induced interruptions.

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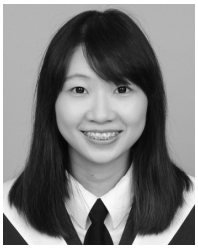

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