Avalanche Ruggedness Capability and Improvement of 5-V n-Channel Large-Array MOSFET in BCD Process

Karuna Nidhi, Ming-Dou Ker, *Fellow, IEEE*, Jian-Hsing Lee, and Shao-Chang Huang

***Abstract*— Energy handling capability of large-array devices (LADs) is one of the most dominating concerns for the designers that affect the device design and its reliability. In this paper, the improvement of the avalanche ruggedness capability by using an optional implantation layer has been investigated the first time for the application of 5-V n-channel large-array MOSFET in a bipolar-CMOS-DMOS (BCD) process. Experimental results with extensive measurements verified that the maximum avalanche current (I_{AV}) achieved from the modified device is enhanced by more than twice. Moreover, the energy in avalanche single pulse (EAS) capability is improved by more than five times. A significant improvement is noticed in the avalanche safe-operating-area (A-SOA) as compared to the original device, and the failure analysis is discussed in detail. In addition, the impact of an optional implantation layer on the total gate charge (Qg) is also compared for a LAD with a total width of 12 000 μm.**

***Index Terms*— Avalanche ruggedness, avalanche safe-operating-area (A-SOA), current in avalanche (I_{AV}), large-array device (LAD), time in avalanche (t_{AV}), total gate charge (Qg), unclamped inductive switching (UIS).**

I. Introduction

IN RECENT years, low-voltage power MOSFETs with high avalanche capability and low specific ON-resistance are actively developed due to the extensive expansion of their applications in various areas such as automotive designs, wireless communications, portable devices, dc-to-dc converters, lights, battery charging, and computer peripherals [1]–[3]. MOSFETs are widely used in high switching frequency applications. Hence, the assessment of their stability, robustness, and reliability is vital for the development of high-frequency switching power systems. For low-voltage power MOSFETs, extremely fast switching speed, high reliability, and simple fabrication process with small conduction and switching losses are mostly preferred. However, the continuous shrink of the power integrated technologies and enhancement of the device functions of the designed circuit contradicts with the device robustness. Therefore, the assessment of their stability, reliability, and robustness is vital for the development of fast switching systems [3]–[5]. In low-voltage applications, the effect of the avalanche operations is uttermost crucial for the durability of the devices. Hence, it is necessary to estimate how many avalanche operations a device can withstand before failure. The avalanche ruggedness of the device is usually assessed under the most rigorous test conditions, known as the unclamped inductive switching (UIS) test [4]–[6]. The characterization of the device ruggedness also depends on the electrical and thermal safe-operating-areas (SOAs). It is a challenging concern for designers to maintain the device ruggedness along with SOAs, especially for large-array devices (LADs) having the device size more than 5000 μm. The correlation between the device ruggedness and related tradeoffs with ON-resistance, breakdown voltage (BV), and SOA is shown in Fig. 1. The ruggedness for LADs majorly depends on the parameters such as the device area, the junction temperature T_J, and the ambient temperature T_A can be improved by the compact layout and the optimizations of the process [4]–[14].

Recently, for avalanche ruggedness improvement, many different techniques have been reported to improve and analyze UIS performance [13], [15]–[28]. Several high-voltage rugged device solutions have been proposed and analyzed such as improving the device robustness by layout techniques, especially under analysis of large current and temperature distribution area [14]–[16] or embedding silicon controlled rectifier structures into LAD [17], use of floating RESURFs, trench, floating p-well splits, implanting spacer [18]–[23], copper metallization, suppressing channel conduction techniques,

Manuscript received March 4, 2019; revised April 17, 2019; accepted May 7, 2019. Date of publication May 27, 2019; date of current version June 19, 2019. This work was supported by Vanguard International Semiconductor Corporation, Hsinchu, Taiwan. The review of this paper was arranged by Editor B. Kaczer. *(Corresponding author: Ming-Dou Ker.)*

K. Nidhi is with the Electrical Engineering and Computer Science International Graduate Program, National Chiao Tung University, Hsinchu 30010, Taiwan, and also with the Device Engineering Department, Vanguard International Semiconductor Corporation, Hsinchu 30010, Taiwan (e-mail: knidhi@vis.com.tw).

M.-D. Ker is with the Institute of Electronics, National Chiao Tung University, Hsinchu 30010, Taiwan, and also with the Department of Electronics, I-Shou University, Kaohsiung 840, Taiwan (e-mail: mdker@ieee.org).

J.-H. Lee and S.-C. Huang are with the Device Engineering Department, Vanguard International Semiconductor Corporation, Hsinchu 30010, Taiwan (e-mail: ano.lee2009@gmail.com; ajakes2010@yahoo.com.tw).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TED.2019.2916032

Fig. 1. Correlation between the device ruggedness and related trade-offs with ON-resistance, the BV, and the SOA.

and oxide charge balance process optimizations [24]–[26]. However, unlikely to HV MOSFETs and discrete devices, a very few studies were found for UIS ruggedness for low-voltages (especially lower than 20 V, not ever reported to the author's knowledge) MOS devices. For the low-voltage power switch devices, operating in the high-stress region with high current needs to be thoroughly understood for its efficient design. A novel low-voltage (30 V) trench power MOSFET was reported for enhancing both ON-resistance and the avalanche capability in the 0.5-μm technology [27]. A marvelous low ON-resistance for 20-V rated SAT-MOS was proposed in a 0.35-μm large-scale integrated (LSI) design rule with high forward blocking voltage and large current capability [28]. There have not been many instances to characterize the ability of low-voltage (LV) MOSFETs to withstand the single-pulse UIS because many designers have not demanded UIS requirements. The increasing use of LV MOSFETs in automotive and switching applications makes the necessity to have the avalanche ruggedness under UIS at inductive operations [2], [4], [5], [8], [9].

In this paper, a 5-V n-channel LAD MOSFET structure in a 0.15-μm bipolar-CMOS-DMOS (BCD) process is studied first time to analyze and enhance UIS capability. It was found to have very poor avalanche current withstand ability for the original device. Significant improvement in UIS performances is noticed and compared to the original device after using additional implantation at body area without affecting the electrical parameters such as threshold voltage, ON-resistance, and so on. The total gate charge is also studied and compared for the devices.

II. Device Design

The LV MOS studied in this paper is fabricated in a 0.15-μm BCD process. The layout top view and the cross-sectional view of the original along with the modified device are shown in Fig. 2(a)–(c), respectively. The only difference between the modified structure and the original device is additional p-type Boron implantation, named as zener diode implant (ZDI) implantation at the P+ body area. ZDI layer is an optional layer provided by the foundry. The original device without additional layer is labeled as NCH while the device

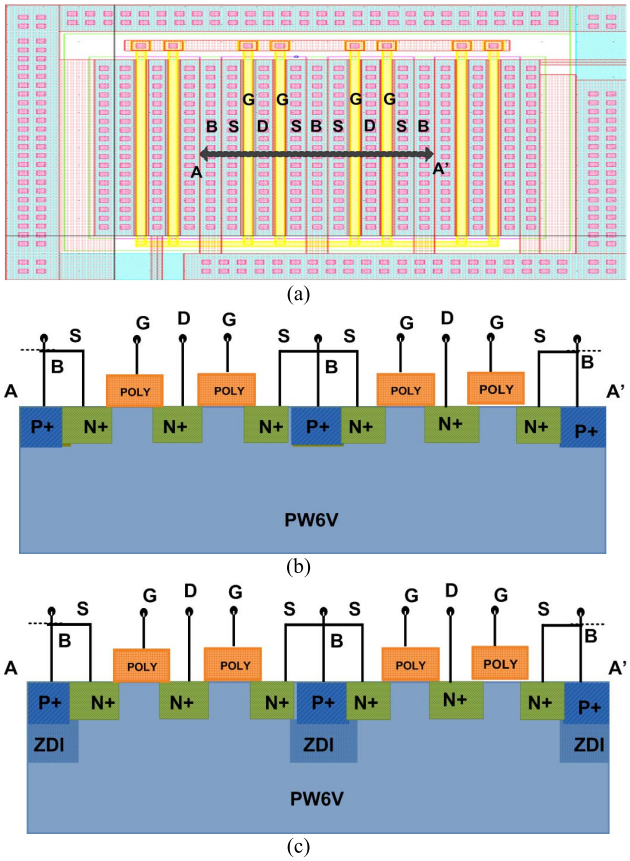

Fig. 2. (a) Layout top view, (b) cross-sectional view along the A-A' line for the original device in which P+ body pick-up is inserted after every 2 fingers, and (c) cross-sectional view along the A-A' line with an additional implantation (ZDI) at P+ body area in the original device.

with the additional ZDI layer is labeled as NCH_ZDI. For this work, LAD structures were drawn in multifingered layout style with a total effective width (W) of 6000 μm (80 fingers) and 12 000 μm (2 $\times$ 80 fingers) to emulate the high-current driving capability of the output array. The channel length and each device width are kept the same for all MOS transistors, i.e., 0.6 and 75 μm, respectively. P+ guard ring is surrounding the whole device to define that the body potential will affect the turn-on uniformity in LADs. To improve the secondary breakdown current (I_{t2}), the additional body pickup structures of "two fingers per pickup" are inserted into the source region of the LADs, as shown in Fig. 2, which will effectively balance R_{SUB} between parasitic BJTs [9].

In order to prevent the failure during the device operations, especially when integrating LADs into the analog power ICs, the most important electrical parameters including OFF-state BV, threshold voltage (V_{th}), and the specific ON-resistance ($R_{\mathrm{ON,sp}}$) of the large array is noticed carefully to achieve the optimal performances [9]. For the correlation between the device ruggedness and SOA, the electrical and thermal instability characterization should be examined at shorter and longer pulsewidths, respectively. The additional ZDI implantation layer impact on SOAs and its dc performances were discussed in [9]. Table I shows the characterized comparison of the dc, transmission line pulse (TLP), and the thermal SOA (T-SOA) for NCH and NCH_ZDI under 12 000 μm.

TABLE I
COMPARISON OF DC, TLP, AND T-SOA CHARACTERISTICS

	DC			TLP PW= 100ns, V_{GS}=0V		T-SOA PW= 300µs
Device	BV (V)	V_{th} (V)	$R_{ON,sp}$ (mΩ-mm^2)	Vt1 (V)	It2 (A)	Max I_{Drain} (A)
NCH	10	0.75	2.54	10.4	0.95	1.45
NCH_ZDI	10	0.76	2.56	10.4	5.62	3.75

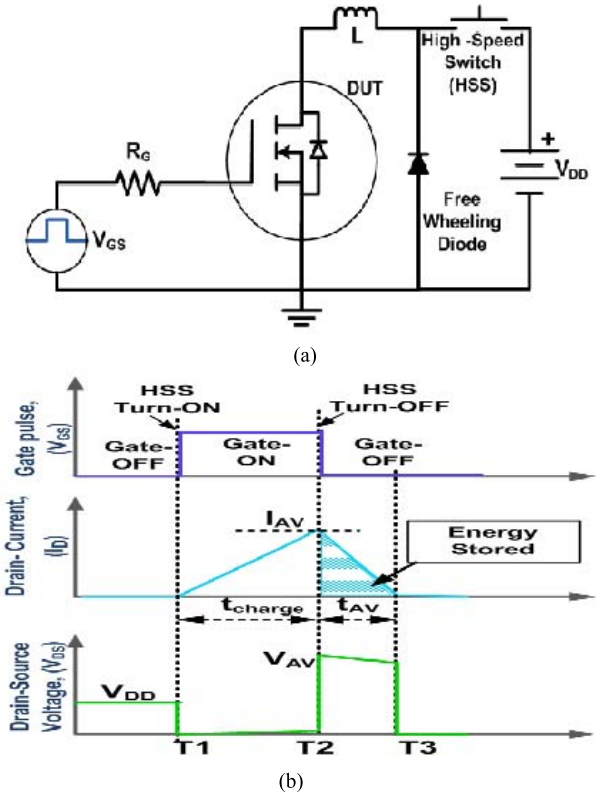

Fig. 3. (a) Schematic UIS test circuit recognized by JEDEC std. (b) Operational UIS waveforms.

III. UNCLAMPED INDUCTIVE SWITCHING OF NCH AND NCH_ZDI

For switching applications, rugged devices are important, as these devices must have to sustain a great deal of stress, especially when inductive loads are involved. To analyze the impact of additional ZDI layer to the device ruggedness under normal circuit operations, UIS test needs to be determined. UIS is an extremely high-stress test used to determine the maximum amount of avalanche energy a device can handle by forcing a charged unclamped inductor to discharge through the device under test (DUT).

To analyze the avalanche ruggedness characteristics, an improved, optimized, and industry-recognized single-pulse UIS test circuit is used for this work. The schematic UIS test circuit and its typical operational waveforms recognized to the JEDEC standard are shown in Fig. 3(a) and (b), respectively [29]–[31].

A high-speed switch (HSS) and freewheeling diode are added to the traditional test method, as shown in Fig. 3(a). During the UIS test, the control circuit turned on the HSS and the current rises to the desired level through the inductive load (L) results in the charging of the inductor. The major advantage of the modified UIS test circuit is that its V_{DD} can be increased beyond the MOSFET's maximum rated V_{DS}. This will speed up the inductors initial charge time (t_{charge} = T2 − T1) leading to overall faster test times as well as less device ON-state time and, therefore, less self-heating of the device prior to the avalanche.

When the MOSFET's gate is switched on, the HSS is also enabled, as shown in waveform [Fig. 3(b)], its drain current rises to the desired test current in a fixed time interval (T2 − T1) at the rate of

$$\frac{di}{dt} \approx \frac{V_{DD}}{L} \tag{1}$$

where the total series resistance along the circuit is assumed to be small, L is the load inductor, and V_{DD} is the supply voltage.

Once the desirable test current is reached, MOSFET's gate and the HSS are switched off immediately. This turns off the DUT and simultaneously removes the power supply to the device so that only the energy stored in the inductor field is available for dissipation in the device under avalanche conditions. A normal DUT now develops a high avalanche voltage (V_{AV}) that rapidly dissipates the inductor's magnetic field. The value of the expected rate of inductor field decline is calculated (T3 − T2) for each type of device, using the inductance selected, the given peak current, and the rated drain-to-source voltage (rated V_{DS}) parameter value for the device. The energy, which is stored in the inductor, is dissipated on the DUT during the avalanche time period (t_{AV} = T3 − T2), and the device will enter into the dynamic avalanche breakdown (V_{AV}) mode. At this point, the DUT must withstand a BV until the drain current decreases from the maximum avalanche current (I_{AV}) to 0 in a time period of t_{AV}. The time in avalanche (t_{AV}) is expressed as

$$t_{AV} \approx \frac{I_{AV} * L}{V_{AV}}. \tag{2}$$

After the HSS is turned off, the freewheeling diode becomes the path for the circulating current and thus keeping the voltage drop in the inductor equal to the avalanche energy. The energy in avalanche single pulse (EAS) is calculated as

$$\text{EAS} \approx \frac{1}{2} * L * I_{AV}^2. \tag{3}$$

In this paper, the UIS test is performed for LAD structure having a total effective width (W) of 6000 and 12 000 μm using the ITC 55100 UIS load tester under SOP-8 package. In order to identify the avalanche behavior of the DUT, UIS measurement test conditions were defined by V_{DD} = 5 V and V_{GS} = 6 V. The measurements were performed on numerous devices at room temperature with different inductive loads.

The maximum pass case typical current and voltage waveforms of original (NCH) LAD structure for the inductance load (L) equal to 2 mH under 6000 and 12 000 μm are

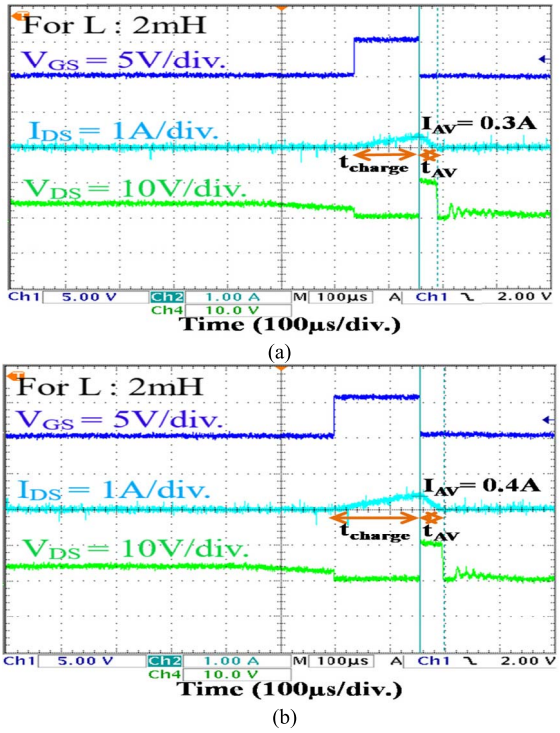

Fig. 4. Maximum pass case typical current and voltage waveforms of NCH for the inductance load (L) = 2 mH under (a) W = 6000 μm and (b) W = 12 000 μm.

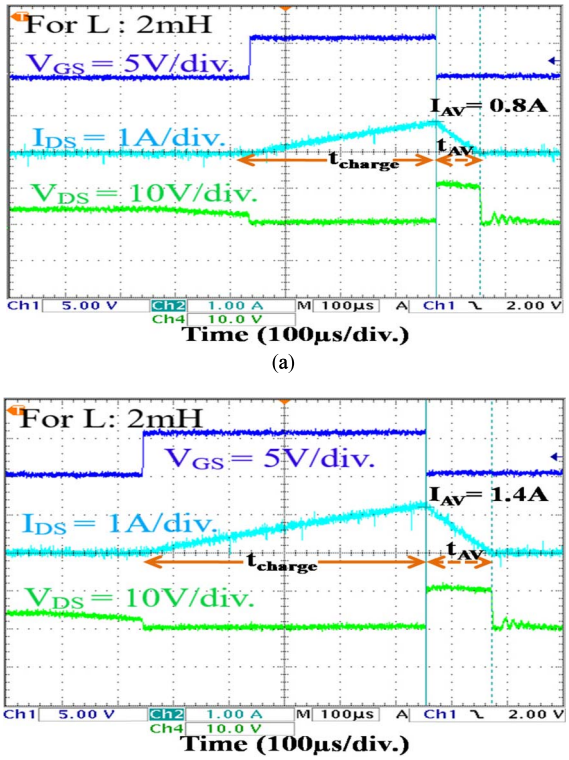

Fig. 5. Maximum pass case typical current and voltage waveforms of NCH_ZDI for the inductance load (L) = 2 mH under (a) W = 6000 μm and (b) W = 12 000 μm.

shown in Fig. 4(a) and (b), respectively. For a passing test, the avalanche current (I_{AV}) decreases almost linearly to zero at $t = t_{AV}$. Smaller avalanche current is achieved by the original device (NCH) because both the hole and electron current will produce sufficient amount of voltage across the body-drain capacitor and the body resistance to turn on the n-p-n bipolar junction transistor (BJT). The parasitic BJT is activated early even at small avalanche current due to increased base resistance. The measured avalanche current sustained by NCH is 0.3 and 0.4 A for 6000 and 12 000 μm, respectively.

In order to improve the device ruggedness, the ability to achieve the maximum avalanche current during UIS events must be improved, and at the same time, the turn-on ability of the parasitic drain-body-source n-p-n BJT must need to be suppressed. Fig. 5(a) and (b) shows the maximum pass case waveforms of NCH_ZDI for the inductance load (L) = 2 mH under 6000 and 12 000 μm, respectively. Using the same analysis as the original device (NCH), the parasitic BJT is activated at avalanche current of approximately 0.8 and 1.4 A under 6000 and 12 000 μm, respectively. The charging time (t_{charge}) is different in Figs. 4 and 5 because the measurements were performed for the maximum pass case of the DUTs. The maximum current sustained by the NCH and NCH_ZDI is different so as t_{charge}. From UIS plots for NCH and NCH_ZDI as shown in Figs. 4 and 5, it is inferred that adding ZDI implantation in P+ body area is an effective way to suppress the parasitic n-p-n BJT. The avalanche current sustained by the modified device (NCH_ZDI) is more than twice that of the original device (NCH) for L = 2 mH.

Fig. 6 shows the device cross-sectional view with the ZDI implantation layer to effectively suppress the turn-on of the

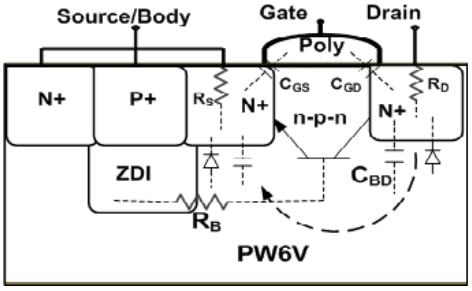

Fig. 6. Device cross-sectional view with ZDI layer to suppress the turn-on of the emitter-base junction.

emitter–base junction. During the avalanche event, the device is subjected to a voltage in excess of its BV, and the electric field across the junction will reach a value at which the avalanche multiplication will commence. A large number of impact-generated carriers are created to form the avalanche current (I_{AV}) to consume unclamped inductive energy. The maximum electric field occurs due to the PW6V diffusion resulting in most of the avalanche current entering into the body region. The lightly doped region constitutes a body resistance, which will give rise to a voltage drop beneath the N+ diffusion. The p-n junction formed by the body and source diffusion is the base–emitter junction of the parasitic n-p-n. Once the voltage drop grows larger than built-in potential of N+ source/PW6V (~0.7), the avalanche current or body resistance (R_B) becomes high enough so that the p-n junction will become forward biased and turning the BJT-on to form a current path with the thermal breakdown. The rise in

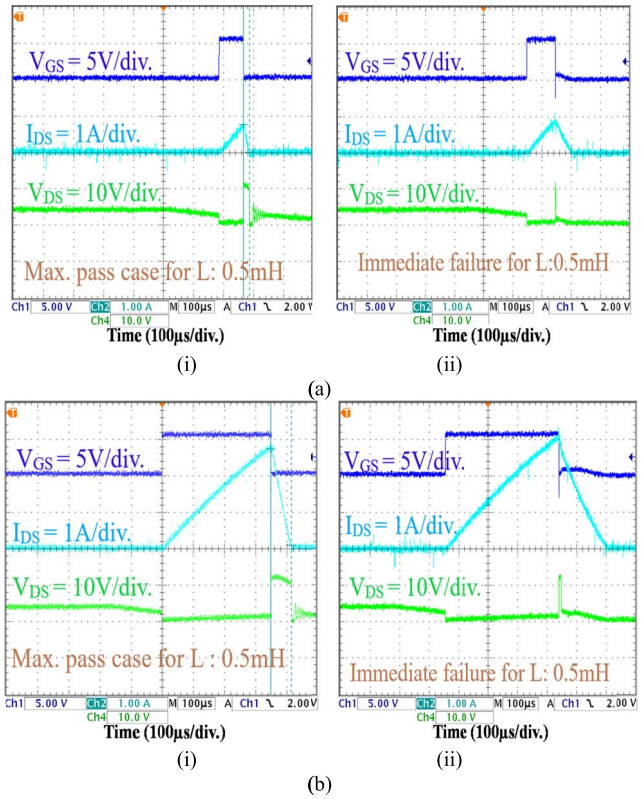

Fig. 7. Typical UIS waveforms of (i) maximum pass and (ii) immediate failure for $L = 0.5$ mH (a) NCH and (b) NCH_ZDI under $W = 12\,000$ μm.

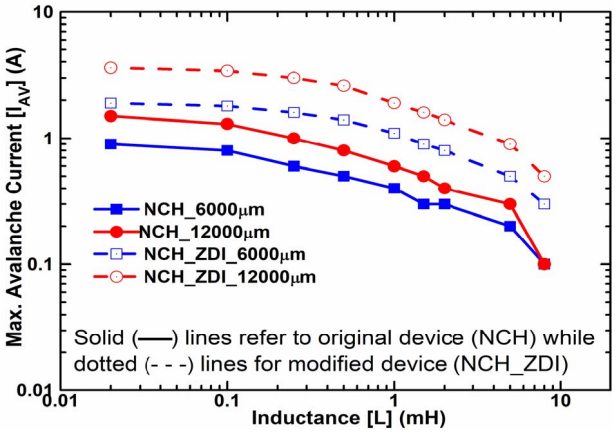

Fig. 8. Measured maximum avalanche current (I_{AV}) comparison at different inductance values for NCH (solid lines) and NCH_ZDI (dotted lines) under $W = 6000$ and 12 000 μm.

avalanched induced base–emitter voltage due to a positive resistive temperature coefficient while, at the same time, due to nonuniformity in the diffusions, the negative temperature coefficient of base–emitter voltage associated with a forward biased p-n junction. The heat generated by the energy from avalanche current and current crowding will rapidly result in the secondary breakdown of the parasitic transistor. Under the large time-varying current, the failure may be caused by electromagnetic induction exerts on all interconnects to affect the behavior of transistors may be attributed to the skin effect at the early turn-on [32]. With an applied voltage, a critical field is reached where impact ionization tends to infinity and

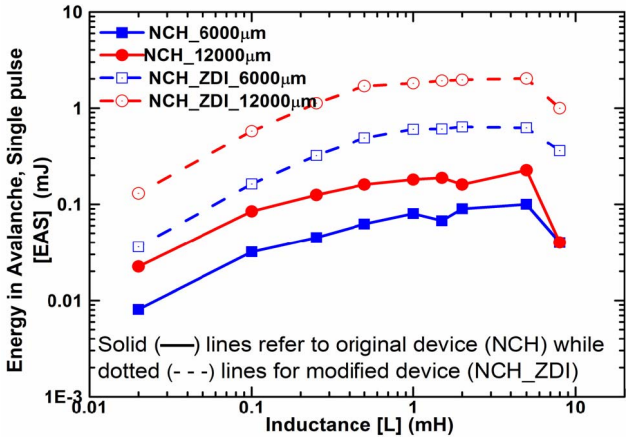

Fig. 9. Calculated EAS comparison at different inductance values for NCH (solid lines) and NCH_ZDI (dotted lines) under $W = 6000$ μm and 12 000 μm.

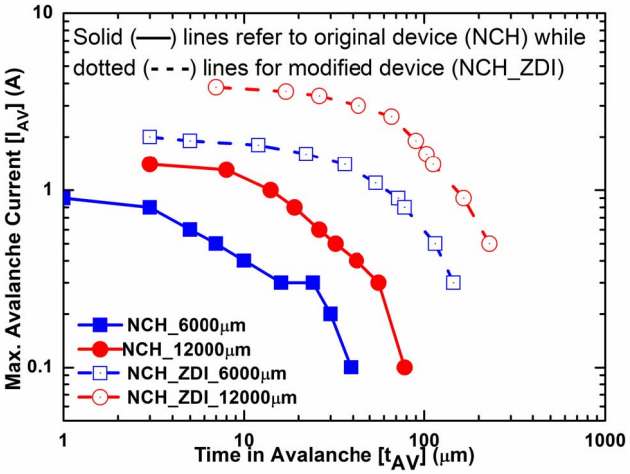

Fig. 10. A-SOA comparison for NCH (solid lines) and NCH_ZDI (dotted lines) under $W = 6000$ and 12 000 μm.

carrier concentration increases due to the avalanche activation. The strong electric field causes the maximum current to flow in close proximity of the parasitic BJT. In order to suppress the bipolar to turn-on, a p-type implantation layer at the P+ body area will reduce the parasitic resistance due to higher doping concentration as compared to PW6V. The net effect of reducing R_B will decrease the voltage drop on the resistor to prevent the BJT to turn on and neglect any kind of domination of the skin effect, which eventually leads to generate higher avalanche current in comparison to the original device (NCH). UIS measurements were performed under low inductor values (short avalanche duration) for their maximum pass (just before failure) and immediate failure cases so that the avalanche robustness of both the devices (NCH and NCH_ZDI) are limited by the activation of parasitic BJT but not the rise in junction temperature.

Fig. 7 shows the UIS performance of NCH and NCH_ZDI under identical conditions $V_{DD} = 5$ V $V_{GS} = 6$ V, and $L = 0.5$ mH. Fig. 7(a) show the original device (NCH) performance, whereas Fig. 7(b) shows the performance of the modified device (NCH_ZDI) in which (i) is the maximum pass and (ii) is an immediate failure case under

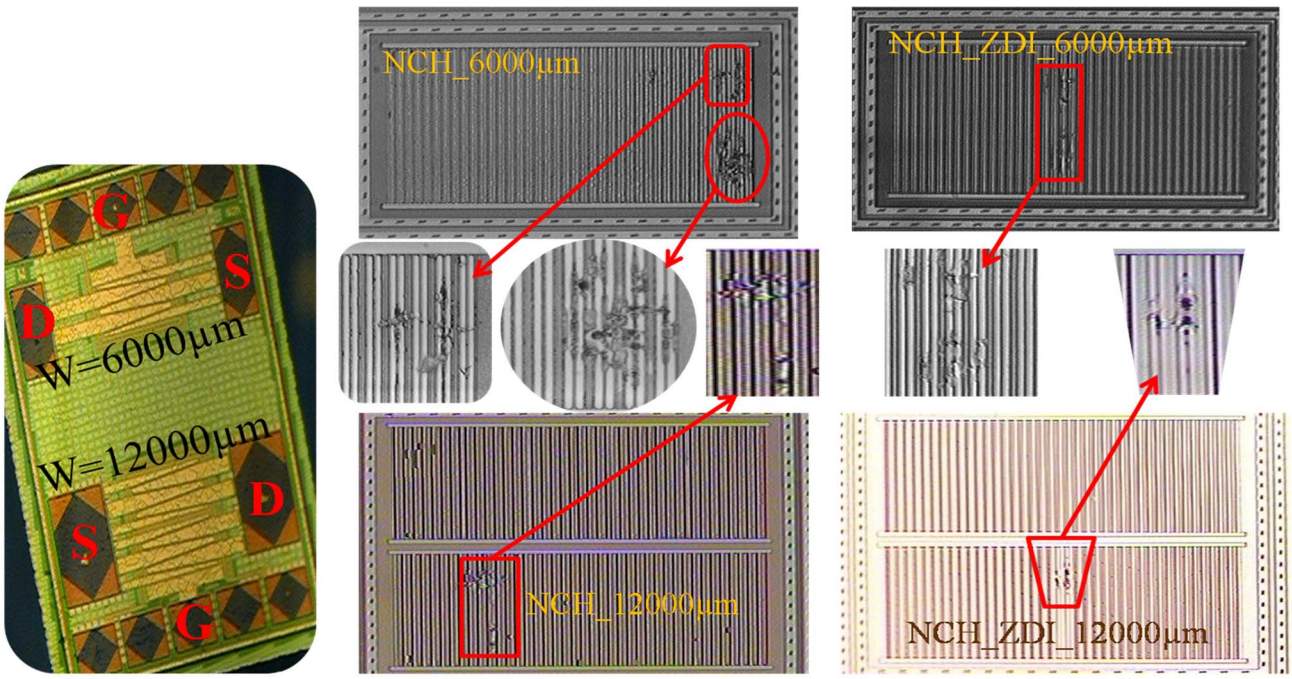

Fig. 11. Failure devices after UIS event (a) decapsulated die and delayered DUTs to OD for (b) NCH devices and (c) NCH_ZDI device under $W = 6000$ and 12 000 μm.

12 000 μm, respectively. In the immediate failure case, the avalanche current is large enough to activate the parasitic BJT at some location of the device due to the negative temperature coefficient of the base–emitter junction. A hotspot may form due to either current crowding or thermal runway occurrence at the location of the activated parasitic BJT.

In high-performance circuits and applications, designers use to push devices to its extreme condition of switching speed and current. In order to achieve high currents, designers will use parallel MOSFET devices but it should be noted that MOSFETs connected in parallel do not equally share current when they are avalanched. The maximum avalanche current the device can sustain is obtained from the peak value of the drain current waveform shown in Fig. 7(i). Meanwhile, due to self-heating during the avalanche with a larger inductor, the rate of reduction in the maximum avalanche current is faster. The maximum avalanche current performances of both the devices are compared under 6000 and 12 000 μm as shown in Fig. 8. It shows that the maximum I_{AV} is a function of the inductance value. In case of NCH, the maximum avalanche current (I_{AV}) for the pass case is 0.1 A with different dimensions (W = 6000 and 12 000 μm) under L = 8 mH, as shown in Fig. 8. The minimum measured current and measurement step for ITC 55100 UIS load tester are limited to 0.1A. Both the devices fail for 0.2 A under a similar condition. The curve shown in Fig. 8 can be used to design an application circuit considering the prevention of the MOSFET failure in case of unintended avalanche conditions.

Since the EAS dissipated in the device is equal to energy stored in the magnetic field of the inductor, this is calculated by using (3). The amount of inductively stored energy that the device is capable of dissipating without the failure actually increases as the inductance increases. The EAS comparison for both the devices under different sizes (6000 and 12 000 μm) is shown in Fig. 9. The calculated EAS capability is inversely proportional to the maximum avalanche current. The energy rugged capability is improved by more than five times than the original device.

To support the designers in determining the maximum avalanche current and the energy handling ability over a range of avalanche conditions, the avalanche SOA (A-SOA) is shown in Fig. 10. The curve is plotted between the measured maximum avalanche current (I_{AV}) and time in avalanche (t_{AV}) for different inductors. The curve is drawn to ensure that the device will never exceed its actual capability nor push the device beyond the safe mode of the operation. It allows designers to estimate, under a wide range of inductances and currents, whether the device is exceeding its avalanche capability or not. Fig. 10 shows the comparison of the avalanche SOA (I_{AV} vs. t_{AV}) for NCH and NCH_ZDI under two different dimensions of LAD structures. It can be seen that the peak avalanche current sustainable by the device decreases with increasing the avalanche duration, i.e., when a larger inductor is used, a smaller peak current is needed to destroy the device. For the real IC applications, the size could be much larger than 6000 or 12 000 μm. However, the devices of 6000 or 12 000 μm studied in this paper can be as a useful reference for designers.

IV. Failure Analysis and FOM

Avalanche is a critical working condition for any power MOSFETs to analyze how the variations in current affect its behavior [33]. To investigate the location of failure on the die during the UIS event, the failure analysis is performed on several failed devices. The image of a decapsulated die is shown in Fig. 11(a). No defect can be seen from the top, and

it indicates that there is no melting of metal layers during the avalanche failure. For further analysis, failed DUTs of NCH and NCH_ZDI are delayered to OD, as shown in Fig. 11(b) and (c), respectively. The damages on the drain, poly gate, and the source contacts verify that the failure is caused by the current crowding due to the activation of the parasitic n-p-n BJT. The destruction point seems to be melted probably due to the abrupt current concentration at a weak area. Carefully inspected to all the failure DUTs, it was found that the damage points of the original device (NCH) samples are similar and located near the edge, as shown in Fig. 11(b). It verified the early activation of parasitic n-p-n BJTs that lead current crowding in the source–drain area and domination of the skin effect due to higher R_B. The heat generated by the energy from the avalanche current and current crowding rapidly result in the secondary breakdown of the parasitic transistor. On the other hand, additional ZDI implantation at the P+ body area will reduce the base resistance to prevent the device from early turn-on as well as reduce the domination of the skin effect during the UIS event. Fig. 11(c) shows the damage locations are in the center of the devices. It verifies that the current distribution uniformity of NCH_ZDI is better than the original device. The failure point around the middle part of the modified devices indicates the less efficient cooling within the device around the center; since near the edge, pads are known as a good heat sink.

Immediate failure curves shown in Fig. 7 for $L = 0.5$ mH indicate that failure caused by the current as both the devices hold the avalanche BV for a finite time before destruction. The experimental waveforms during the failure of NCH and NCH_ZDI under 12 000 μm shown in Fig. 12 are evidence for the current failure. It has been found that the original device (NCH) and the modified device (NCH_ZDI) hold its avalanche BV for ~200 ns and ~10 μs before destruction, as shown in Fig. 12(a) and (b), respectively. The destruction in the NCH device inferred that the current crowding effect is more prominent due to higher R_B, which leads BJT to turn on much earlier than the modified device.

To give the interpretation and verify the mechanism of silicon test results and failure locations, a 2-D device UIS simulation using TSUPREME and MEDICI is performed for NCH and NCH_ZDI under the eight-finger structure. Fig. 13 shows the UIS waveforms of pass and failure cases for (a) NCH and (b) NCH_ZDI at a fixed load inductor ($L = 0.15$ mH) under different gate pulses. Eight-finger NCH device meets the failure at a gate pulse of 1000 ns (pass for 900 ns); while NCH_ZDI shows the failure at 1300 ns under the similar condition (pass for 1200 ns). Both the devices hold its avalanche BV for a few nanoseconds before destruction, as shown in Fig. 13(a) and (b). The failure of NCH at lower gate pulse inferred the nonuniformity and massive current crowding in the source–drain area that leads BJT to turn on earlier as compared to NCH_ZDI. Fig. 13(c) shows the net doping profile before MEDICI UIS device simulation to verify the structural difference between NCH and NCH_ZDI in TCAD process simulation. The total current, hole current, and the temperature distribution profiles are compared during UIS failure for NCH (at 1000 ns) and NCH_ZDI (1300 ns) at

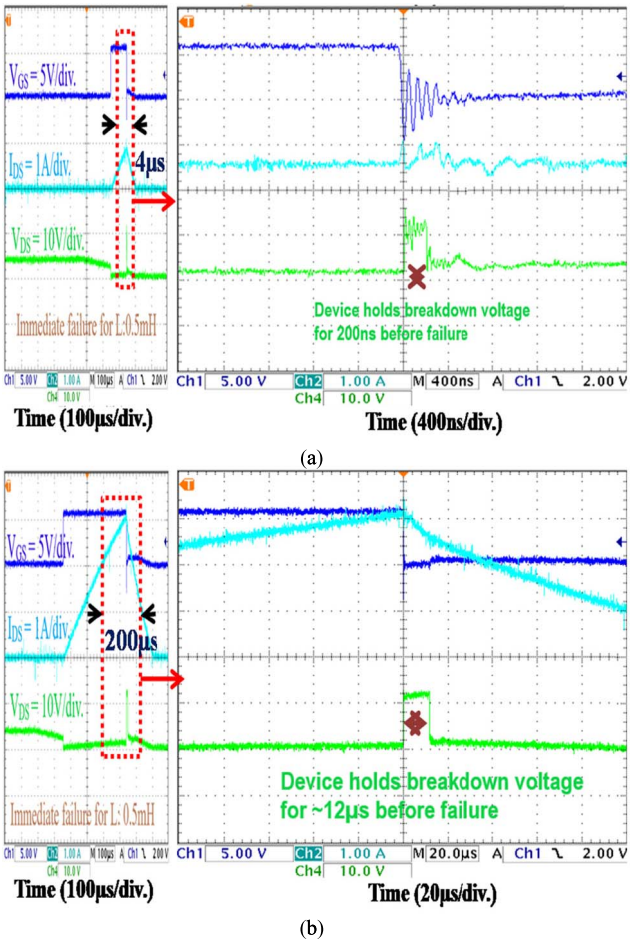

Fig. 12. Immediate failure curves for $L = 0.5$ mH of (a) NCH and (b) NCH_ZDI refer the current failure.

2E-6 second. Failure locations are interpreted at a position of current crowding and the maximum temperature distribution from the TCAD profile. The failure location observed in the NCH device is nearer to the edge while for NCH_ZDI is around the center part of the device. NCH_ZDI device capability to sustain longer pulsewidth and its current and temperature profile during UIS failure inferred that additional ZDI implantation reduces the body resistance (R_B) and improve the device uniformity that leads to delay the BJTs turn-on. The failure trends of waveforms and the failure locations during TCAD simulation for both the devices are almost similar to the silicon measurement.

Since a significant improvement is observed in dynamic parameters like SOAs (E-SOA and T-SOA) and the avalanche ruggedness, the total gate charge (Qg) needs to be compared to observe the impact of additional ZDI implantation. The value of Qg is a key parameter because it gives other essential information about switching such as gate driving loss, switching time, and so on [34].

The gate–source voltage versus time measurement is performed for both the devices under the same measurement conditions $V_{DD} = 5$ V, $V_{GS} = 6.5$ V, and $I_G = 0.05$ A. Qg is a product of gate current (I_G) and time (t). The impact on Qg due to stray capacitance is excluded. The total gate charge (Qg), the gate–source charge (Qgs), and

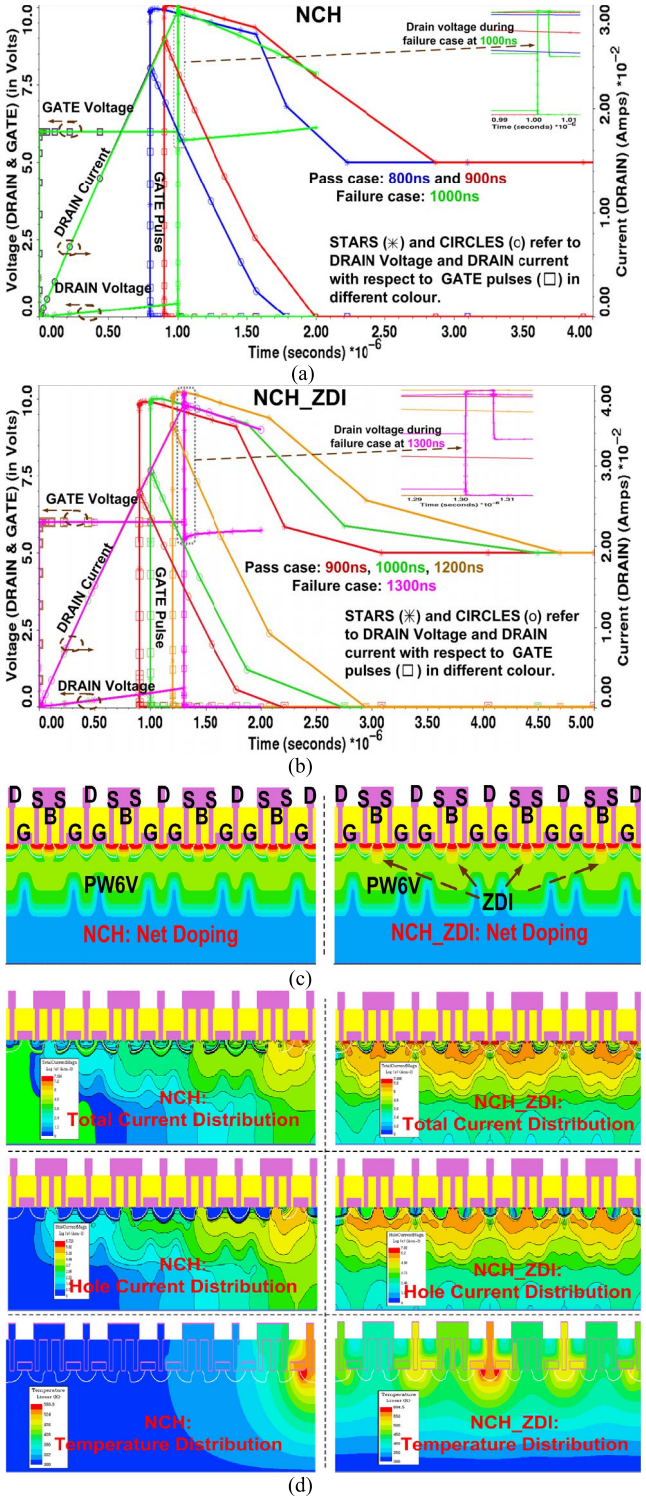

Fig. 13. UIS TCAD simulated waveforms comparison at different gate-pulse funder eight-finger structures of (a) NCH and (b) NCH_ZDI. TCAD profiles comparison including (c) doping and (d) total current, hole current, along with temperature distribution for the failure case.

the gate–drain charge (Qgd) are compared, as shown in Fig. 14 or both the devices under $W = 12\,000\ \mu$m. It shows that the differences are almost negligible in term of Qgs, Qgd, and Qg between both the devices. The measured Qg value for NCH and NCH_ZDI is 0.215 and 0.218 nC, respectively. The ON-resistance of both the devices is the same

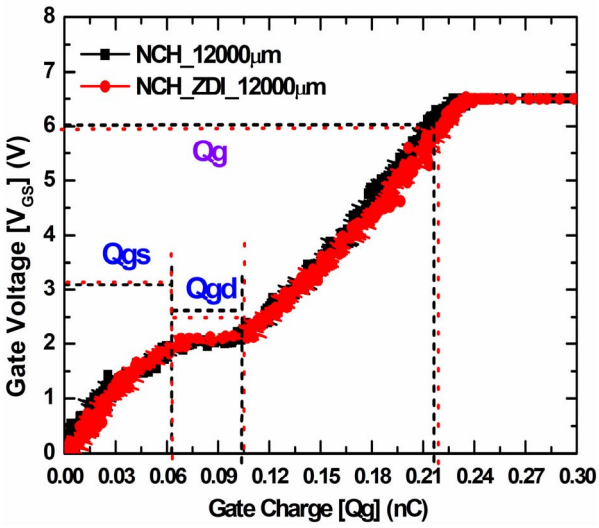

Fig. 14. Measured Qgs, Qgd, and Qg are compared with excluding the impact of stray capacitance for NCH and NCH_ZDI under $W = 12\,000\ \mu$m.

(mentioned earlier in Section II). Hence, the figure of merit (FOM) that is the product of ON-resistance and the total gate charge (Qg) remains the same.

V. Conclusion

The improvement of the avalanche ruggedness under the UIS test has been investigated the first time for a 5-V n-channel large array MOSFET with an optional implantation layer (ZDI) at the P+ body area in 0.15-μm BCD process. Measurement results showed that the maximum withstand current is improved by more than twice while energy handling capability is enhanced by more than five times compared to the original device without affecting their dc parameters such as ON-resistance and threshold voltage. The A-SOA has also showed a significant improvement. The improved A-SOA provides an advantage to the designers to calculate the safe margin for their applications. In addition, the total gate charge (Qg) comparison showed that FOM remains unaffected after using ZDI implantation in the P+ body area. The modified device actively can be used as a load switch, fan speed and e-fuse controller, hot swap, battery charger, power management, and automobile's applications.

Acknowledgment

The authors would like to thank T. Lin, Y.-N. Jou, and C.-C. Chen for their valuable technical suggestions. They would also like to thank Vanguard International Semiconductor Corporation for the chip fabrication and measurement support.

References

[1] K. Owyang, C. Bulucea, F.-I. Hshieh, and H. Yilmaz, "Advances in power MOSFET technologies for automotive applications," in *Proc. Automot. Power Electron.*, Jan. 1989, pp. 9–14. doi: 10.1109/APE.1989.97148.

[2] G. Moxey, "New developments in power conversion techniques for low voltage applications," in *Proc. IEE Colloq. Recent Adv. Power Devices*, Jun. 1999, p. 3. doi: 10.1049/ic:19990593.

[3] C. Hu, "Device challenges and opportunities," in *Symp. VLSI Technol., Dig. Tech. Papers*, Jun. 2004, pp. 4–5. doi: 10.1109/VLSIT.2004.1345359.

[4] B. J. Baliga, *Modern Power Devices*, New York, NY, USA: Wiley, 1977.

[5] G. Van den Bosch, P. Moens, P. Gassot, D. Wojciechowski, and G. Groeseneken, "Analysis and application of energy capability characterization methods in power MOSFETs," in *Proc. 30th Eur. Solid-State Circuits Conf.*, Sep. 2004, pp. 453–456. doi: 10.1109/ESSDER.2004.1356589.

[6] C. Buttay, T. B. Salah, D. Bergogne, B. Allard, H. Morel, and J.-P. Chante, "Avalanche behavior of low-voltage power MOSFETs," *IEEE Power Electron. Lett.*, vol. 2, no. 3, pp. 104–107, Sep. 2004. doi: 10.1109/LPEL.2004.839638.

[7] O. Alatise *et al.*, "The impact of repetitive unclamped inductive switching on the electrical parameters of low-voltage trench power nMOSFETs," *IEEE Trans. Electron Devices*, vol. 57, no. 7, pp. 1651–1658, Jul. 2010. doi: 10.1109/TED.2010.2049062.

[8] V. d'Alessandro, L. La Spina, N. Rinaldi, and L. K. Nanver, "SOA reduction due to combined electrothermal and avalanche effects in multifinger bipolar transistors," in *Proc. IEEE Bipolar/BiCMOS Circuits Technol. Meeting*, Oct. 2008, pp. 85–88. doi: 10.1109/BIPOL.2008.4662718.

[9] K. Nidhi, M.-D. Ker, T. Lin, and J.-H. Lee, "Improving safe-operating-area of a 5-V n-channel large array MOSFET in a 0.15-μm BCD process," *IEEE Trans. Electron Devices*, vol. 65, no. 7, pp. 2948–2956, Jul. 2018. doi: 10.1109/TED.2018.2838545.

[10] C. Buttay, O. Brevet, B. Allard, D. Bergogne, and H. Morel, "Paralleling of low-voltage MOSFETs operating in avalanche conditions," in *Proc. Eur. Conf. Power Electron. Appl.*, Sep. 2005, pp. 1–9. doi: 10.1109/EPE.2005.219271.

[11] K. Fischer and K. Shenai, "Dynamics of power MOSFET switching under unclamped inductive loading conditions," *IEEE Trans. Electron Devices*, vol. 43, no. 6, pp. 1007–1015, Jun. 1996. doi: 10.1109/16.502137.

[12] Y. S. Chung and B. Baird, "Electrical-thermal coupling mechanism on operating limit of LDMOS transistor," in *IEDM Tech. Dig.*, Dec. 2000, pp. 83–86. doi: 10.1109/IEDM.2000.904264.

[13] J. B. Steighner and J.-S. Yuan, "The effect of SOA enhancement on device ruggedness under UIS for the LDMOSFET," *IEEE Trans. Device Mater. Rel.*, vol. 11, no. 2, pp. 254–262, Jun. 2011. doi: 10.1109/TDMR.2011.2121068.

[14] F. F. Oettinger, D. L. Blackburn, and S. Rubin, "Thermal characterization of power transistors," *IEEE Trans. Electron Devices*, vol. 23, no. 8, pp. 831–838, Aug. 1976. doi: 10.1109/T-ED.1976.18495.

[15] R. R. Stoltenburg, "Boundary of power-MOSFET, unclamped inductive-switching (UIS), avalanche-current capability," in *Proc. 4th Annu. IEEE Appl. Power Electron. Conf. Expo.*, Mar. 1989, pp. 359–364. doi: 10.1109/APEC.1989.36987.

[16] T. Ye and K. W. A. Chee, "Ruggedness evaluation and design improvement of automotive power MOSFETs," in *Proc. 17th Int. Symp. Qual. Electron. Des.*, Mar. 2016, pp. 211–214. doi: 10.1109/ISQED.2016.7479202.

[17] W.-Y. Chen and M.-D. Ker, "Characterization of SOA in time domain and the improvement techniques for using in high-voltage integrated circuits," *IEEE Trans. Device Mater. Rel.*, vol. 12, no. 2, pp. 382–390, Jun. 2012. doi: 10.1109/TDMR.2012.2187450.

[18] V. Khemka, V. Parthasarathy, R. Zhu, and A. Bose, "Correlation between static and dynamic SOA (energy capability) of RESURF LDMOS devices in smart power technologies," in *Proc. 14th Int. Symp. Power Semiconductor Devices (ICs)*, Jun. 2002, pp. 125–128. doi: 10.1109/ISPSD.2002.1016187.

[19] H. Wang *et al.*, "A floating RESURF EDMOS with enhanced ruggedness and safe operating area," in *Proc. IEEE Conf. Electron Devices Solid-State Circuits*, Dec. 2007, pp. 279–282. doi: 10.1109/EDSSC.2007.4450116.

[20] R. K. Williams, W. Grabowski, M. Darwish, M. Chang, H. Yilmaz, and K. Owyang, "A 1 million-cell 2.0-mΩ 30-V TrenchFET utilizing 32 Mcell/in^2 density with distributed voltage clamping," in *IEDM Tech. Dig.*, Dec. 1997, pp. 363–366. doi: 10.1109/IEDM.1997.650400.

[21] S.-S. Kim, C.-M. Yun, Y.-I. Choi, and M.-K. Han, "A new 600V PT-IGBT for the improved avalanche energy by employing the floating p-well," in *Proc. IEEE 15th Int. Symp. Power Semiconductor Devices (ICs)*, Apr. 2003, pp. 71–74. doi: 10.1109/ISPSD.2003.1225233.

[22] J. Zeng and C. F. Wheatley, "An improved power MOSFET using a novel split well structure," in *Proc. 11th Int. Symp. Power Semiconductor Devices (ICs)*, May 1999, pp. 205–208. doi: 10.1109/ISPSD.1999.764098.

[23] C. Kocon, J. Zeng, and R. Stokes, "Implant spacer optimization for the improvement of power MOSFETs' unclamped inductive switching (UIS) and high temperature breakdown," in *Proc. 12th Int. Symp. Power Semiconductor Devices (ICs)*, May 2000, pp. 157–160. doi: 10.1109/ISPSD.2000.856795.

[24] F. Alagi, L. Labate, A. Andreini, and C. Contiero, "Sub-millisecond energy handling capability improvement of IC power devices with thick copper metallization," in *Proc. IEEE 15th Int. Symp. Power Semiconductor Devices (ICs)*, Apr. 2003, pp. 249–252. doi: 10.1109/ISPSD.2003.1225275.

[25] J. Chen, L. Radic, and T. Henson, "Suppressing channel-conduction during dynamic avalanche to improve high density power MOSFET ruggedness and reverse recovery softness," in *Proc. 25th Int. Symp. Power Semiconductor Devices IC's*, May 2003, pp. 321–324. doi: 10.1109/ISPSD.2013.6694413.

[26] J. Yedinak, R. Stokes, D. Probst, S. Kim, A. Challa, and S. Sapp, "Avalanche instability in oxide charge balanced power MOSFETs," in *Proc. IEEE 23rd Int. Symp. Power Semiconductor Devices (ICs)*, May 2011, pp. 156–159. doi: 10.1109/ISPSD.2011.5890814.

[27] J. C. W. Ng *et al.*, "A novel low-voltage trench power MOSFET with improved avalanche capability," in *Proc. 22nd Int. Symp. Power Semiconductor Devices (ICs)*, Jun. 2010, pp. 201–204.

[28] A. Narazaki, K. Takano, K. Oku, H. Hamachi, and T. Minato, "A marvelous low on-resistance 20V rated self alignment trench MOSFET (SAT-MOS) in a 0.35μm LSI design rule with both high forward blocking voltage yield and large current capability," in *Proc. 16th Int. Symp. Power Semiconductor Devices (ICs)*, May 2004, pp. 393–396. doi: 10.1109/WCT.2004.240223.

[29] "Unclamped inductive switching rugged MOSFETs for rugged environments," Vishay Siliconix, Itzehoe, Germany, Appl. Note AN601, 1994. [Online]. Available: https://www.vishay.com/docs/70572/70572.pdf

[30] "Unclamped inductive switching (UIS) test and rating methodology," Renesas Electron. Corp., Tokyo, Japan, Appl. Notes AN1968, Nov. 2015. [Online]. Available: https://www.renesas.com/tw/zh/www/doc/application-note/an1968.pdf

[31] *Single Pulse Unclamped Inductive Switching (UIS) Avalanche Test Method*, Standard JESD 24-5, JEDEC, Oct. 2002.

[32] J.-H. Lee *et al.*, "Physics of SOA degradation phenomena in power transistors under ESD conditions," in *Proc. Elect. Overstress/Electrostatic Discharge Symp. (EOS/ESD)*, Sep. 2016, pp. 1–9. doi: 10.1109/EOSESD.2016.7592561.

[33] F. Iannuzzo, C. Abbate, and G. Busatto, "Instabilities in silicon power devices: A review of failure mechanisms in modern power devices," *IEEE Ind. Electron. Mag.*, vol. 8, no. 3, pp. 28–39, Sep. 2014. doi: 10.1109/MIE.2014.2305758.

[34] R. J. E. Hueting, E. A. Hijzen, A. Heringa, A. W. Ludikhuize, and M. A. A. Zandt, "Gate-drain charge analysis for switching in power trench MOSFETs," *IEEE Trans. Electron Devices*, vol. 51, no. 8, pp. 1323–1330, Aug. 2004. doi: 10.1109/TED.2004.832096.