ESD Protection Design With Diode-Triggered Quad-SCR for Separated Power Domains

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***Abstract*—To effectively protect the interface circuit between separated power domains from electrostatic discharge (ESD) damage, a new diode-triggered quad-silicon-controlled rectifier (DTQSCR) is proposed and realized in a 0.18-μm 1.8-V/3.3-V CMOS process. Since the DTQSCR embeds four silicon-controlled rectifier paths and a structure of back-to-back diodes, the silicon area can be efficiently reduced more than 30% as compared to the traditional ESD protection design under the same ESD specification. From the measurement results in silicon chip, an interface circuit (level shifter) with the proposed ESD protection design can successfully sustain a human-body-model of greater than 5.5 kV. The proposed ESD protection device is suitable to protect the interface circuits between different power domains.**

***Index Terms*—Electrostatic discharge (ESD), ESD protection, separated power domains, silicon-controlled rectifier (SCR).**

I. Introduction

With the development of integrated circuits (ICs) toward system-on-chip (SoC) applications, more multiple separated power domains have become evident in commercial IC for specified circuit functions, such as mixed-signal IC. Besides, reliability requirements such as electrostatic discharge (ESD) for IC products also have become more critical [1], [2]. Unfortunately, the interference circuits across the separated power domains are very sensitive to ESD events. Unexpected current paths during ESD stress had been reported to cause damage on the interface circuit between the separated power domains [3]–[5]. To sustain the required ESD specification, such as 1 kV in the human-body model (HBM) [6], [7], several different approaches to avoid ESD damages on the interface circuits had been reported [8]–[11]. The typical ESD protection scheme for integrated circuits with separated power domains is shown in Fig. 1. Each power domain has an independent power-rail ESD clamp circuit, typically a gate-grounded NMOS (GGNMOS) [12], [13] or a silicon-controlled rectifier (SCR) [14], [15]. In addition, the back-to-back diodes are used to connect the separated ground lines (V_{SS1} and V_{SS2}) to provide ESD discharge current paths across the separated power domains. When ESD zaps across the separated power-to-ground pins, for example, V_{DD1} to V_{SS2}, the ESD current will be discharged from power-rail ESD clamp circuit 1, and then flows through the back-to-back diodes to V_{SS2}. This long current path may create a large voltage drop to induce damage on the interface circuits. Moreover, since more multiple separated power domains are implemented on the SoC chip, the whole-chip ESD protection design has become increasingly complex. Therefore, the ESD protection structure for the separated power domains should be integrated to reduce the complexity of circuit layout and to save the silicon area.

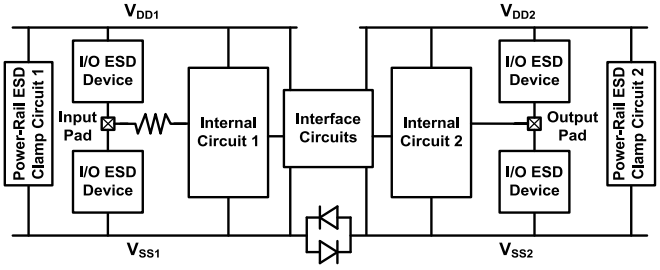

Fig. 1. Traditional ESD protection scheme used to protect the integrated circuits with separated power domains.

To provide more efficient ESD current path between separated power domains, a new power-rail ESD clamp circuit that includes four ESD current discharge paths and two embedded back-to-back diodes is shown in Fig. 2. A special device called quad-silicon-controlled rectifier (QSCR) has been proposed to meet this requirement [16]. However, the characteristics of QSCR such as trigger voltage (V_{t1}) and layout area should be further improved. In this work, a modified diode-triggered quad-silicon-controlled rectifier (DTQSCR) is proposed to overcome the internal ESD damage on the interface circuits and meliorate the ESD protection performance of QSCR.

The purpose of this study was to examine whether the use of DTQSCR will effectively protect the interface circuit against cross-power-domain positive HBM ESD stress. Since SCR is a unidirectional device, a reverse diode must be added between V_{DD} and V_{SS} to discharge the ESD current under the negative HBM ESD stress. The proposed ESD devices and a level shifter as the interface circuit are fabricated in 0.18-μm 1.8-V/3.3-V CMOS process. By using the diode trigger mechanism, the trigger voltage (V_{t1}) and layout area can

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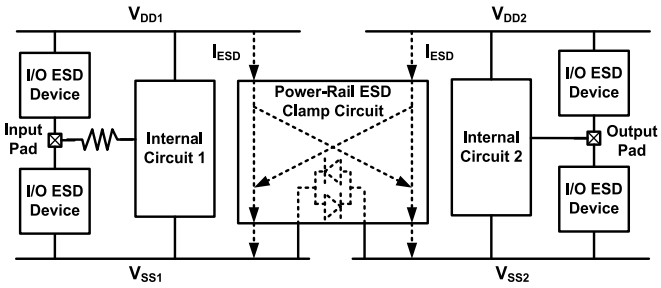
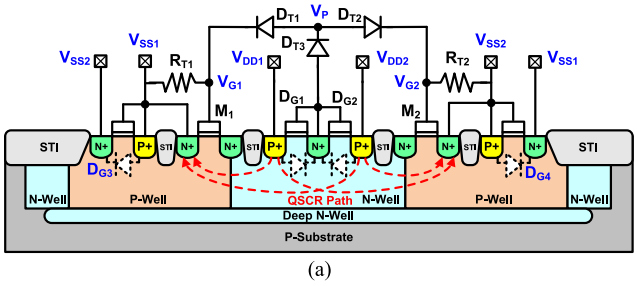
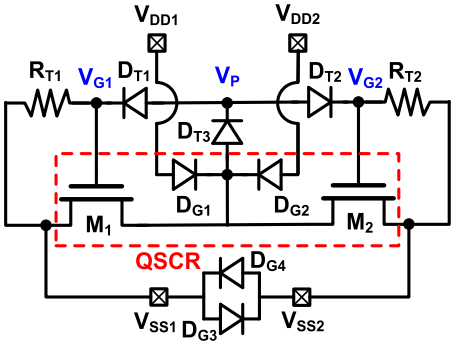


Fig. 2. Proposed ESD protection scheme to protect the integrated circuits with separated power domains. Interface circuit is not shown.



(a)



(b)

Fig. 3. (a) Device cross-sectional view and (b) equivalent circuit of the proposed DTQSCR.

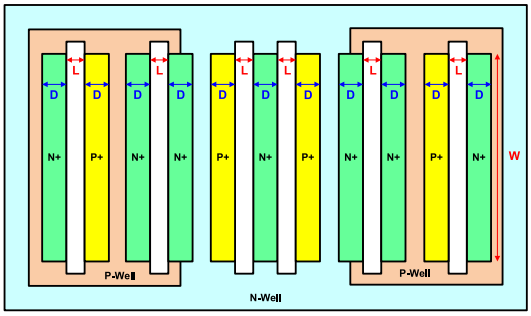


Fig. 4. Device top layout view of the proposed DTQSCR.

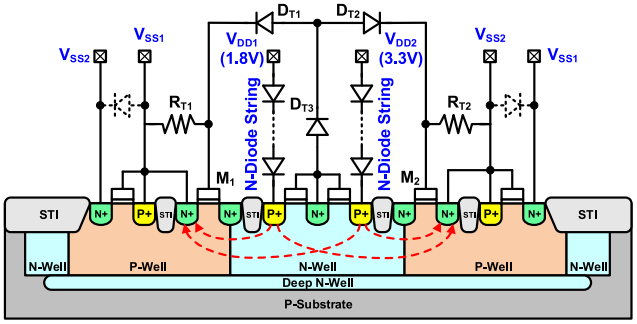


Fig. 5. Device cross-sectional view of the proposed DTQSCR with diode strings for 1.8-V/3.3-V applications.

be efficiently reduced. As comparing to the traditional ESD protection scheme with GGNMOS, the proposed ESD protection design for the integrated circuits with separated power domains has been successfully verified in silicon test chip to sustain a HBM ESD level of greater than 5.5 kV.

II. Proposed ESD Protection Design

A. Circuit Implementation

Fig. 3(a) shows the cross-sectional view of the proposed DTQSCR, which includes a deep n-well, two p-wells, and three n-wells. The deep n-well is used to connect three n-wells to isolate two p-wells from the p-substrate. The n-well has two butting gated diodes (D_{G1} and D_{G2}) [17], [18], which have a gate structure with both p+ and n+ implantations between the anode and cathode of the diode structure. The p+ regions of D_{G1} and D_{G2} are connected to V_{DD1} and V_{DD2}, respectively. To form QSCR path, two NMOS-like configurations (M_1 and M_2) are inserted into the interface between n-well and p-well to construct a similar structure with low-voltage triggering SCR (LVTSCR) [19]–[21]. There are a total of four parasitic SCR paths between the two positive terminals (V_{DD1} and V_{DD2}) and the two negative terminals (V_{SS1} and V_{SS2}). Adding a suitable trigger circuit to reduce the trigger voltage of SCR has been popular in ESD protection design [22], [23]. The three trigger diodes (D_{T1}, D_{T2}, and D_{T3}) connected like a T-network are used to trigger on the M_1 and M_2 to turn on the parasitic SCR [24], [25]. To integrate the back-to-back diodes in DTQSCR, two gated diodes (D_{G3} and D_{G4}) are embedded into two p-wells, respectively. To simulate the trigger characteristic of the proposed ESD protection design, an equivalent circuit of DTQSCR is shown in Fig. 3(b), where the SCR paths are not shown. The top layout view of DTQSCR without trigger diodes is shown in Fig. 4. In this work, the width (W) of the DTQSCR and each diode are selected as 50 μm. The gate length (L = 1 μm) and junction length (D =3.1μm) of each device are the same. The resistors (R_{T1} and R_{T2}) connected to trigger diodes (D_{Tn}) are selected as 100 kΩ to reduce the standby leakage current. All design parameters are listed in Table I.

Using SCR as the ESD protection device should consider the latchup concern [26]. To avoid the latchup issue, the holding voltage of SCR must be higher than the power supply voltage. Hence, two diode strings are connected to the DTQSCR to increase the holding voltage of DTQSCR, as shown in Fig. 5. Since this work is fabricated in a 1.8-V/3.3-V CMOS process, the holding voltage for the low-voltage domain and high-voltage domain must be higher than 1.8 V and 3.3 V, respectively. Several test circuits are also listed in Table I. The test patterns include the GGNMOS, test A, test B, and test C. Test circuit A is the DTQSCR

TABLE I
DESIGN PARAMETERS OF THE ESD PROTECTION CIRCUITS

	GGNMOS	Test A	Test B	Test C
W/L (μm/μm)	500/0.35	50/1	50/1	50/1
Resistor R_{Tn} (Ω)	none	100k	100k	100k
Junction Length D (μm)	6.2	3.1	3.1	3.1
Additional diode number on V_{DD1}	none	0	1	2
Additional diode number on V_{DD2}	none	0	3	4
Device total area (μm^2)	3931	4110	5718	6640
Each diode dimension	W=50 μm, D=3.1 μm			

without the diode string on V_{DD1} and V_{DD2}. The test circuit B has the DTQSCR with one additional diode on V_{DD1} and three additional diodes on V_{DD2}, whereas the test circuit C has the DTQSCR with two additional diodes on V_{DD1} and four additional diodes on V_{DD2}.

B. Circuits Simulation

1) ESD-Like Waveform Condition: To simplify the circuit simulation, the test circuit B is selected to simulate the function of DTQSCR. In the simulation with ESD-like waveform, the rise time of 10 ns and the pulse width of 100 ns are selected as a typical HBM event. Since the normal operation voltage is 3.3 V on high-voltage domain, a high voltage of 5 V is selected as the ESD-like pulse to investigate the triggering on operation of the proposed design before the devices get into breakdown.

Fig. 6 shows the simulated voltages of transient waveform on each node of the proposed test circuit B. In Fig. 6(a), under the same-power-domain ESD stress condition, when the ESD voltage is applied on V_{DD1} with V_{SS1} grounded, the high voltage of the ESD pulse will turn on the diode string to trigger on the M_1 and M_2. In other words, the ESD current will first flow through the diode string and the trigger diodes to the node V_P. The partial current then flows through the D_{T1} and R_{T1} to the V_{SS1}, and another also flows through the D_{T2}, R_{T2}, and back-to-back diode to V_{SS1}. The voltage drop on the resistors will trigger on the M_1 and M_2 to discharge the ESD current. Since the I_{M1} is larger than I_{M2}, the parasitic SCR path under the M_1 will be first triggered on to conduct the main ESD current. Then, this current also turns on the parasitic SCR path under the M_2. Both SCR paths are in the on-state to discharge the ESD current.

In Fig. 6(b), under the cross-power-domain ESD stress condition, when the ESD voltage is applied on V_{DD1} and V_{SS2} grounded, the transient current will flow through the R_{T1} and R_{T2} to charge up the gate voltages of the M_1 and M_2. Under this condition, both SCR paths from V_{DD1} to V_{SS2} will be triggered on to conduct the main ESD current. The circuit operational mechanism is the same, when the ESD pulse is applied on V_{DD2} and V_{SS1} or V_{SS2} grounded.

2) Normal Power-On Condition: Under the normal power-on condition, the V_{DD1} (1.8V) and V_{DD2} (3.3V) power-on waveforms have a rise time in the range of milliseconds (ms) and a low level voltage. Fig. 7 shows the simulated voltages at each node of the proposed circuit under normal power-on condition. Since both normal power-on voltages are lower than the turn-on voltage of the diode string, both M_1 and M_2 are kept in off-state. Therefore, the SCR path can be kept off under normal power-on condition.

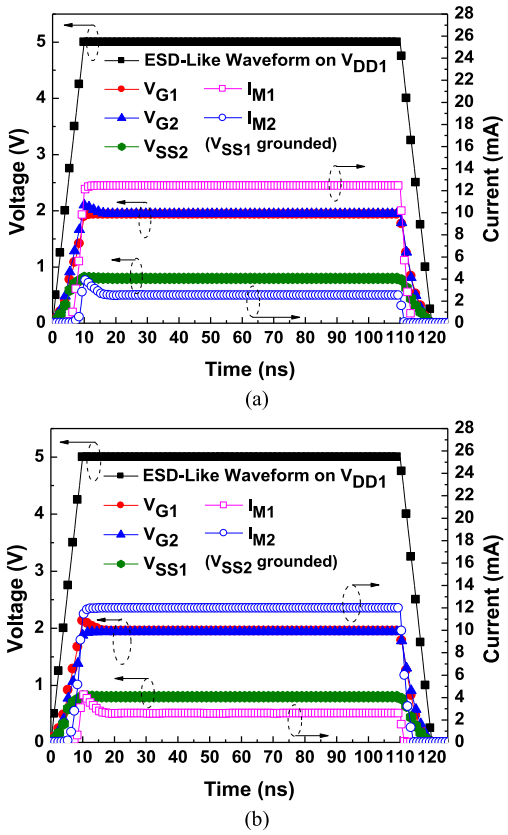


Fig. 6. Simulation results of the voltage on each node of the proposed DTQSCR during (a) the positive V_{DD1}-to-V_{SS1} ESD-like waveform condition, and (b) the positive V_{DD1}-to-V_{SS2} ESD-like waveform condition.

III. EXPERIMENTAL RESULTS OF TEST CIRCUITS

The proposed circuits studied in this work are implemented in a 0.18-μm 1.8-V/3.3-V CMOS process. The additional diodes in diode string are realized by the traditional p+/n-well diode, and its junction area is drawn as 50 × 3.1 μm^2. To compare with the proposed circuits, traditional ESD clamp is implemented by the GGNMOS with device dimension (W/L) of 500 μm/0.35 μm.

A. Transmission Line Pulsing (TLP) Measurement

To investigate the device behavior during ESD transient pulse, a transmission-line-pulsing (TLP) generator gave a waveform with pulse width of 100 ns and rising time of 10 ns as a typical HBM event. Fig. 8 and Fig. 9 show the comparison of TLP I-V curves among all test circuits under the same-power- domain and cross-power-domain ESD stress conditions. By adding the diode string on V_{DD1} and V_{DD2} (Test B and Test C), the trigger voltage (V_{t1}) is increased proportionally with the number of stacked diodes: up to 5.5, 6.3, 7, and 7.9 V for the one-, two-, three- and four-stacked diodes, respectively. The second breakdown current (I_{t2}) of the

TABLE II
MEASURED RESULTS OF GGNMOS AND PROPOSED CIRCUITS UNDER SAME-DOMAIN ESD TEST

Test condition	Positive V_{DD1}-to-V_{SS1}				Positive V_{DD2}-to-V_{SS2}			
Test Circuit	GGNMOS	Test A	Test B	Test C	GGNMOS	Test A	Test B	Test C
V_{t1} (V)	8.9	4.3	5.5	6.3	8.9	4.3	7.0	7.9
V_h (V)	6.1	2.1	3.4	4.4	6.1	2.1	5.5	6.5
I_{t2} (A)	3.8	6.7	6.3	6	3.8	6.7	5.8	5.3
R_{on} (Ω)	4.29	5.0	5.5	5.97	4.29	5.0	6.0	6.38
HBM (kV)	5.5	>8	>8	>8	5.5	>8	>8	>8

TABLE III
MEASURED RESULTS OF GGNMOS AND PROPOSED CIRCUITS UNDER CROSS-DOMAIN ESD TEST

Test condition	Positive V_{DD1}-to-V_{SS2}				Positive V_{DD2}-to-V_{SS1}			
Test Circuit	GGNMOS	Test A	Test B	Test C	GGNMOS	Test A	Test B	Test C
V_{t1} (V)	9.7	4.3	5.6	6.4	9.7	4.3	7.2	8.1
V_h (V)	7.3	2.5	3.8	4.8	7.3	2.5	5.9	6.9
I_{t2} (A)	3.7	6.6	6	5.8	3.7	6.6	5.6	5.3
R_{on} (Ω)	6.43	5.04	5.53	6.02	6.43	5.04	6.17	6.5
HBM (kV)	5.5	>8	>8	>8	5.5	>8	>8	>8

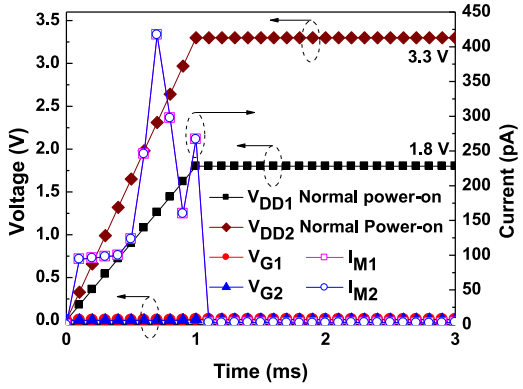


Fig. 7. Simulated results of the voltage on each node of the proposed DTQSCR under normal power-on condition.

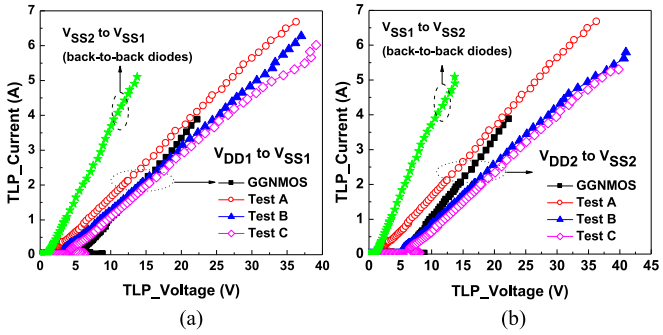


Fig. 8. TLP measured I-V characteristics of GGNMOS and DTQSCRs under (a) positive V_{DD1}-to-V_{SS1} and (b) positive V_{DD2}-to-V_{SS2} test condition. Both figures contain TLP measured I-V curve of back-to-back diodes.

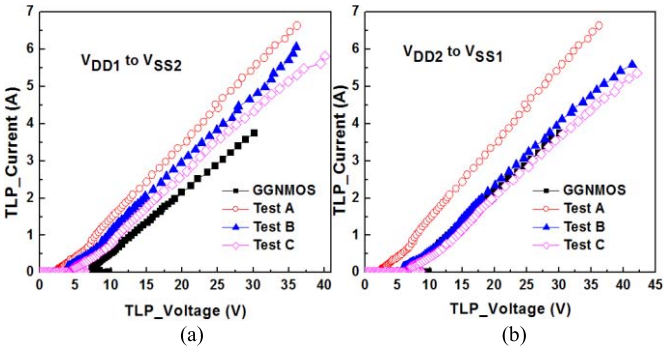


Fig. 9. TLP measured I-V characteristics of GGNMOS and DTQSCRs under (a) positive V_{DD1}-to-V_{SS2} and (b) positive V_{DD2}-to-V_{SS1} test condition.

proposed circuits under each test condition is all higher than 5.5 A, but that of the GGNMOS is lower than 4 A. However, when the number of diodes in diode string is increased, the I_{t2} of proposed circuits is degraded. Due to the high holding voltage caused by the diode string, the number of diodes in the diode string should be carefully designed to meet the application request. In this work, for 1.8-V/3.3-V application, the holding voltage for the low- voltage domain and high-voltage domain must be higher than 1.8 V and 3.3 V, respectively, to avoid the latchup issue. According to the measurement results, the test circuit B is the suitable one for this 1.8-V/3.3-V application. In addition, the TLP I-V curves under ground-to-ground test condition (back-to-back diodes) are also included in Fig. 8. All these measurement results are listed in Table II and Table III.

B. ESD Robustness

The HBM tester is used to verify the ESD robustness of the fabricated circuits. The ESD pulses are stressed to each test circuit under positive V_{DD1}-to-V_{SS1}, positive V_{DD1}-to-V_{SS2}, positive V_{DD2}-to-V_{SS1}, and positive V_{DD2}-to-V_{SS2} ESD stress conditions. The failure criterion is defined as the I-V characteristics of the circuit shifting more than 30% from its initial curve after each ESD test level. All the DTQSCR test circuits can sustain more than 8 kV HBM ESD level under each test condition, but the GGNMOS with a device size (W) of 500 μm can only sustain the ESD level of 5.5 kV. The HBM

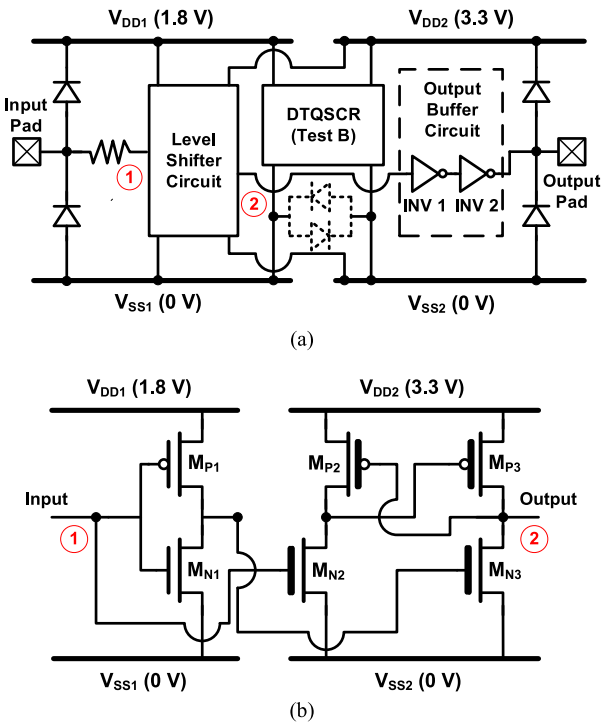


Fig. 10. (a) Test circuit used to verify the protection effectiveness of the proposed ESD protection design (DTQSCR of test B) for the interface circuit (level shifter circuit) across the separated power domains, and (b) the circuit implementation of level shifter circuit across the separated power domains.

test results among all test circuits are also listed in Table II and Table III.

C. Application and Verification

To verify the ESD protection effectiveness of the DTQSCR for interface circuit across the separated power domains, a level shifter with the ESD protection design of test B is especially implemented in Fig. 10(a). In additional to the DTQSCR, the ESD protection device for I/O port is realized by a p+/n-well diode. The circuit implementation of level shifter, as shown in Fig. 10(b), is used to convert the logic signals of low-level voltage (1.8 V) to the high-level voltage (3.3 V). To confirm the circuit function, the test circuit can be verified by applying a signal at the input pad (with the power domain of V_{DD1} and V_{SS1}) and measuring the output waveform (with the power domain of V_{DD2} and V_{SS2}). During the verification procedure, the V_{DD1} and V_{DD2} are biased at 1.8 V and 3.3 V, respectively, whereas the V_{SS1} and V_{SS2} are both grounded. A pulse generator connected to input pad is used to give a 500-kHz periodic waveform to the test circuit. The input signal and output waveform of the test circuit are monitored by the oscilloscope. The measured results of the test circuit before ESD stress are shown in Fig. 11(a). Since the interface circuit across the separated power domains was often damaged under cross-power-domain ESD stresses, the measured results after the cross-power-domain ESD stress conditions (positive V_{DD1}-to-V_{SS2} and positive V_{DD2}-to-V_{SS1}) are monitored in Figs. 11(b) and 11(c). In Fig. 11(b), due to the damage of inverter (M_{P1} and M_{N1}) in the low-voltage domain,

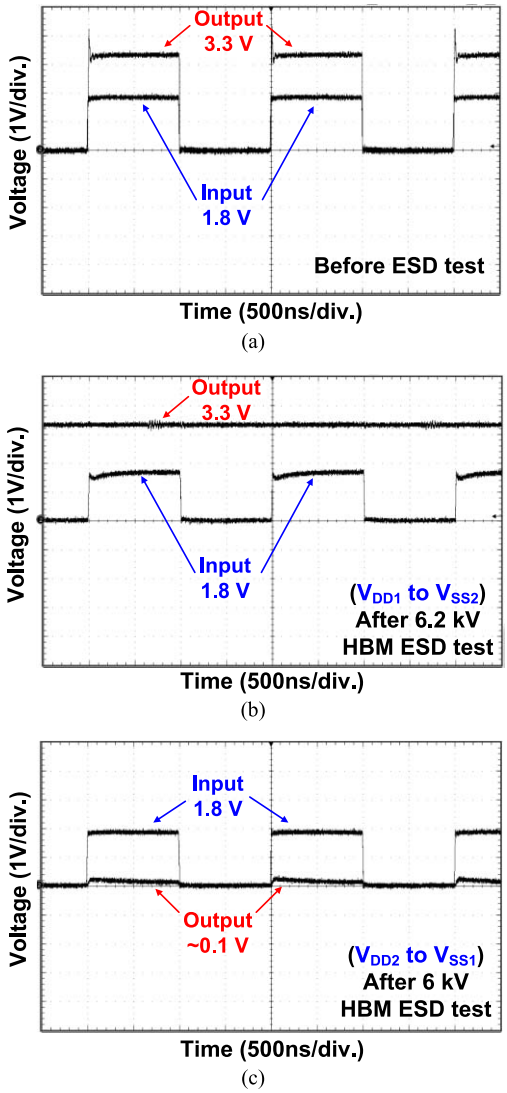


Fig. 11. Measured voltage waveforms of a level shifter across the separated power domains that protected by the proposed ESD protection design of test B, (a) before ESD test, (b) after 6.2 kV positive V_{DD1}-to-V_{SS2} HBM stress, and (c) after 6 kV positive V_{DD2}-to-V_{SS1} HBM stress.

the waveform of the input signal is distorted, and the output signal is always kept at 3.3 V. In Fig. 11(c), the results show no degradation on input signal waveform, but the output signal is clamped to $\sim$ 0.1 V, where the NMOS in the output buffer circuit (INV 2) was damaged.

Besides, a level shifter with traditional ESD protection scheme realized by GGNMOS as power-rail ESD clamp is also implemented in the same test chip, as shown in Fig. 12. After the cross-power-domain ESD stress (positive V_{DD1}-to-V_{SS2} and positive V_{DD2}-to-V_{SS1}), the measured waveforms of the traditional ESD protection scheme are similar to that in Figs. 11(b) and 11(c). The failure point in the traditional ESD protection scheme is almost the same as that of the proposed circuit. All the test results are listed in Table IV. The ESD robustness of the test circuit can be judged by the lowest level among the four modes of ESD test condition. Therefore, the HBM ESD robustness of a level shifter with proposed ESD protection design of test B and a level shifter

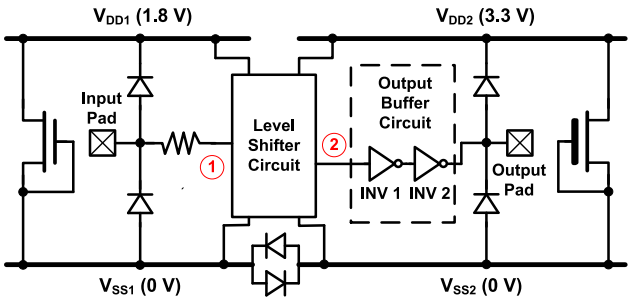


Fig. 12. Test circuit used to verify the protection effectiveness of the GGNMOS for the interface circuit (level shifter circuit) across the separated power domains.

TABLE IV
MEASURED RESULTS OF THE INTERFACE CIRCUIT WITH DIFFERENT ESD PROTECTION DESIGNS

	A level shifter protected by traditional GGNMOS	A level shifter protected by the proposed design of Test B
Total Layout Area (μm^2)	13253	10423
ESD Stress	HBM (kV)	
V_{DD1}-to-V_{SS1}	5.2	6
V_{DD1}-to-V_{SS2}	5	6
V_{DD2}-to-V_{SS1}	5	5.8
V_{DD2}-to-V_{SS2}	5.2	5.8
FOM (V/μm^2)	**0.38**	**0.56**

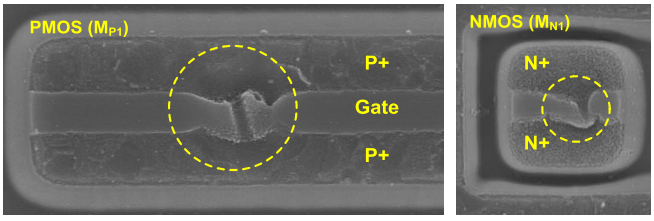


Fig. 13. SEM photograph on the level shifter protected by the proposed design (test B) after 6.2-kV V_{DD1}-to-V_{SS2} HBM ESD stress. Failures are located both on the M_{P1} and M_{N1} of the level shifter.

with the traditional ESD protection design of GGNMOS is 5.8 and 5 kV, respectively.

D. Failure Analysis

To observe the failure location on the interface circuits after ESD stress, the scanning electron microscope (SEM) experiment was applied. The SEM photograph on the interface circuit that protected by the proposed design (test B) after the positive V_{DD1}-to-V_{SS2} HBM ESD stress of 6.2 kV is shown in Fig. 13. The failure point was found at the M_{P1} and M_{N1} of the level shifter. Since the input pad is floating (that may be coupled to somewhat voltage level due to the parasitic capacitance) under V_{DD1}-to-V_{SS2} ESD stress condition, some ESD current would flow through the channels of M_{P1} and M_{N1} to ground that caused the burned-out results as shown in Fig. 13. Under positive V_{DD2}-to-V_{SS1} HBM ESD stress of 6 kV, the failure point on the interface circuit protected by the proposed design (test B) is only located at the NMOS in the output buffer (INV 2), as shown in Fig. 14. The output buffer has

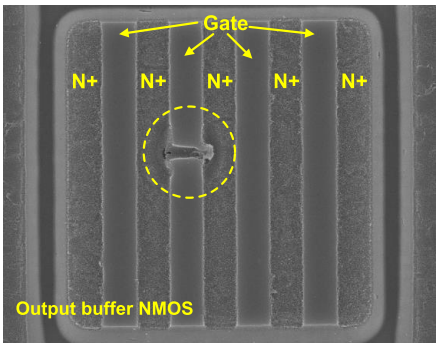


Fig. 14. SEM photograph on the level shifter protected by the proposed design (test B) after 6-kV V_{DD2}-to-V_{SS1} HBM ESD stress. Failure is located on the NMOS in the output buffer (INV 2).

large device dimensions to drive the signal to the output pad, and the PMOS in output buffer typically has a lager dimension (twice size of the NMOS). Therefore, the NMOS in output buffer is burned out before the PMOS under the V_{DD2}-to-V_{SS1} HBM ESD stress of 6 kV.

E. Comparison

The ESD protection circuits are often desired to have high ESD robustness but only occupy small silicon area. Therefore, the figure of merit (FOM) can be expressed as

$$FOM = \frac{HBM}{Area}. \quad (1)$$

where the *Area* is the total layout area of all devices shown in Fig. 10(a) and Fig. 12, respectively. The FOM among the test circuits are compared and shown in Table IV. The FOM's of a level shifter protected by the traditional design (GGNMOS) and that protected by the proposed design (test B) are 0.38 and 0.56 V/μm^2, respectively. With the proposed ESD protection design (test B), under the same HBM ESD level of specification, the silicon area can be efficiently reduced more than 30%, as comparing to that of traditional ESD protection design (GGNMOS).

IV. CONCLUSION

The DTQSCR embedded four SCR paths has been proposed and successfully verified to be an effective ESD protection solution for the interface circuits across separated power domains. By applying the diode-triggering circuit technique, the trigger voltage (V_{t1}) of DTQSCR can be reduced low enough for efficient ESD protection. Comparing to the traditional ESD protection design with GGNMOS, and the FOM (ESD level / layout area) of the proposed design is significantly improved ~47% to protect the interface circuits across separated power domains.

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