Study and Verification on the Latch-Up Path Between I/O pMOS and N-Type Decoupling Capacitors in 0.18-μm CMOS Technology

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***Abstract*—On-chip decoupling capacitors often formed by varactor or nMOS have been widely used to shunt the power-line noise in integrated-circuit products. Because the N+ cathode of these capacitors is connected to ground, an unexpected latch-up path between I/O pMOS and n-type decoupling capacitors may be accidentally triggered on. In this paper, the non-typical latch-up path between I/O pMOS and n-type decoupling capacitors was investigated in 0.18-μm 1.8/3.3-V CMOS technology. The measurement results from the silicon chip with split test structures have verified that the n-type decoupling capacitor near the I/O pMOS can cause a high risk of latch-up. Therefore, the layout rules between the decoupling capacitor and I/O devices should be carefully defined to prevent the occurrence of such an unexpected latch-up path.**

***Index Terms*—Latch-up, decoupling capacitor, varactor, silicon-controlled rectifier (SCR).**

I. Introduction

With the evolution of CMOS technology, both high-voltage (HV) and low-voltage (LV) devices can be integrated together in a single chip to achieve high functionality and more circuit performance. Due to the integration of HV and LV devices, some non-typical latch-up paths may occur to cause unrecoverable failures [1]–[3]. In CMOS ICs, traditional latch-up path is formed by the parasitic silicon-controlled rectifier (SCR) structure between power lines of V_{DD} and V_{SS}. The parasitic SCR may be accidentally triggered on by external glitches to generate a low-impedance path between the power lines [4], [5]. The device cross-sectional view and the equivalent circuit of traditional latch-up path in a p-substrate bulk CMOS technology is shown in Fig. 1. The latch-up equivalent circuit is composed of a vertical p-n-p BJT (Q_{PNP}) coupled with a lateral n-p-n BJT (Q_{NPN}). The latch-up mechanism of positive feedback regeneration will be initiated when one of the BJTs is turned on [6]. It is difficult to block latch-up path thoroughly because a parasitic p-n-p-n path inherently exists in the CMOS technology. To further reduce the probability of latch-up occurrence, there are some advanced technologies those can effectively prevent ICs from latch-up, such as epitaxial substrate [7], retrograde well [8], trench isolation [9], or SOI (silicon on insulator). Even though such advanced techniques are able to make latch-up free, the fabrication cost of CMOS ICs will be obviously increased. Therefore, the common solution of latch-up prevention in the commercial IC products was adopting the guard rings in layout, which surrounded the devices to suppress the occurrence of latch-up event [10], [11].

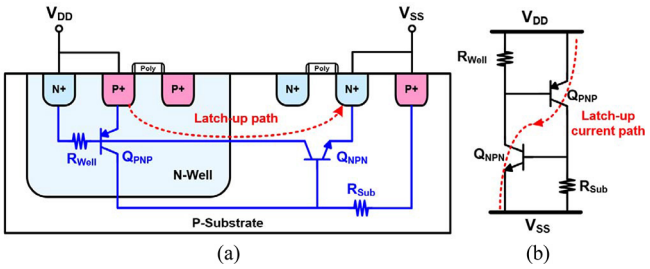

Fig. 1. (a) Device cross-sectional view and (b) equivalent circuit of traditional latch-up structure in a p-substrate bulk CMOS technology.

With the increase on clock frequency for fast computing and the decrease on supply voltage for power saving, IC products have become more sensitive to noise disturbances including power supply noise or switching noise. To reduce power supply noise, on-chip decoupling capacitors are often added into the power distribution networks [12]. One of the common on-chip decoupling capacitors used in CMOS ICs is varactor, which can be considered as an NMOS in N-well, as drawn in Fig. 2(a). As compared with the NMOS capacitor realized in a grounded P-well, the electrons in varactor can be easily accumulated in low-voltage bias without generating the inversion layer to get the *C-V* curve as shown in Fig. 2(b), and the capacitance of varactor is similar to NMOS capacitor when the voltage bias is above V_T.

To utilize this phenomenon, the N+ diffusions drawn in N-well must be grounded. Unfortunately, the N-well with a deep junction depth of ~2 μm may collect more electrons in the p-type substrate. As reported in [3], the p-n-p-n path from the I/O ESD device (PNP BJT) to the decoupling capacitor of varactor was unexpectedly triggered on to cause latch-up

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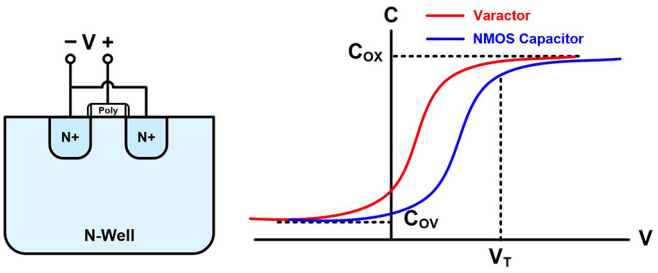


(a) (b)

Fig. 2. (a) The cross-sectional view of varactor and (b) the *C-V* curve of varactor and NMOS capacitor in the p-substrate bulk CMOS technology.

TABLE I
TRIGGER CHARACTERIZATION IN LATCH-UP CURRENT TEST [13]

Latch-Up I-test	Range of Stress	Force Current
Positive I-Test	I	< 50 mA
	II	50 to < 100 mA
	III	100 to < 150 mA
	IV	150 to < 200 mA
	V	>= 200 mA
Negative I-Test	I	> -50 mA
	II	-50 mA to > -100 mA
	III	-100 to > -150 mA
	IV	-150 to > -200 mA
	V	< -200 mA

failure. Therefore, the layout rules on the spacing between the decoupling capacitor and I/O devices should be considered and carefully defined.

To examine the latch-up immunity, methods with positive and negative current tests (I-tests) had been already defined in the Joint Electron Device Engineering Council (JEDEC) standards. The characterization of the trigger current for latch-up I-test specified in JESD78D is listed in Table I [13]. Although the standard JESD78E [14] modified the highest latch-up I-test level back to 100 mA, many companies still improve their IC productions with I-test level of 200 mA against latch-up event for better reliability consideration.

In this work, the latch-up concern between I/O PMOS and varactor with a grounded N-Well was studied and investigated in silicon under different test structures. The layout parameters such as anode-to-cathode spacings and guard-ring width are also verified to seek their impacts on latch-up immunities. Furthermore, the varactor will be replaced with an NMOS capacitor in a grounded P-Well to compare the risk of latch-up. In the experimental measurement, the dc curve tracer (Tek370B) is used to verify the holding voltage (V_{hold}) of each latch-up test structure, and more examinations on latch-up immunity are verified by a commercial latch-up tester.

II. TEST STRUCTURES

The device structure and cross-sectional view of I/O PMOS, varactor, and NMOS capacitor are shown in Fig. 3. The devices verified in this paper are implemented in a 0.18-μm p-substrate bulk CMOS technology. In this work, the drain of I/O PMOS is treated as an injection pin (I/O) of latch-up I-test to simulate the external interference during the normal circuit

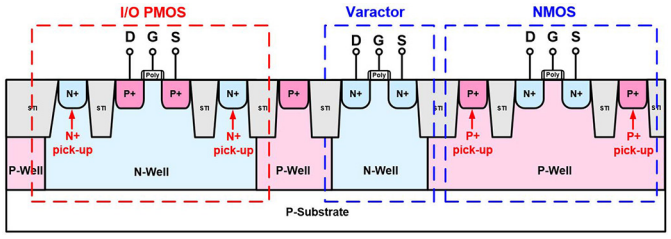


Fig. 3. The cross-sectional view and device structure of I/O PMOS, varactor, and NMOS in a 0.18-μm p-substrate bulk CMOS technology.

operation. In the varactor, the source and drain are connected together and tied to ground to be an on-chip decoupling capacitor, therefore the N-well of the varactor is grounded. The test structures with I/O PMOS drawn close to the varactor with a grounded N-well, or to the NMOS capacitor in a grounded P-Well, are prepared to examine such latch-up issue. By changing their layout parameters, the p-n-p-n latch-up path may become sensitive to external overshooting or undershooting noises. Further, to simply the bias control under measurement, the I/O PMOS and NMOS capacitor in the test structures are kept in off state by connecting its gate to source.

A. Latch-Up Between I/O PMOS and Varactor

The latch-up immunity in the test structure A, composed of I/O PMOS and the varactor with grounded N-Well, has been studied in this work. The layout test parameters include anode-to-cathode spacings (Spacing), guard ring structures, and guard ring width (GW).

The cross-sectional views of the test structure A with different guard ring surroundings are shown in Figs. 4(a) - 4(e) with the split names of type A-1, A-2, A-3, A-4, and A-5, respectively. Test structure A-1 consists of a pair of an I/O PMOS and a varactor without inserting guard ring between them. Test structure A-2 comprises the device pair, and the I/O PMOS is surrounded by an N+ guard ring which is recognized as the base ring for I/O PMOS. Test structure A-3 contains the device pair, and the varactor is surrounded by a P+ guard ring which is recognized as the collect ring for varactor. Test structure A-4 combines the test structures of A-2 and A-3 together, where the I/O PMOS is surrounded by an N+ guard ring, and the varactor is surrounded by a P+ guard ring.

Besides, inserting the double guard rings with grounded p-well ring and V_{DD}-connected n-well ring inside the latch-up path to effectively improve latch-up immunity is one of the most popular solutions. In test structure A-5, two rows of additional guard rings are inserted in the latch-up path between two first guard rings. One of the additional guard ring is P+ type that close to the I/O PMOS, and the other is N+ type that close to the varactor.

B. Latch-Up Between I/O PMOS and NMOS Capacitor

To compare the latch-up issue with the NMOS capacitor, the varactor is replaced by the NMOS capacitor with a grounded P-well in the test structure B. The cross-sectional views of the test structure B with different guard ring surroundings are shown in Figs. 5(a) - 5(e) with the split names of type B-1,

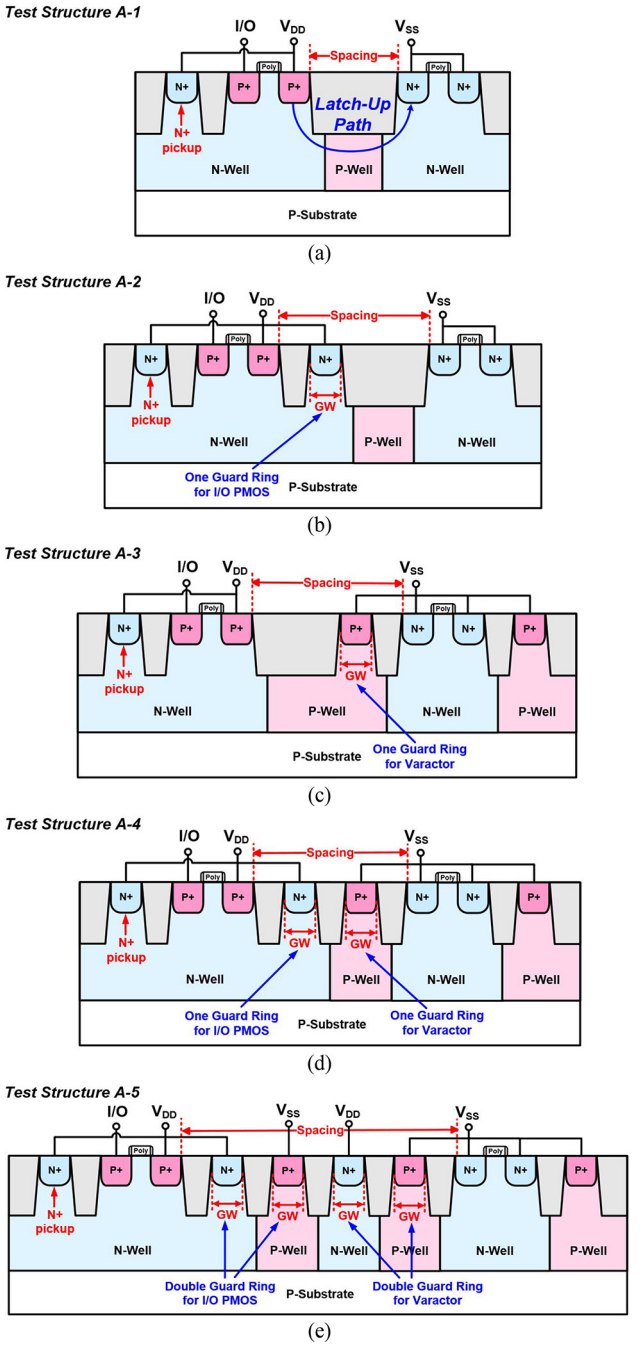


Fig. 4. The cross-sectional views of the test structures (a) A-1, (b) A-2, (c) A-3, (d) A-4, (e) A-5, with a I/O PMOS and a varactor.

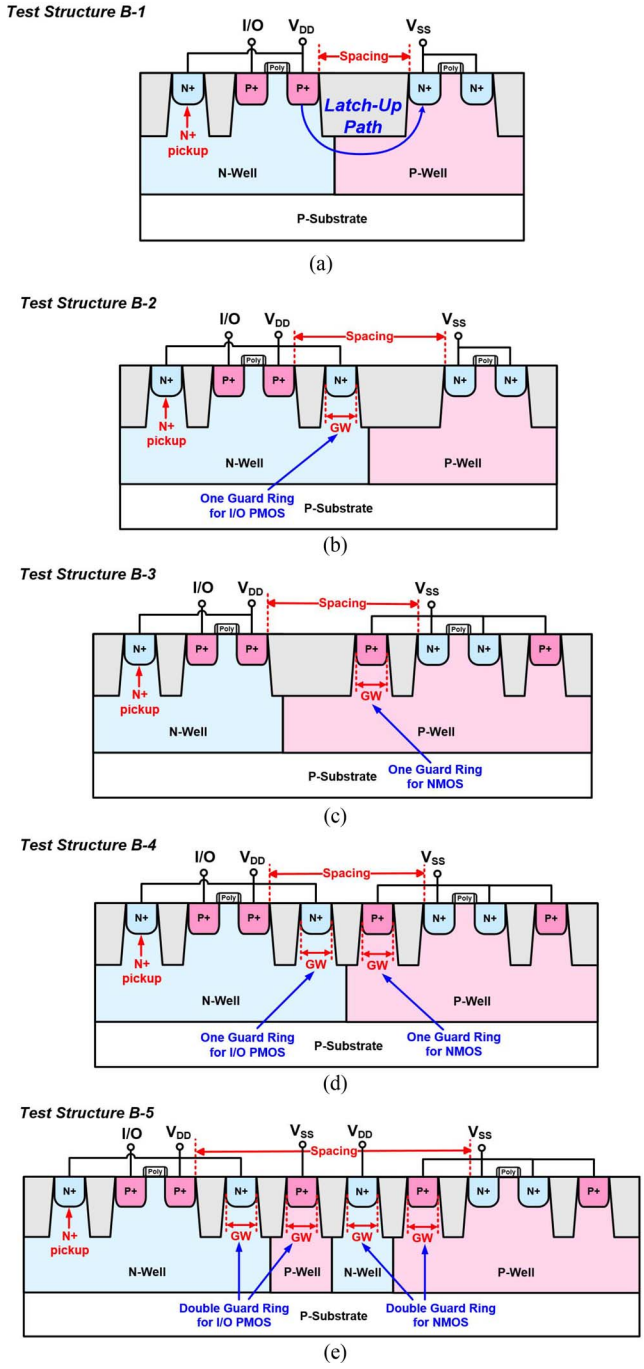


Fig. 5. The cross-sectional views of the test structures (a) B-1, (b) B-2, (c) B-3, (d) B-4, (e) B-5, with an I/O PMOS and an NMOS capacitor.

B-2, B-3, B-4, and B-5, respectively. The split conditions in the layouts of the test structures B-1 ∼ B-5 are similar to those used in the test structures A-1 ∼ A-5. The layout parameters such as guard ring structures, anode-to-cathode spacings, and guard ring width are also investigated in the test structure B.

Fig. 6 shows the simplified layout top views of test structures A and B to illustrate the layout parameters. In order to inject large enough current under latch-up I-test, the dimension of the I/O PMOS with a total channel width of 420 μm is larger than that of the varactor or NMOS, which are drawn with a total channel width of 30 μm.

III. Experimental Results

A. DC I-V Characteristics

The dc I-V characteristics of the test structures to investigate the latch-up characteristics are measured by the Tek370B curve tracer at the room temperature of 25 °C. Based on the latch-up criterion, the latch-up risk cannot be neglected as long as the holding voltage (V_h) of the test structures is lower than V_{DD} (3.3 V). Figs. 7(a) and 7(b) show the *I-V* characteristics of test structures A and B, traced from V_{DD} to V_{SS} with an anode-to-cathode spacing of 12 μm and a guard ring width

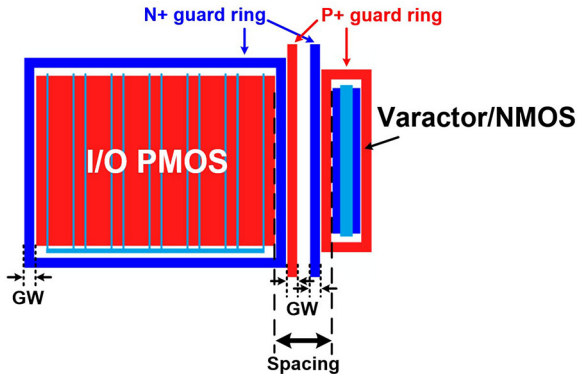


Fig. 6. Simplified layout top view of test structures A and B with related layout parameters.

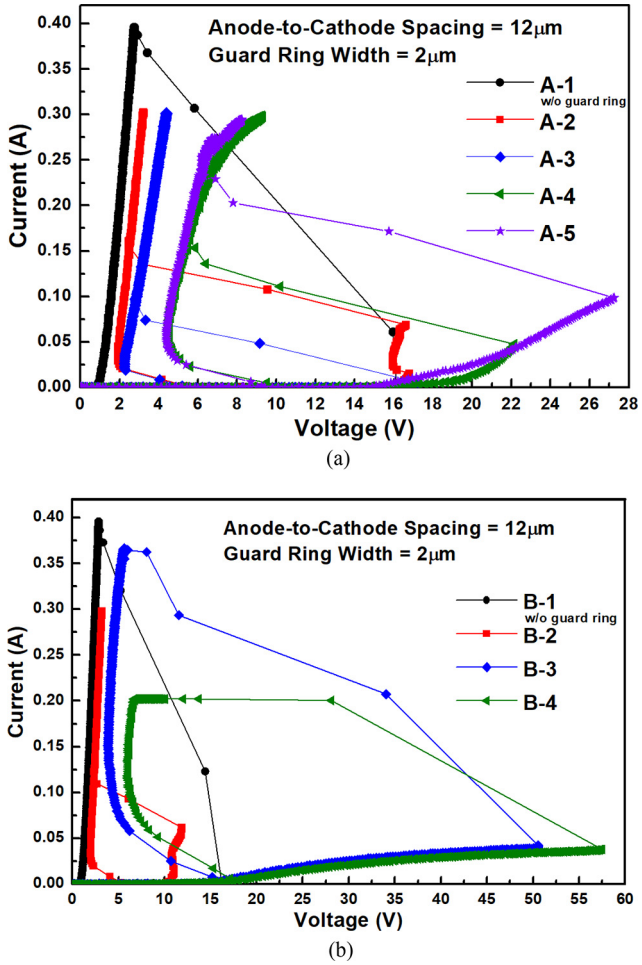


Fig. 7. The measured dc *I–V* characteristics of test structures (a) A and (b) B with an anode-to-cathode spacing of 12 μm and a guard ring width of 2 μm.

of 2 μm. The measured results of the test structures show the obvious snapback phenomenon and bring down the voltage.

Further, to examine the latch-up risk of test structure A, the measured relations between V_h and anode-to-cathode spacings with different types and guard ring widths for test structure A are shown in Fig. 8. In this figure, the V_h of test structures A-1, A-2, and A-3 are lower than V_{DD} (3.3 V) obviously. For test structures A-4 and A-5 with an anode-to-cathode spacing

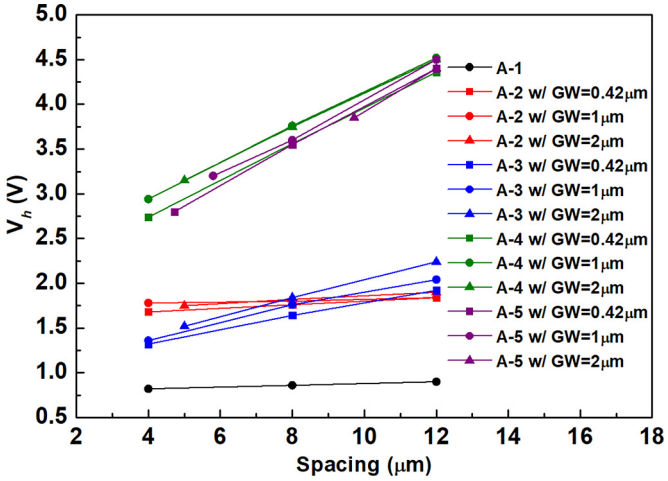


Fig. 8. Relations between V_h and anode-to-cathode spacings with different types and guard ring widths for test structure A.

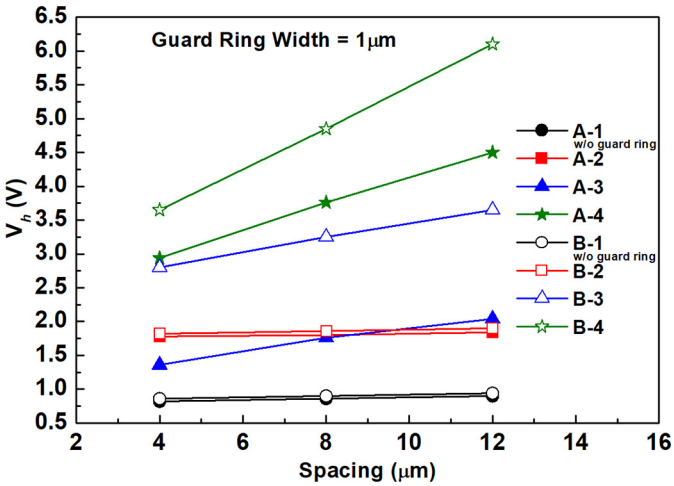


Fig. 9. Relations between V_h and anode-to-cathode spacings with different test types, where the guard ring widths for test structures A and B are kept the same of 1 μm.

of above 8 μm and a guard ring width of above 0.42 μm, the latch-up occurrence can be avoided because the V_h is greater than V_{DD} (3.3 V).

To observe the divergence of latch-up risk between varactor and NMOS, the comparison of the relations between V_h and anode-to-cathode spacings with different types but same guard ring width for test structures A and B is shown in Fig. 9, where the *I-V* curves of the type B-5 cannot be measured because these test structures were burned out once the snapback phenomenon occurred during the dc measurement. Under the same test conditions, the V_h of test structure B is greater than that of test structure A. Any test structure with a higher holding voltage will have a high immunity against latch-up. From the comparing results shown in Fig. 9, the layout rules for the spacing between the I/O PMOS and varactor should be carefully defined to prevent latch-up issue. Such a latch-up risk can be further verified under the latch-up current test of JEDEC standard.

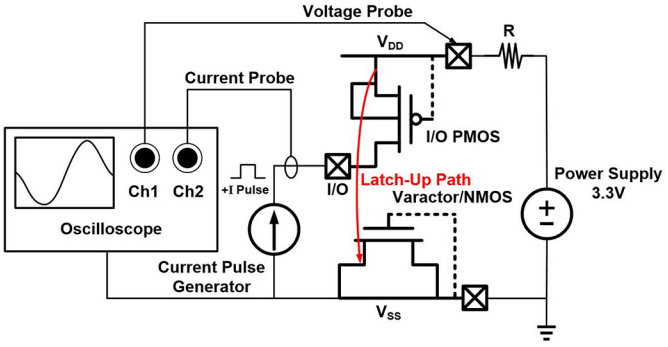


Fig. 10. Latch-up measurement on the test structure with the positive current pulse applied to the I/O pad (connected to the drain of I/O PMOS).

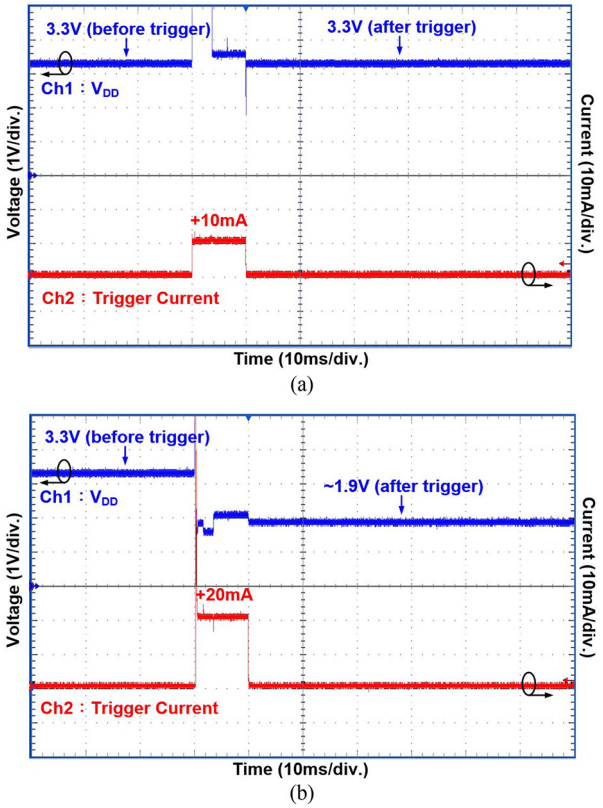


Fig. 11. Measured waveforms of test structure A-3 with an anode-to-cathode spacing of 5 μm and a guard ring width of 2 μm under latch-up positive I-test of (a) 10-mA, and (b) 20-mA, applied to the I/O pin.

B. Latch-Up Current Test

To correlate the dc measurement results, the latch-up current trigger test has been specified in the JEDEC standard (JESD78D). Based on the structures in [10], n-type cathodes in P-Well are most sensitive to positive current injection and as a result this pulse polarity was used for the analysis. The measurement setup of JEDEC latch-up trigger current test is illustrated in Fig. 10. The device under test (DUT) is initially biased at normal circuit operating voltage of 3.3 V (V_{DD}), and the V_{SS} pin is connected to ground. A positive current pulse is applied to the I/O pin that connected to the drain of the I/O PMOS. The voltage and current waveforms on the DUT are monitored by the oscilloscope. As the trigger current pulse with a pulse width of 10 ms is injected to I/O pin, the latch-up event can be judged by monitoring the decrease on voltage waveform of the V_{DD} pin.

Figs. 11(a) and 11(b) show the measured waveforms of test structure A-3 with an anode-to-cathode spacing of 5 μm and a guard ring width of 2 μm under latch-up positive I-test with 10-mA and 20-mA trigger currents applied to the I/O pin, respectively. As shown in Fig. 11(a), the parasitic p-n-p-n path did not be fired on by the trigger current, because the voltage of V_{DD} pin is still kept at 3.3 V after the latch-up I-test. While latch-up is triggered on by the 20-mA I-test, the voltage at V_{DD} is clamped down to ~1.9 V, as shown in Fig. 11(b). The test structure A-3 with an anode-to-cathode spacing of 5 μm and a guard ring width of 2 μm can pass the positive I-test of 10 mA, but fail under 20-mA I-test. By changing the trigger current level and repeating the experimental procedures, the threshold level of trigger current to fire on latch-up path can be found for each test structure.

Moreover, to enhance accurateness of measured data and detailed examination, a commercial latch-up test machine (Thermo Scientific MK.1) with a pulse width of 10 ms, a slew rate of 100-V/1-ms, and a pulse step of 1 mA has been commonly used in IC industry to verify the latch-up immunity. Based on the JESD78D of JEDEC standard, the highest latch-up immunity level under positive I-test is set at 200 mA. For test structures A-2, A-3, and A-4 with different guard ring widths, the measured relations between the anode-to-cathode spacings and the latch-up immunity level under positive current test at a high temperature of 125 °C are summarized in Fig. 12. From the detailed measured results, the test structures A-2 and A-3 have very weak latch-up immunity level of below 10 mA under positive current test, because the holding voltages of the parasitic SCR's in those test structures are all lower than V_{DD} of 3.3V. As a result, the spacing between the I/O PMOS and varactor must be extended wider to improve latch-up immunity, even though either I/O PMOS or varactor has a single guard ring. According the measured results in Fig. 8 and Fig. 12, adding a P+ guard ring for varactor and an N+ guard ring for I/O PMOS with a guard ring width of 1 μm is the better solution to block the latch-up path, because the latch-up immunity can pass 200 mA in this test structure.

To further compare the latch-up issue induced from the I/O PMOS to the varactor (with a grounded N-well) or NMOS capacitor (in a grounded P-Well), the measured relations between the latch-up immunity level under positive current test at 125 °C and anode-to-cathode spacings for the test structures A-1, A-2, A-3, B-1, B-2, and B-3 with the same guard ring width of 1 μm are shown in Fig. 13.

For the different test structures but the same type, the latch-up immunity level of test structure B is essentially greater than that of the test structure A. The measured results illustrate that the latch-up risk of I/O PMOS with varactor is higher than that of I/O PMOS with NMOS. In fact, the area of P-sub/N-Well junction is really larger than P-Well/N+ junction for the same dimension of varactor and NMOS, because the junction depth of N+ diffusion (~0.2μm) is quite shallower than that of

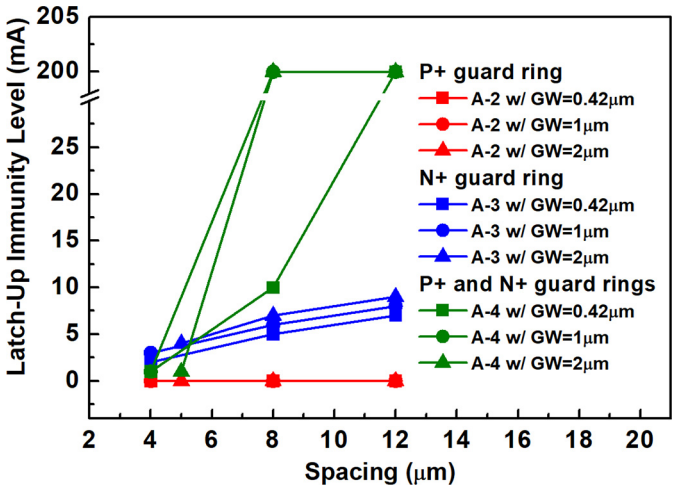


Fig. 12. Relations between the latch-up immunity level under positive current test at 125 °C and the anode-to-cathode spacings for the test structures A-2, A-3, and A-4 with different guard ring widths.

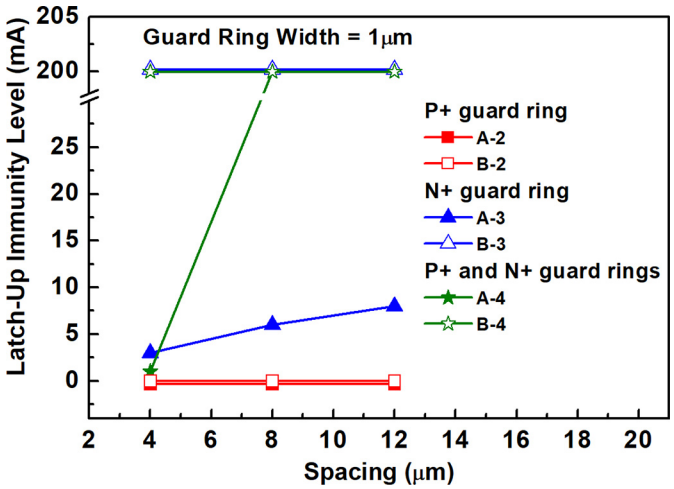
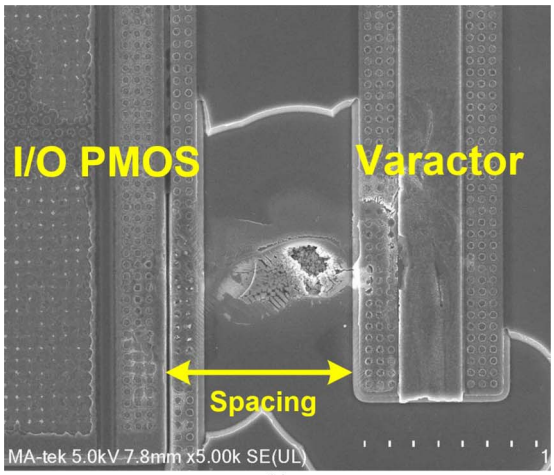


Fig. 13. Relations between the latch-up immunity level under positive current test at 125 °C and anode-to-cathode spacings for the test structures A-1, A-2, A-3, B-1, B-2, and B-3 with the same guard ring width of 1 μm.

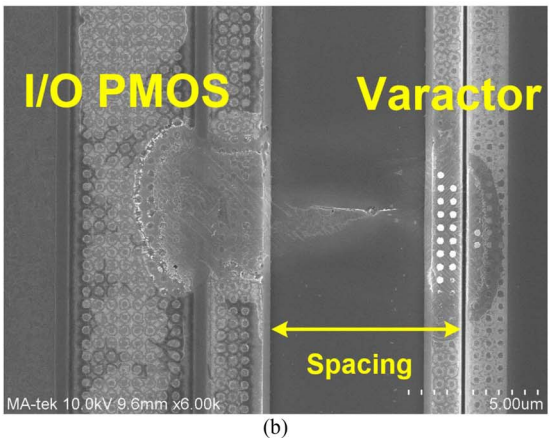
N-Well (∼2μm). As the noise current injecting into the p-substrate, the deeper N-Well junction will absorb the huge noise current to turn on the lateral n-p-n BJT, and further fire on the latch-up path. The gaps of the latch-up immunity in Fig. 12 and 13 are very obvious because the latch-up event will not happen once the V_h of the parasitic SCR is below V_{DD}.

C. Failure Analysis

To further observe the certain failure locations, the scanning electron microscope (SEM) experiment was used. After latch-up current test, the latch-up induced damages on the test structures A-2 and A-3, with the same guard ring width of 1 μm and anode-to-cathode spacing of 8 μm, are investigated and shown in Figs. 14(a) and 14(b), respectively. The latch-up current flowing through the silicon chip caused serious non-recoverable burned-out failure, which obviously located at the path between I/O PMOS and varactor.



(a)



(b)

Fig. 14. SEM photographs of test structures (a) A-2, and (b) A-3, with the same guard ring width of 1 μm and anode-to-cathode spacing (Spacing) of 8 μm after the latch-up positive I-test.

IV. Discussion

In this work, the latch-up risk between the I/O PMOS and the varactor with grounded N-Well has been investigated in details through the fabricated silicon testchip. Similar latch-up path was ever reported in some prior work [15]. For a given CMOS technology by foundry, the guard ring parameters between PMOS and NMOS had been often comprehensive and illustrated in details. Design rules check (DRC) can flag the inappropriate spacing between P+ diffusion of PMOS and N+ diffusion of NMOS by calculating with accuracy. In addition, for a foundry to provide the CMOS process to the customers, the design rules to prevent the latch-up risk between the I/O PMOS and the varactor with grounded N-Well should be given. Some additional latch-up testkeys with split layout parameters, as those presented in this work, should be verified in silicon to formulate the design rules against such non-typical latch-up path.

For the design houses to tape out their chips, the EDA tool should be used to check whether there is any varactor with the grounded N-Well inside the chip layout [16]. For CMOS IC's, especially with the digital circuits, the N-Well are typically tied to V_{DD} or V_{CC}, therefore we can use the EDA tool to find out any N-Well that was not tied to V_{DD} or V_{CC}. If yes, the

clearance/distance from the N-Well of varactor to the neighbor PMOS that connected to V_{DD} or V_{CC} should be re-confirmed with foundry to avoid such non-typical latch-up issue.

If the silicon area was seriously limited for inserting additional guard rings in layout, the N-Well and N+ diffusion of varactor can be tied to V_{DD} with its gate tied to ground to avoid such latch-up event. However, the capacitance value of varactor will be decreased in such a re-connection way.

V. Conclusion

The latch-up issue between I/O PMOS and the varactor with a grounded N-Well has been investigated in 0.18-μm CMOS technology, and compared to that between I/O PMOS and the NMOS capacitor in a grounded P-Well. According to the measurement results in silicon chip, it is really high latch-up concern that on-chip decoupling capacitor realized by the varactor with a grounded N-Well is more sensitive to latch-up risk when it was drawn in layout close to I/O PMOS devices. In the bulk CMOS technology with p-type substrate, the N-well biased at a lower voltage level for some special applications (such as varactor) will collect more trigger current than N+ diffusion in a grounded P-Well to induce serious latch-up event. Fortunately, such a latch-up risk can be solved by adding guard rings with wider spacings under the cost of somehow increasing the layout area. The foundry in semiconductor industry must split comprehensive testkeys with different layout parameters to formulate the corresponding design rule against the latch-up path presented in this work. In addition, EDA tool with some specified additional rules to check such latch-up path in the chip layout should be built in the tape-out flow to avoid latch-up failure.

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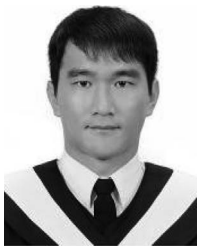

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