An Efficient, Wide-Output, High-Voltage Charge Pump With a Stage Selection Circuit Realized in a Low-Voltage CMOS Process

Zhicong Luo, *Member, IEEE*, Li-Chin Yu, and Ming-Dou Ker, *Fellow, IEEE*

***Abstract*— A wide-output, power-efficient, high-voltage charge pump with a variable number of stages is proposed and realized in a 0.18 μm 1.8 V/3.3 V CMOS process. The proposed stage selection circuit changes the node voltages in the charge pump circuit in a domino effect to ensure that the maximum voltages across the terminals of each transistor are kept within the normal supply voltage (V_{DD}). The stage selection circuit is able to bypass or activate each stage of the charge pump. Experimental results indicate that the proposed charge pump provides a wide-output voltage range: 3.3–12.6 V from a 3.3 V input source. A peak efficiency of 70% was reached in the charge pump at a current loading of 3.5 mA. By selecting the optimal number of active stages, the overall power efficiencies can be greater than 60% under the output voltages of 4.8 V, 8.1 V, and 10.8 V, respectively. By optimizing the number of active stages, an increase of up to 35% power efficiency can be gained. The proposed stage selection circuit is applicable to other on-chip wide-output charge-pumps.**

***Index Terms*— Wide-output, power-efficient, high-voltage, charge pump, stage selection circuit.**

I. Introduction

CLOSED-LOOP deep brain stimulation (DBS) systems with monitoring the disease state of patients is one of the ongoing engineering technologies. The closed-loop DBS system usually consists of an amplifier, a digital signal processor, an ADC, a stimulator, and a charge pump [1]–[2]. The stimulator and charge pump in the DBS system are the exceptions because the operating voltages of these circuits are very high. The 12 V-tolerant stimulators had been developed in the low-voltage CMOS process [3]–[5]. This approach opens the possibility for implementing a fully integrated closed-loop DBS system in a digital low voltage CMOS technology [1], [2]. In addition, stimulators consumed a great deal of power in the closed-loop DBS systems. Thus, there is a necessary to improve the power efficiency of stimulators. Dynamic power supply techniques for the stimulators are widely used to improve the power efficiency. In the existing dynamic power supply techniques, the supply voltages of stimulators are adjusted in real time when needed. Implementing 3-stage regulated charge pump to output a dynamic DC voltage has been shown to greatly reduce power consumption [6].

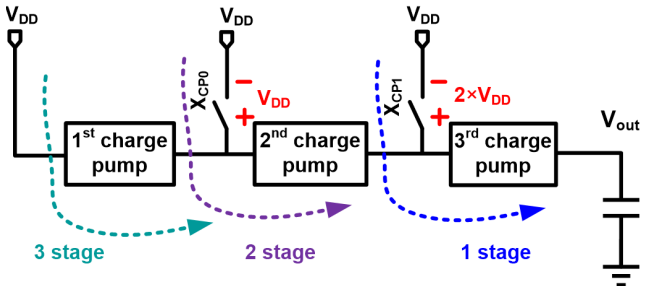

Fig. 1. A reconfigurable regulated wide-output charge pump.

Ideally, in a conventional regulated n-stage charge pump, the output voltage can be adjusted from V_{DD} to $(n+1)\times V_{DD}$ by changing the reference voltage (V_{TARGET}) or the operating clock frequency, where n refers to the number of stages [7], [8]. However, plotting the power efficiency (η) versus the conversion ratio for a wide value range presents a curve closer to an upside down U shape; the power efficiency has a limited range where it reaches its highest values and then decreases rapidly for both higher and lower conversion ratios. Changing the number of active stages of the charge pump shifts the η curve. For a specific conversion ratio, there is an optimal number of stages that provides the highest efficiency [9], [10].

Wide-output charge pumps with reconfigurable stages have therefore been proposed to select an optimal number of active stages to achieve the maximum efficiency at each conversion ratio [7]–[10]. The simplified core circuit of a charge pump is shown in Fig. 1. In this example, the three stages of this charge pump are arranged in series to produce an output voltage. When only two stages are used, switch X_{CP0} is turned on, the first charge pump cell is turned off, and the second charge pump cell begins with an input voltage of V_{DD} rather than the output voltage from the first charge pump. Thus,

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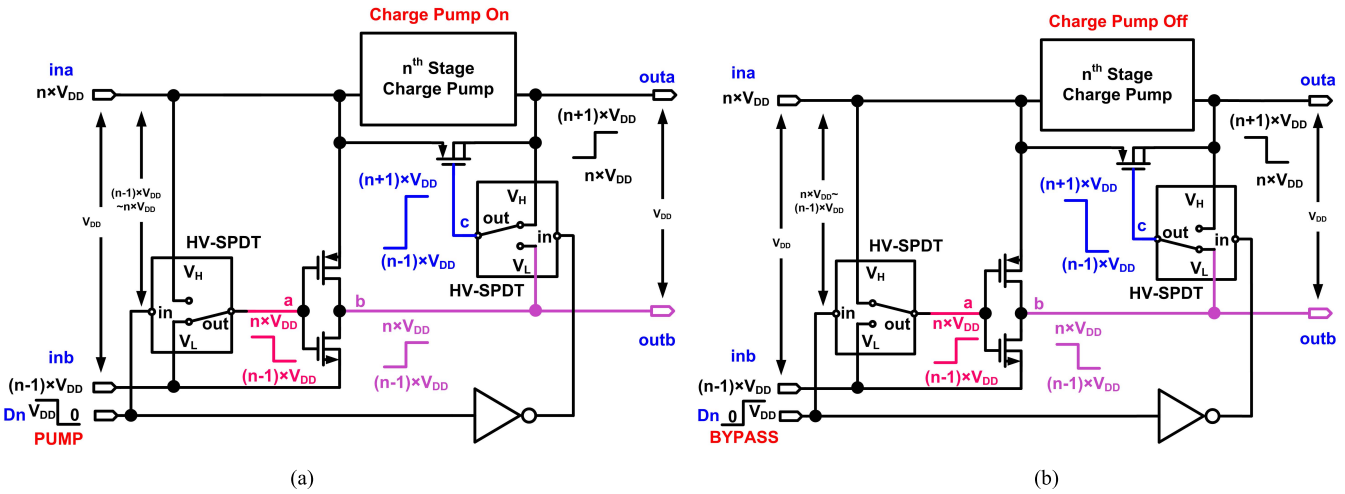

Fig. 2. The operation of a stage selection circuit in (a) pump mode and (b) bypass mode.

$3 \times V_{DD}$ output voltage is produced. When three stages are used, the voltage across the switches X_{CP0} and X_{CP1} are V_{DD} and $2\times V_{DD}$, respectively. Conventionally, high-voltage devices are used as switches (i.e., X_{CP0} and X_{CP1}) to prevent the transistors from electrical overstress and gate-oxide unreliability. These high-voltage devices are manufactured using a standard CMOS process with some special layout techniques and high-voltage layers, thus disadvantageously increasing the layout area of the charge pump.

In [11], an integrated hybrid 4/6-stage step-up converter using low-voltage devices was proposed. Only the lower two stages pump cells in the DC-DC upconverter were designed to be bypassed or activated in the different gain modes. When the bypass switch is turned off and the charge pump is turned on, the voltage drop across the bypass switch is close to $(2 \times V_{DD})$. The source-gate or source-drain voltages of some transistors in the bypass switch are close to $(2 \times V_{DD})$. V_{DD} in [11] is 1 V, thus, all transistors in the bypass switch are operating within the safe voltage range. But, if V_{DD} is 3.3 V, these low-voltage transistors are over-stressed.

In this paper, an efficient, wide-output, high-voltage charge pump with a stage selection circuit is proposed and realized in a low-voltage CMOS process. The proposed new stage selection circuit ensures that the maximum voltages across the terminals of each transistor in the charge pump are kept within the normal supply voltage (V_{DD}). The new stage selection circuit is able to bypass or activate each stage of the charge pump.

II. Operation and Implementation of Proposed Circuit

Figure 2 details the operation of the proposed stage selection circuit. The bypass switch (PMOS transistor) in the stage selection circuit is in parallel with each pump cell. Unlike the prior circuit in [7], which directly connected the input voltage source (V_{DD}) to the input nodes of each pump cell, the proposed structure eliminates voltage overstress in the bypass switches. Each pump cell can be operated in two modes: pump mode or bypass mode. The signal D_n is used to control the bypass switch. In pump mode, the bypass switch is turned off by the falling edge of the control signal and the paralleled pump cell operates in pump mode. In bypass mode, the rising edge of the control signal turns on the bypass switch and the paralleled pump cell is turned off.

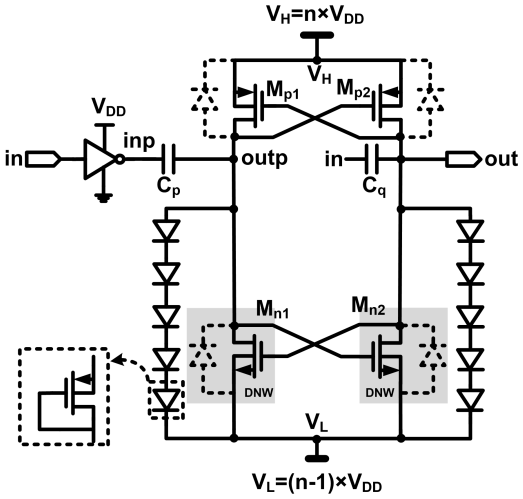

Fig. 3. A schematic of the proposed high-voltage single-pole double-throw. C_p and C_q are implemented by using the metal-insulator-metal capacitor.

Once the control signal D_n switches from high (V_{DD}) to low (0 V) in pump mode (Fig. 2(a)), the voltage at node *a* will switch from high $(n \times V_{DD})$ to low $((n-1) \times V_{DD})$. Thus, node *c* will be connected to node *outa*, and the voltage at node *c* switches from a low $((n-1) \times V_{DD})$ to a high level voltage equal to the voltage at node *outa*, fully turning off the PMOS transistor. The voltage at node *b* also switches from low $((n-1) \times V_{DD})$ to high $(n \times V_{DD})$. The pump cell is then enabled by turning on the clock of the pump cell. The voltages at node *outa* and node *c* will then reach $(n+1) \times V_{DD}$. The maximum voltages across all transistor terminals in the charge pump are kept within the normal supply voltage (V_{DD}). In bypass mode (Fig. 2(b)), the rising edge of the control signal

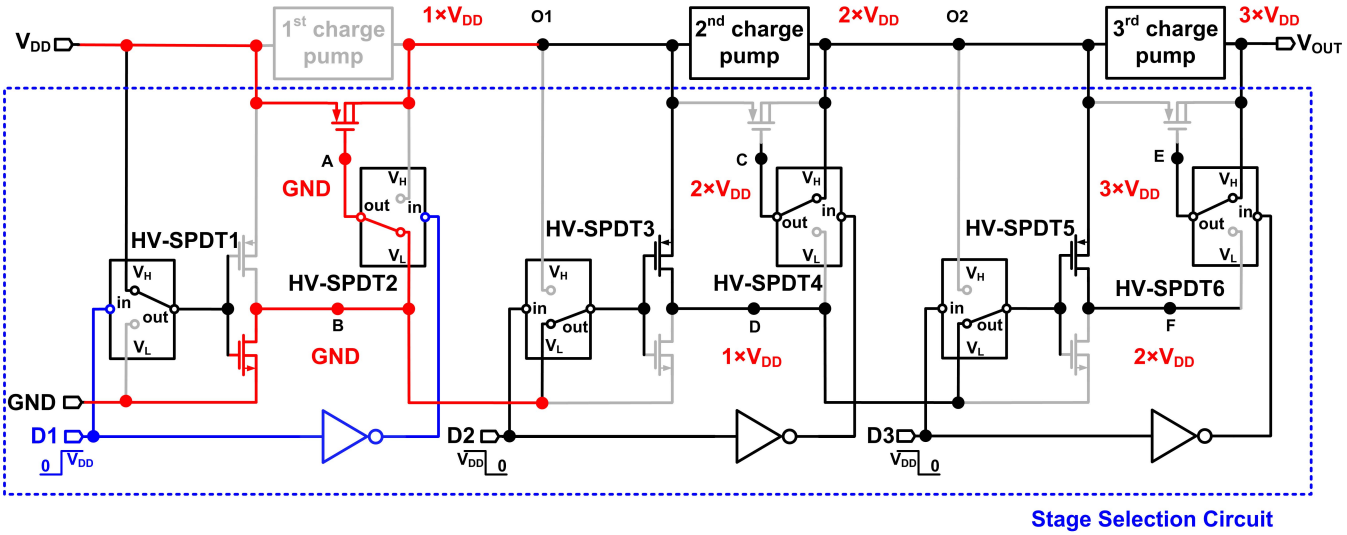

Fig. 4. An example of a 3-stage charge pump with a stage selection circuit. When D1 switches from low (0V) to high (V_{DD}), the first stage charge pump is bypassed. Therefore, the 3-stage charge pump generates an output voltage of $3 \times V_{DD}$.

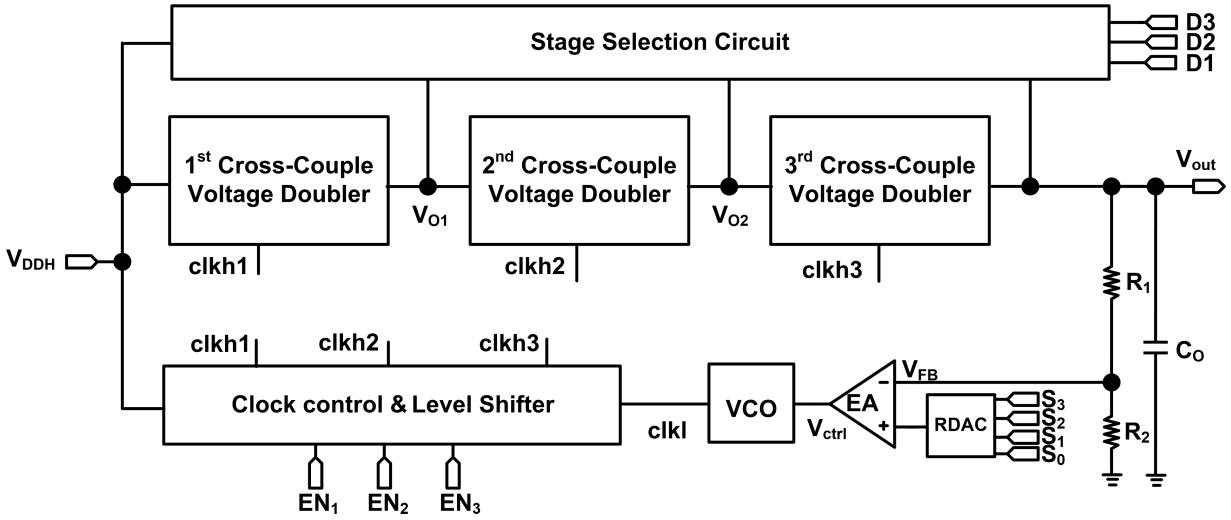

Fig. 5. The proposed wide-output, power-efficient, and high-voltage regulated charge pump.

D_n turns on the PMOS transistor, turns off the pump cell, and connects nodes *outa* and *ina*, thus bypassing the pump cell.

The detailed circuit of the proposed high-voltage single-pole-double-throw (HV-SPDT) cell is shown in Fig. 3. As a voltage level shifter circuit, HV-SPDT connects the output node to the nodes V_H or V_L by the input control signal. A conventional voltage level shifter can be realized in both high-voltage and low-voltage processes. The standard method for manufacturing high-voltage devices involves the standard CMOS process with high-voltage layers and some special layout techniques, thus disadvantageously increasing the layout area of the level shifter. Another approach involves stacking low-voltage devices [12]–[15]. However, as prior circuit topologies employing this method use $(n-1)$ stacked inverters to withstand $n \times V_{DD}$ voltage, these topologies are difficult to use with dynamic power supplies.

In Fig. 3, when the input signal (in) changes from 0 V to V_{DD}, the voltage at node *out* changes up with a factor ΔV:

$$\Delta V = \frac{C_q \cdot V_{DD}}{C_q + C_{par}}, \tag{1}$$

where C_{par} is the parasitic capacitance at the node *out*. By well adjustment, the voltages at nodes o*utp*and *out* switch from one state to the other. Two cross coupled pairs are adopted to store the state information. Thus, HV-SPDT has two stable states and can be used to store state information.

If the voltages on the nodes (*outp* and *out*) become lower than $(n-1) \times V_{DD}$ or higher than $n \times V_{DD}$, the parasitic diodes of the NMOS or PMOS transistor will be turned on, respectively, thus restricting the voltage on the nodes between $n \times V_{DD}$ and $(n-1) \times V_{DD}$.

A diode connection string was added to maintain the voltage drops between the nodes (*outp* and *out*) and the node V_L within V_{DD} (about five times threshold voltage). If the voltage on the node V_L abruptly decreases, the diode string will be turned on to decrease the voltages of nodes *outp* and *out*.

An example of a three-stage charge pump with a stage selection circuit is shown in Fig. 4. The number of active stages is set by the stage selection circuit. When the control signal D1 is switched from low (0 V) to high (V_{DD}), the bypass transistor is turned on, and the voltage on node

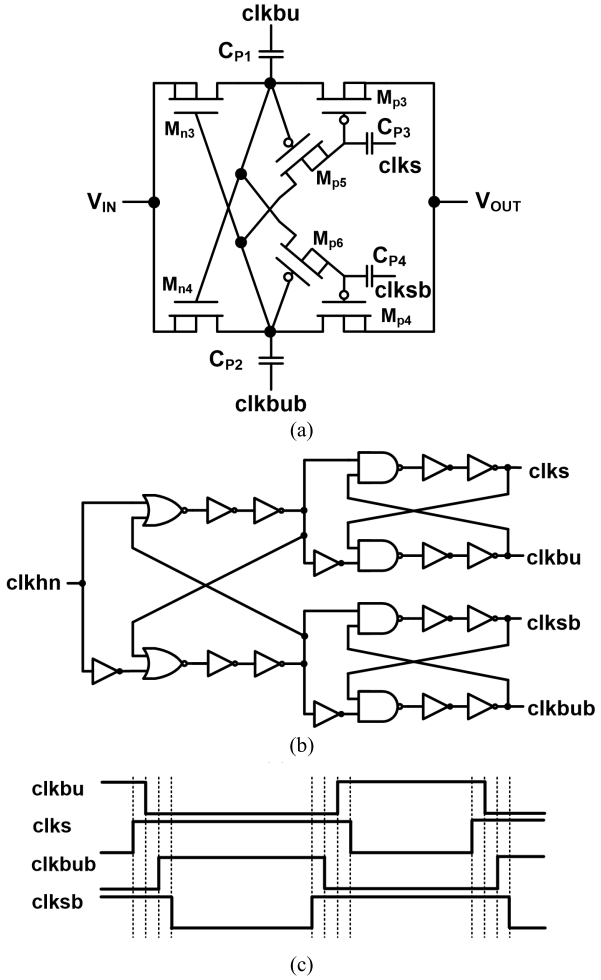

Fig. 6. (a) The detailed circuit of the cross-couple voltage doubler. (b) Detailed circuit of the non-overlapping 4-phase clock generator. (c) The waveform diagram of the non-overlapping 4-phase clock generator.

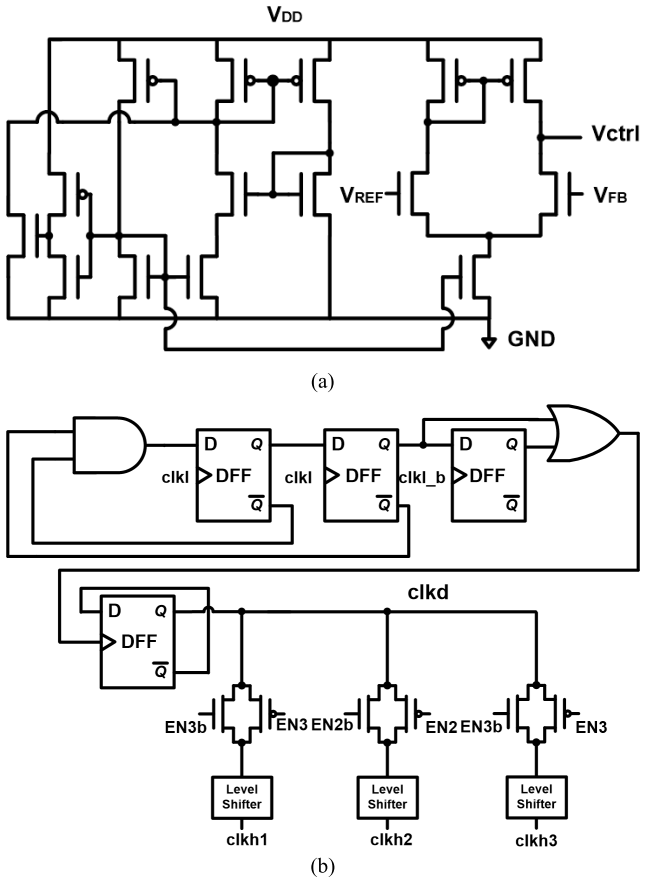

Fig. 7. (a) Detailed circuit of the error amplifier. (b) Detailed circuit of the phase shift clock generator.

O1 decreases to V_{DD}. If the voltage on node *O2* remains at $3\times V_{DD}$, voltage overstress would occur between the terminals of the bypass transistor, HV-SPDT, and charge pump circuit. The diode connection string in HV-SPDT was thus added to ensure the voltages at the nodes (*out* and *outp*) in HV-SPDT those were changed with the voltage at node *O1*. As the voltage across the diode connection string is about V_{DD}, the bypass transistor is turned on, and the voltage at node *O2* drops from $3\times V_{DD}$ to $2\times V_{DD}$. Similarly, the voltage at node V_{out} will change from $4\times V_{DD}$ to $3 \times V_{DD}$. Overall, the voltages on nodes *O1* to *On* would change in a domino effect.

The proposed wide-output charge pump, shown in Fig. 5, consists of an error amplifier, a voltage divider, resistive DAC, VCO, level shifter, clock generator, stage selection circuit, and three-stage charge pump. The charge pump uses a PFM feedback network to generate the regulated output voltage. The output voltage (V_{ctrl}) of the error amplifier is determined by the difference in voltage between V_{FB} and the output voltage of the resistive digital-to-analog converter. The clock frequency of *clkl* is controlled by V_{ctrl}. When the output voltage (V_{out}) is lower than the predefined voltage, V_{ctrl} and the frequency of *clkl* increases until V_{out} reaches the predefined voltage. Similarly, when V_{out} is higher than the predefined voltage, the frequency of *clkl* decreases. To determine which stages of the charge pump to pump or bypass, a stage selection circuit and clock controller were implemented and are controlled by signals D1, D2, D3, EN1, EN2, and EN3. Each stage of charge pump has its own four-phase clock generator, which provides the charge pump with the necessary adaptive control signals.

A detailed circuit of the four-phase cross-coupled voltage doubler is shown in Fig. 6(a) [16]. The capacitor pairs for voltage pumping (C_{P1} and C_{P2}) and for clock boosting (C_{P3} and C_{P4}) were used to reduce conduction losses and voltage drops. The gate driving of the NMOS transistors (M_{n3} and M_{n4}) were separated from that of the PMOS transistors (M_{p3} and M_{p4}) by using a voltage doubler cell. The bulk terminals of the devices were connected to their respective source terminals. Fig. 6(b) shows the circuit of non-overlapping 4-phase clock generator. Fig. 6(c) shows the waveform diagram of the non-overlapping 4-phase clock generator. The error amplifier is shown in Fig. 7(a). Fig. 7(b) shows the circuit of clock generator, which consisting of a frequency divider and three level shifters. The level shifter translates the signals from 1.8 V to 3.3 V.

III. Experimental Results

The high-voltage charge pump has been fabricated in a 0.18-μm 1.8-V/3.3-V CMOS process, and the die photo is

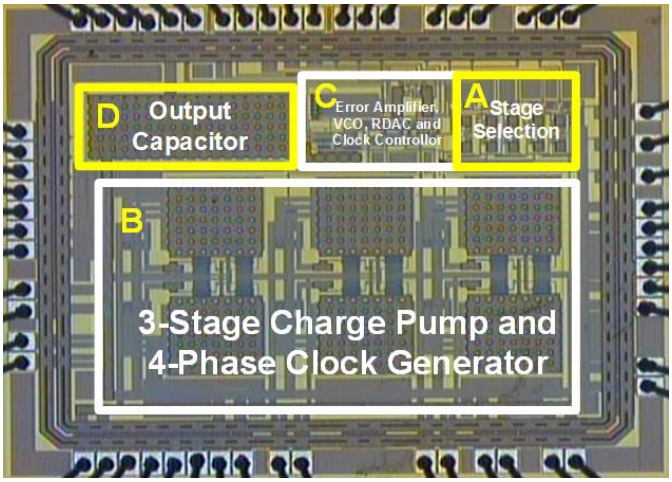

Fig. 8. Die photo of the fabricated high-voltage regulated charge pump.

shown in Fig. 8. The pumping capacitors (C_P) of charge pump are 50 pF, and the output capacitor (C_O) is 100 pF. All capacitors in the charge pump are fully on-chip and implemented by using the metal-insulator-metal capacitor. The silicon area of the charge pump is 1.88×1.53 mm^2.

A. Peak Transient Voltage

The peak transient voltage occurred in the transient state of changing charge pump stages in the condition of the heavy loading current. Simulation results showed that the voltages across the terminals of all transistors can be limited to the nominal supply in the steady state. Nominal supply voltage in IC applications usually has 10% of tolerance. With the normal power supply of 3.3 V, it covers the operating voltage of 2.97 V to 3.63 V in steady-state condition. With the maximum peak transient voltage of $\sim$ 3.7 V in a very short time period of several nanoseconds, the overstress issue on the proposed circuit in the transient state is tolerable.

B. Measurement Results

The measurement results of HV-SPDT cell were shown in Fig. 9, the output square wave signal switched between the voltages on nodes V_H and V_L. All transistors in the proposed level shifter operated within the safe voltage range, thus eliminating any electrical overstress and gate-oxide unreliability. In addition, simulation and measurement results showed that the proposed HV-SPDT is equivalently or less sensitive to process, voltage, and temperature variations.

The control signals (D1, D2, D3, S3, S2, S1, and S0), shown in Fig. 5, were generated by an Arduino UNO. A Keithley 2400 source meter was used to provide the power supply voltages. The measured voltage waveforms on nodes *O1*, *O2*, V_{out} in Fig. 5 are shown in Fig. 10. Signals S3, S2, S1, and S0 were first set to 1, 1, 1, and 0, respectively. The voltage doublers in the high-voltage charge pump were then sequentially enabled by changing D1, D2, and D3 to 1, 1, and 1, then 0, 1, and 1, then 0, 0, and 1, then 0, 0, and 0, then 0, 0, and 1, then 0, 1, and 1, and finally, 1, 1, and 1.

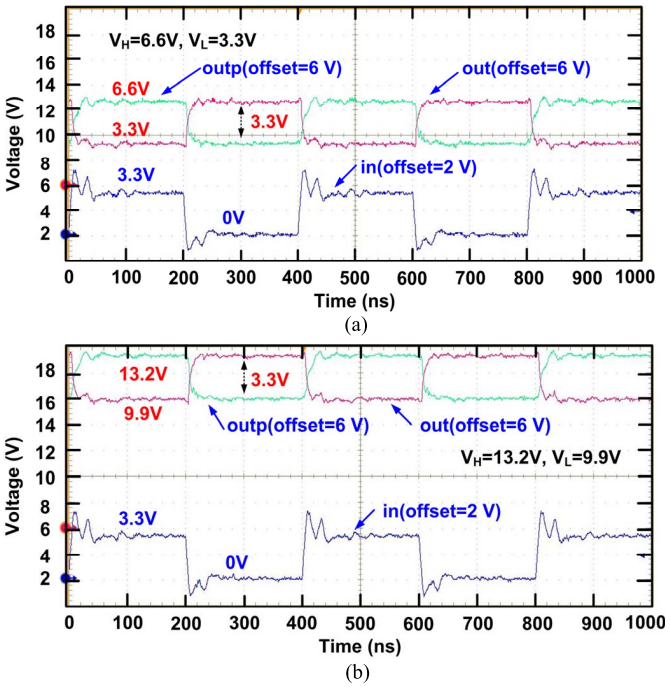

Fig. 9. The measurement result of HV-SPDT output waveforms (a) when $V_H = 6.6$ V and $V_L = 3.3$ V, and (b) when $V_H = 13.2$ V and $V_L = 9.9$ V.

When D1, D2, and D3 were set to 1, 1, and 1, respectively, all of the pump cells were bypassed and turned off, and the voltage on nodes *O1*, *O2*, V_{out} was 3.3 V, as shown in Fig. 10. Once D1 switched from high to low, the first stage voltage doubler was enabled and the output voltage of the high-voltage charge pump rose to 5.9 V. When D2 switched from high to low, the second stage voltage doubler was enabled, rising the output voltage of the high-voltage charge pump to 8.6 V. When all of the voltage doublers were enabled, the voltages on nodes V_{out}, *O2*, and *O1* were 11.4 V, 8.6 V, and 5.9 V, respectively.

The output voltage of the high-voltage charge pump under different controlling patterns and a current loading of 0.5 mA is shown in Fig. 11. This operating process can be divided into 11 phases. During phase 1, the control signals D1, D2, and D3 switched from low to high, thus turning off and bypassing all of the pump cells and resulting in an output voltage of the high-voltage charge pump of 3.3 V. During phase 2, the control signals D1, D2, D3 switched from high to low, enabling all of the pump cells. Once S3, S2, S1, and S0 changed to 1, 1, 1, and 0, respectively, the output voltage was 12.6 V. During phase 3, D1 switched from low to high, turning off and bypassing the first stage pump cell, resulting in an output voltage of about 9 V. During phase 4, the control signals S3, S2, S1, and S0 were changed to 1, 0, 0, and 1, respectively; the resulting output voltage was 8.1 V. During phase 5, D2 switched from low to high, turning of an bypassing the first and second stage pump cells. Once S3, S2, S1, and S0 were changed to 0, 1, 0, and 1, respectively, the output voltage was 4.8 V. The number of optimal active stages varied at different target voltages; 3-stage, 2-stage, and 1-stage pump cells were used to provide the target voltages of 12.6 V, 8.1 V, and 4.8 V, respectively.

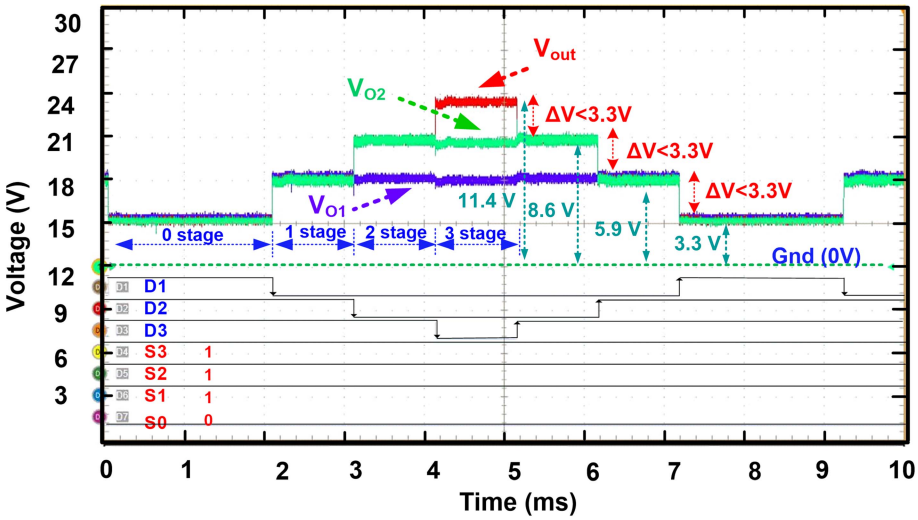

Fig. 10. The measured voltage waveforms on nodes *O1*, *O2*, and V_{out} under a current loading of 3.5 mA, as the number of active stages changes from 0 to 3 to 0.

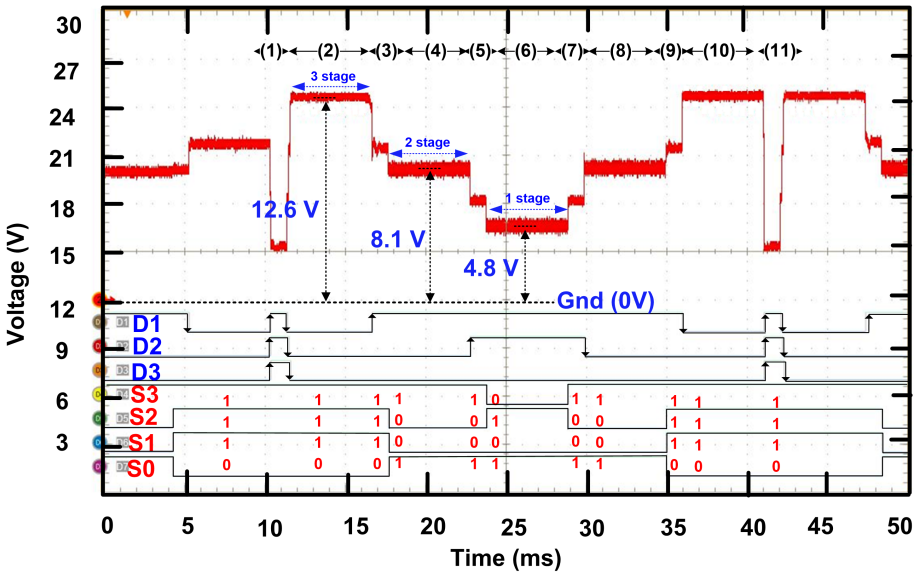

Fig. 11. The output voltage of the high-voltage charge pump under a current loading of 0.5 mA and under different controlling patterns.

Power efficiency vs. output voltage under a varying number of active stages and current loading is shown in Fig. 12. The targeted voltages were 12.6, 10.8, 8.1, and 4.8 V. As was shown in Fig. 11, to achieve each of these, S3, S2, S1, and S0 were set to 1, 1, 1, and 0; 1, 1, 0, and 0; 1, 0, 0, and 1; and 0, 1, 0, and 1, respectively. Although an output voltage of 4.8 V could be produced by the charge pump with any number of active stages, a power efficiency of approximately 60% was reached when using a one-stage pump cell.

The power efficiency of the proposed high-voltage charge pump with or without the stage selection circuit is shown in Fig. 13. Use of the stage selection circuit allowed for multiple optimal conversion ratios. By selecting the optimal number of active stages, the measured power efficiencies can be greater than 60% under the output voltages of 4.8 V, 8.1 V, and 10.8 V, respectively. By optimizing the number of active stages, an increase of up to 35% power efficiency can be gained. Therefore, the proposed stage selection circuit can greatly improve the power efficiency under a wide output voltage range. By adding the load detection and adaptive control circuits as shown in [7] and [10], the proposed stage-selection circuit is able to select the optimal number of active stages automatically for a specified output voltage and loading current with maximum power efficiency.

In addition, the proposed regulated charge pump did not generate a specified 12.6-V output voltage in the case of heavy loading current. There are several factors those contribute to output voltage error due to the loading current, including the internal resistance of the charge pump, and so on [20]–[22]. As the loading current changes, the voltage drop across the internal resistance also changes due to which the output voltage also gets affected. When the loading current increases,

TABLE I
PERFORMANCE COMPARISON WITH THE PRIOR WORKS

	ISSCC 2014 [17]	TCAS-I 2017 [18]	JSSC 2010 [19]	JSSC 2015 [11]	U. S. Patent 2012 [7]	This work
Technology	0.16-μm CMOS	0.18-μm 1.8-V/3.3-V CMOS	0.35-μm n-well CMOS process	0.18-μm low voltage CMOS	High-voltage process	0.18-μm 1.8-V/3.3-V CMOS
Stage	6×	3×	2×/3×	4×/ 6×	1×/ 2×/ 3×	1×/ 2×/ 3×
Conv. Ratios	4.8	3.2	2~3	3~6	n/A	1~3.3
Vout	16 V@7mA	10.5V@3.5mA	3.6~6V	3~6V	4~9V	3~10.8V@3.5mA 3~12.6V@0.5mA
Output Current	0.1 ~ 7 mA	0.5 ~ 3.5 mA	< 60mA	30 μA ~ 240 μA	n/A	0.5 ~ 3.5 mA
Cap	SMD Ext. 1μF×2 +100nF+220nF	MIMCAP Integrated 400pF	1μF (Flying) + 2.2μF (Output)	MIMCAP and MOSCAP	n/A	MIMCAP Integrated 400pF
Efficiency	70%@7mA	69%@3mA	62% ~ 91%	48% ~ 58%	50% ~ 62%	60% ~ 70%

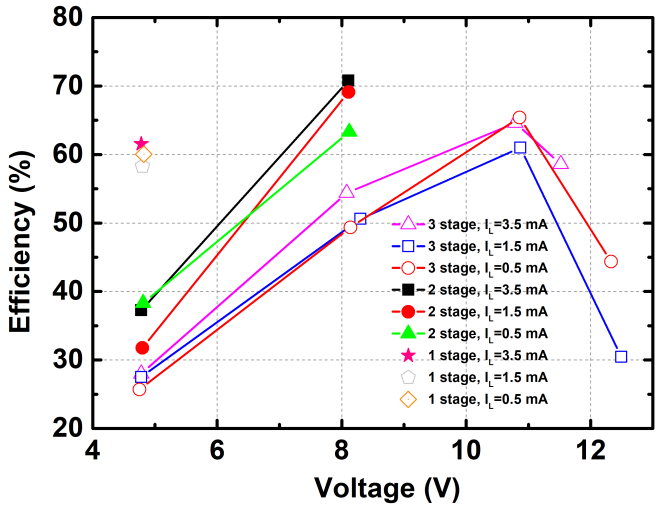

Fig. 12. Efficiency vs. output voltage of the proposed charge pump under a varying number of active stages.

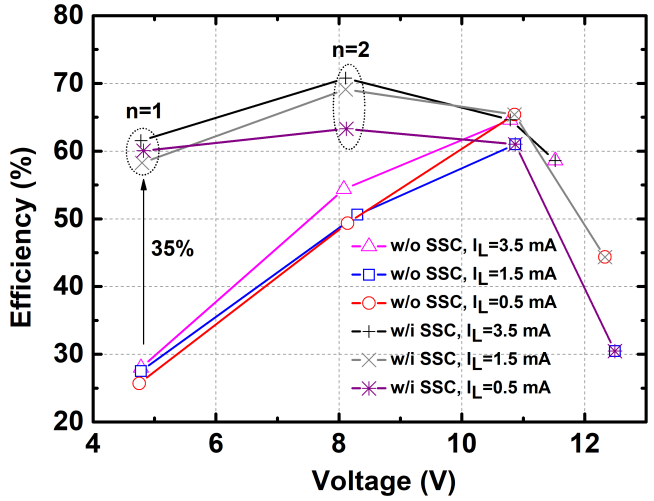

Fig. 13. Power efficiency vs. output voltage of the proposed charge pump with or without the stage selection circuit (SSC).

the output voltage decreases. In this design, the proposed unregulated charge pump is just able to generate 11.4-V voltage when the loading current is 3.5 mA. Thus, the scheme in Fig. 5 did not get the output voltage to the desired level for the 3-stage configuration.

C. Performance Comparison With Prior Works

Key specifications of the proposed charge pump are compared with prior works in Table I, including charge pumps with reconfigurable stages and step-up charge pumps with a large output current. With a DC input voltage of 3.3 V, the proposed charge pump is capable of providing a voltage of 10.8 V with a current loading of 3.5 mA, thus achieving DC conversion efficiencies of up to 70% with total integrated capacitances of 400 pF.

IV. CONCLUSION

A stage selection circuit using only standard low-voltage transistors for a multi-stage charge pump was designed and verified in a 0.18 μm 1.8 V/3.3 V CMOS process. The proposed stage selection circuit was realized in a low-voltage CMOS process, and it was able to select which pump cells to bypass for optimal power efficiency. The proposed HV-SPDT in the stage selection circuit ensures that the maximum voltages across the terminals of each transistor are kept within the normal supply voltage (V_{DD}). The proposed high-voltage charge pump with the stage selection circuit can provide a wide output voltage range of 3.3 ~ 12.6 V. The proposed wide-output charge pump can maximize the overall power efficiency, especially suitable for the implanted neuro-simulator with high-voltage operation.

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