Optimization Design on Active Guard Ring to Improve Latch-Up Immunity of CMOS Integrated Circuits

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***Abstract*— A new optimization design of an active guard ring has been proposed to improve latch-up immunity of CMOS integrated circuits and been successfully verified in a 0.18-μm 1.8-/3.3-V CMOS technology. Codesigned with the on-chip electrostatic discharge (ESD) protection devices (gate-ground nMOS and gate-VDD pMOS) equipped at the input–output (I/O) pad, the overshooting/undershooting trigger current during latch-up test can be conducted away through the turned-on channels of the ESD protection MOSFET's to the power rails (V_{DD} or V_{SS}). Therefore, the trigger current injecting from the I/O devices (that directly connected to the I/O pad) through the substrate to initiate the latch-up occurrence at the internal circuit blocks can be significantly reduced. Thus, the latch-up immunity of the whole chip can be effectively improved under the same placement distance between the I/O cells and the internal circuit blocks. The new proposed design is a cost-efficient solution to improve latch-up immunity and also to mention good ESD robustness of the I/O cells.**

***Index Terms*— Active guard ring, electrostatic discharge (ESD) protection, guard ring, latch-up, silicon-controlled rectifier (SCR).**

I. Introduction

IN CMOS integrated circuits, latch-up is formed by the parasitic silicon-controlled rectifier (SCR) structure which crosses between V_{DD} and V_{SS}. When the parasitic SCR path is triggered on by the external overshooting/undershooting noises at input–output (I/O) pads, a low-impedance path will be generated to conduct a huge current from V_{DD} to V_{SS} [1]–[3]. The huge current of the latch-up path often causes unrecoverable failures in the CMOS chips. Due to the inherent parasitic SCR paths existing in the CMOS technology, the latch-up issue has been one of the main reliability concerns in CMOS IC products.

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TABLE I
TRIGGER CHARACTERIZATION IN LATCH-UP CURRENT TEST [4]

Immunity Level	Test	Magnitude of Trigger Force Current
A	Positive I-Test	≥ 100 mA
	Negative I-Test	≥ 100 mA
B	If immunity level A cannot be achieved	

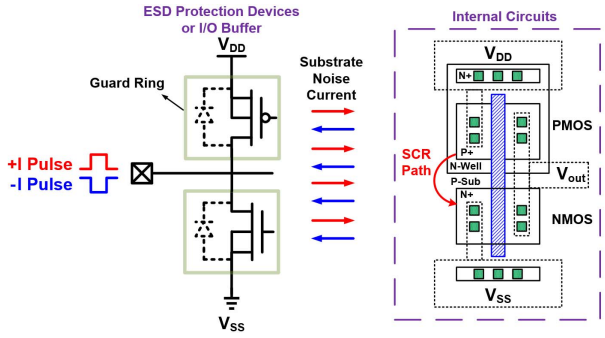

Fig. 1. Traditional latch-up prevention in CMOS IC with guard rings to surround the ESD protection devices and I/O buffer.

Joint Electron Device Engineering Council (JEDEC) has defined the method with test procedures to investigate the latch-up immunity with positive and negative trigger current tests (I-tests) for CMOS ICs. The trigger characterization for latch-up I-test in the up-to-dated standard (JESD78E) is listed in Table I [4]. To avoid damages or reliability issues from the latch-up phenomenon in real field applications, IC companies may have even much higher specification on latch-up immunity level for their CMOS IC products. Therefore, the cost-efficient solution to further improve the latch-up immunity is strongly requested in IC industry.

It is difficult to eliminate the external noises at I/O pads according to the complex operating environments in the extensive applications of CMOS ICs. To improve the latch-up immunity of CMOS ICs, some process methods [5]–[10] and layout skills [11]–[15] had been reported. Without additional special process modification, the guard rings in layout placement are universally applied for latch-up prevention, but those occupy extra silicon area. The illustration of traditional latch-up prevention in CMOS IC with guard rings to surround the electrostatic discharge (ESD) protection devices or I/O buffer is shown in Fig. 1. Under latch-up trigger current

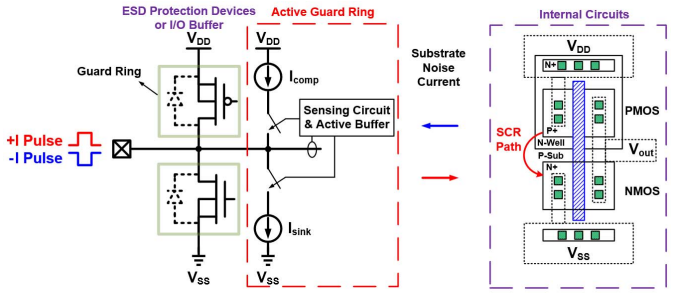

Fig. 2. Concept of active guard ring to reduce substrate noise current at the SCR path of internal circuits under latch-up I-tests.

test, the positive/negative current pulse is injected to I/O pads, which may be conducted to V_{DD}/V_{SS} through the body diode of ESD protection devices or I/O buffer in the forward-biased conditions. In reality, the applied trigger current is not totally absorbed by the body diode of ESD protection devices or I/O buffer. On the contrary, a certain part of trigger current applied at the I/O pad may flow into p-substrate to enable the parasitic SCR path existing in the logic gates of internal circuits without guard rings surrounding them. As a result, to avoid the latch-up concern in the internal circuit blocks due to the latch-up trigger current applied at the I/O pad, the spacing between I/O cells and internal circuit blocks must be extended [15].

A novel design concept named as an active guard ring to improve the latch-up immunity of ICs was reported in [16]. Using additional sensing circuit and active buffer to turn on the ESD protection devices, the large-dimensional ESD devices or I/O buffer can provide or receive extra compensation current to the negative or positive current perturbation through the inversion layer of MOSFET during the latch-up current test, as shown in Fig. 2. Therefore, the latch-up risk of internal circuits decreased significantly because the injected current almost flowed through the channels of I/O devices to the power rails instead of leaking into the substrate. However, the extra layout area of sensing circuit and active buffer can be resulted in an additional layout area. On the other hand, the leakage current caused by the diode string providing the voltage reference for the gate bias in the sensing circuit and active buffer should be further reduced.

In this paper, an optimization design of active guard ring to improve latch-up immunity of CMOS integrated circuits was proposed and verified in 0.18-μm 1.8-/3.3-V CMOS technology. In comparison with the prior active guard ring [16], the new proposed design can successfully integrate the I/O devices and the circuit of active guard rings within a limited I/O cell layout area. In addition, the standby leakage current issue in the prior art is also completely solved. Finally, the detailed examinations to verify the latch-up immunity have been measured by a commercial latch-up test machine.

II. Optimization Design of Active Guard Ring

A. Circuit Implementation

Fig. 3 shows the circuit structure of the proposed active guard ring composed of a sensing circuit block and a pair

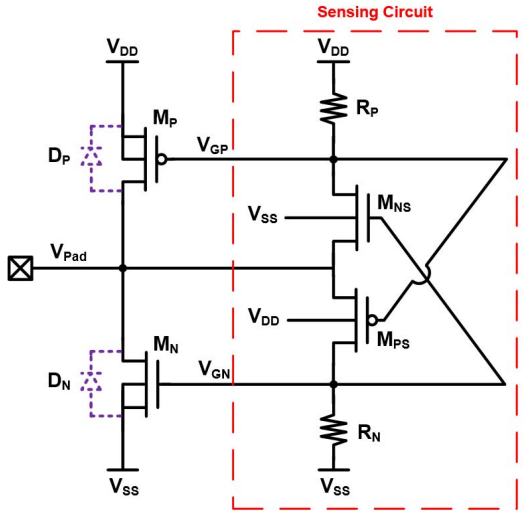

Fig. 3. Circuit structure of the proposed active guard ring with simplification and optimization design.

of large-dimensional ESD protection transistors. The sensing circuit is composed of two sensing devices (M_{PS} and M_{NS}) and two resistors (R_P and R_N).

Under normal circuit operation, the gate voltage of pMOS (V_{GP}) is pulled to V_{DD}, and the gate voltage of nMOS (V_{GN}) is pulled to V_{SS} through R_N. Thus, all devices are kept in OFF-state to prevent the signal loss without excessive leakage current. Under latch-up I-test with the positive or negative trigger currents applied to the I/O pad, the detail circuit operations are shown in Fig. 4(a) and (b), respectively.

In Fig. 4(a), once a large enough positive current pulse is injected to I/O pad under positive I-test, V_{Pad} will be raised up with a certain high voltage above V_{DD}. For the traditional latch-up prevention with guard ring, the trigger current mostly flows into the body diode (D_P) of M_P. With the drain-to-bulk current (I_{DP}) of M_P increasing, more and more substrate noise current will induce latch-up in internal circuits as well. However, in this new proposed design, M_{PS} will be turned on if V_{Pad} is larger than V_{GP} which is normally biased at V_{DD} under power-ON situation. As a result, the gate voltage (V_{GN}) of M_N is pulled up by the channel current of M_{PS}, and the inversion layer of M_N is generated to conduct the trigger current from the pad to V_{SS}. In this way, the latch-up risk is improved with less current injecting into the substrate.

The circuit operation during negative I-test is shown in Fig. 4(b). In contrast to positive I-test, while a large enough negative current pulse is applied to I/O pad, V_{Pad} will be pulled down with a low voltage level below V_{SS}. Therefore, for the latch-up prevention with traditional guard ring, the trigger current is mostly absorbed by the body diode (D_N) of M_N to enhance the latch-up risk of internal circuits. However, in this new proposed design, M_{NS} will be turned on once V_{Pad} is lower than V_{GN} which is normally biased at V_{SS} under power-ON situation. In addition, the gate voltage (V_{GP}) of M_P is pulled down to trigger M_P by the channel current of M_{NS}, and the inversion layer of M_P is generated to conduct some current from V_{DD} to the I/O pad that compensates the negative trigger current applied at the I/O pad. By this way, the drain-to-bulk current (I_{DN}) of M_N is restrained to suppress the latch-up

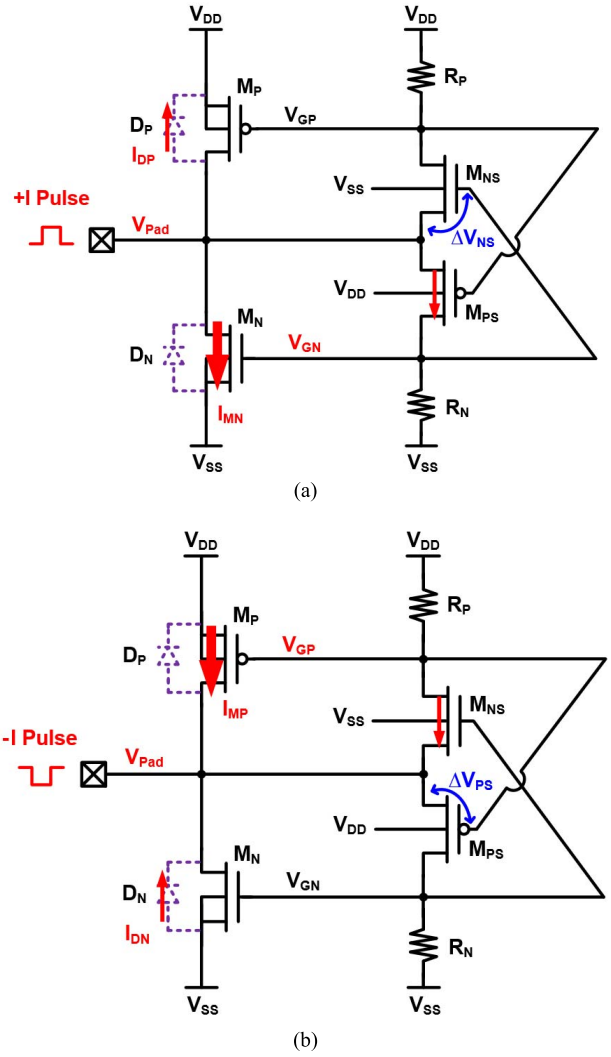

Fig. 4. Circuit operations of the proposed active guard ring during latch-up I-test with (a) positive and (b) negative, trigger current.

event in internal circuits because the current injecting into the substrate through the drain-to-bulk diode of M_N is significantly reduced.

On the other hand, if the gate of M_{NS} is connected to V_{ss} directly, the voltage difference (ΔV_{NS}) between V_{Pad} and the gate voltage of M_{NS} may be over 1.1-times V_{DD} which may cause reliability concern under positive I-test. As a result, the gate of M_{NS} has to be connected to the gate of M_N to avoid the overvoltage stress issue. During negative I-test, the similar reliability issue will show up if the gate of M_{PS} is directly connected to V_{DD}, so the gate of M_{PS} must be connected to the gate of M_P to avoid the overvoltage stress.

B. Simulation

All simulated results are investigated by HSPICE simulation in a 0.18-μm 1.8-/3.3-V CMOS process with the device parameters provided by foundry, including the drain-to-bulk diodes in the ESD devices (M_P and M_N). For latch-up I-test, the timing specification of the trigger pulse has been defined in the JEDEC standard [4]. The positive or negative trigger current pulse with a 10-μs pulsewidth and a 200 mA of peak current is applied to I/O pad, and the V_{DD} is biased at 3.3 V.

TABLE II
SIMULATED RESULTS FOR THE ESD DEVICES WITH THE PROPOSED DESIGN UNDER POSITIVE I-TEST WITH A 200 mA OF CURRENT PULSE

Device	Temperature		
	25°C	75°C	125°C
I_{MP}	1.07mA	1.19mA	1.26mA
I_{MN}	195.3mA	195.5mA	187.1mA
I_{DP}	0.02mA	0.64mA	9.06mA
I_{DN}	3.32mA	2.32mA	1.62mA
ΔV_{NS}	1.29V	1.14V	0.94V

TABLE III
SIMULATED RESULTS FOR THE ESD DEVICES WITH THE PROPOSED DESIGN UNDER NEGATIVE I-TEST WITH A −100 mA OF CURRENT PULSE

ESD Devices with the Proposed Design under Negative I-Test with a -100-mA Current Pulse			
Device	Temperature		
	25°C	75°C	125°C
I_{MP}	99.42mA	98.54mA	91.14mA
I_{MN}	0.27mA	0.30mA	0.31mA
I_{DP}	0.17mA	0.13mA	0.09mA
I_{DN}	0.05mA	0.91mA	7.89mA
ΔV_{PS}	1.93V	1.86V	1.86V

For the ESD devices with the optimized design of active guard ring circuit, the simulated results under positive I-test with a 200 mA of current pulse are listed in Table II. When the positive energy is performed on pad, M_{PS} will be turned on to pull up the gate of M_N. The inversion layer of M_N is generated to provide a low-impedance path and leads the current to V_{SS}. As shown in Table II, the drain-to-source current (I_{MN}) of M_N dominated above 90% trigger current even at 125 °C, and the substrate current is predicted to be decreased effectively.

Table III illustrates the simulated results under negative I-test with a current pulse of −100 mA. The proposed optimization design of active guard ring circuit normally works under negative I-test with a lower peak current. However, the function of the proposed design was degraded under negative I-test with a −200-mA current pulse at high temperature, as illustrated in Table IV. The drain-to-source current (I_{MP}) of M_P dominates about 80% trigger current at 25 °C but only 15% trigger current at 125 °C. Because the turn-on voltage of diode decreases significantly at high temperature, more trigger current is led to the body (drain-to-bulk) diode. In addition, M_P is unable to afford such a high current of 200 mA due to the lower mobility of pMOS with limited device size. As a result, more trigger current at the I/O pad may be injected into the substrate to induce latch-up occurrence at the neighborhood internal circuit blocks at high temperature. To further verify this phenomenon, the simulated results for the ESD devices with the proposed design with an enlarged dimension of M_P under negative I-test of −200-mA current pulse are listed in Table V. At a high temperature of 125 °C,

TABLE IV
SIMULATED RESULTS FOR THE ESD DEVICES WITH THE PROPOSED DESIGN UNDER NEGATIVE I-TEST WITH A −200 mA OF CURRENT PULSE

Device	Temperature		
	25°C	75°C	125°C
I_{MP}	159.5mA	91.06mA	28.71mA
I_{MN}	4.51mA	2.96mA	1.58mA
I_{DP}	0.02mA	0.06mA	0.07mA
I_{DN}	32.96mA	98.63mA	158.3mA
ΔV_{PS}	0.45V	1.35V	2.35V

TABLE V
SIMULATED RESULTS FOR THE ESD DEVICES WITH THE PROPOSED DESIGN AND AN ENLARGED M_P UNDER NEGATIVE I-TEST WITH A −200 mA CURRENT PULSE

Device	Temperature		
	25°C	75°C	125°C
I_{MP}	199.2mA	197.2mA	181.6mA
I_{MN}	0.44mA	0.48mA	0.48mA
I_{DP}	0.01mA	0.06mA	0.04mA
I_{DN}	0.12mA	2.04mA	16.78mA
ΔV_{PS}	1.14V	1.05V	1.07V

TABLE VI
DEVICE DIMENSIONS AND RESISTANCE USED IN THE TESTKEYS

Device	ESD Devices with Traditional Guard Ring	ESD Devices with the Proposed Design	ESD Devices with the Proposed Design and enlarged M_P
M_P	(35 μm*16)/ 0.30 μm	(35 μm*13)/ 0.30 μm	(35 μm*25)/ 0.30 μm
M_N	(35 μm*16)/ 0.35 μm	(35 μm*13)/ 0.35 μm	(35 μm*13)/ 0.35 μm
M_{PS}	N/A	(35 μm*3)/ 0.30 μm	(35 μm*3)/ 0.30 μm
M_{NS}	N/A	(35 μm*3)/ 0.35 μm	(35 μm*3)/ 0.35 μm
R_P	3.8 kohm	3.8 kohm	25 kohm
R_N	10 kohm	10 kohm	10 kohm

M_{NS} will be turned on to pull low the gate of M_P. The inversion layer of M_P is generated to provide a low-impedance path and leads the current to V_{DD}. As shown in Table V, the negative trigger current mainly flows into the inversion layer of MOS to prevent excessive substrate current from causing latch-up event in the internal circuits. The detailed device dimensions used in all simulations are listed in Table VI.

According to HSPICE simulation results shown in Tables II–V, the voltage difference (ΔV_{NS}) between V_{Pad} and the gate voltage (V_{GN}) of M_{NS} is not above 1.1-times V_{DD} (3.63 V) and so is the voltage difference (ΔV_{PS}) between V_{Pad} and the gate voltage (V_{GP}) of M_{PS}. Therefore, there is no overvoltage stress issue in this optimization design of the active guard ring to improve latch-up immunity of CMOS integrated circuits.

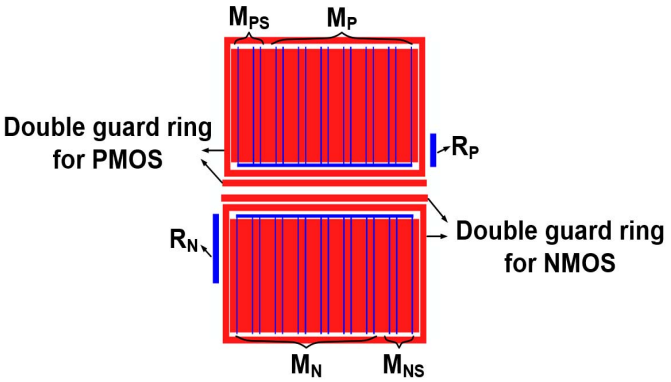

Fig. 5. Layout top view of ESD devices drawn with the proposed optimization design of active guard ring.

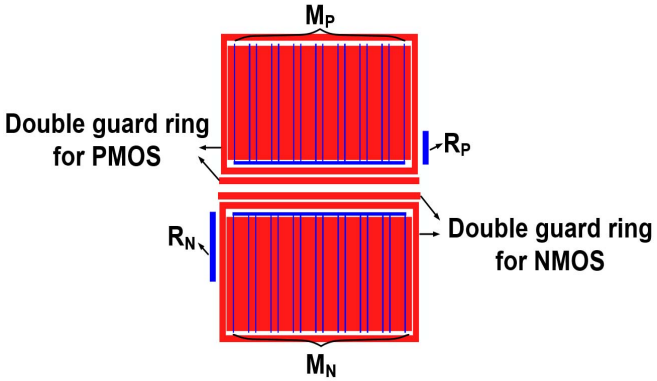

Fig. 6. Layout top view of ESD devices drawn with the traditional guard ring.

To test whether the normal operating I/O signals may mistrigger the proposed design, a signal pulse with a 0.1-ns rising time, a 0.1-ns falling time, a 20-ns pulsewidth, and a 1.1-times pulse voltage of overshoot/undershoot voltage is applied to I/O pad to monitor the gate voltage of each device. All devices in each testkey always are kept in OFF-state, when the overshoot/undershoot signal pulse is applied to I/O pad.

In further optimized layout area of the proposed design, both pMOS devices (M_P and M_{PS}) are placed together and surrounded by guard ring and so are the two nMOS devices (M_N and M_{NS}). The layout top view of the proposed design of the active guard ring is shown in Fig. 5. To compare with the proposed design, the ESD devices composed of a gate-ground nMOS (GGNMOS, M_N) and a gate-V_{DD} pMOS (GDPMOS, M_P) with traditional guard ring is also studied in this paper, and the corresponding layout top view of the traditional design with guard ring is shown in Fig. 6. For the traditional design with guard ring, the total width of GGNMOS is designed to be the same as the total width of all nMOS in the proposed design. Similarly, the total width of GDPMOS is designed to be the same as the total width of all pMOS in the proposed design.

C. Latch-Up Test Structure

Fig. 7 shows the test structure with the external setup of latch-up I-test measurement. The latch-up sensitivity of the

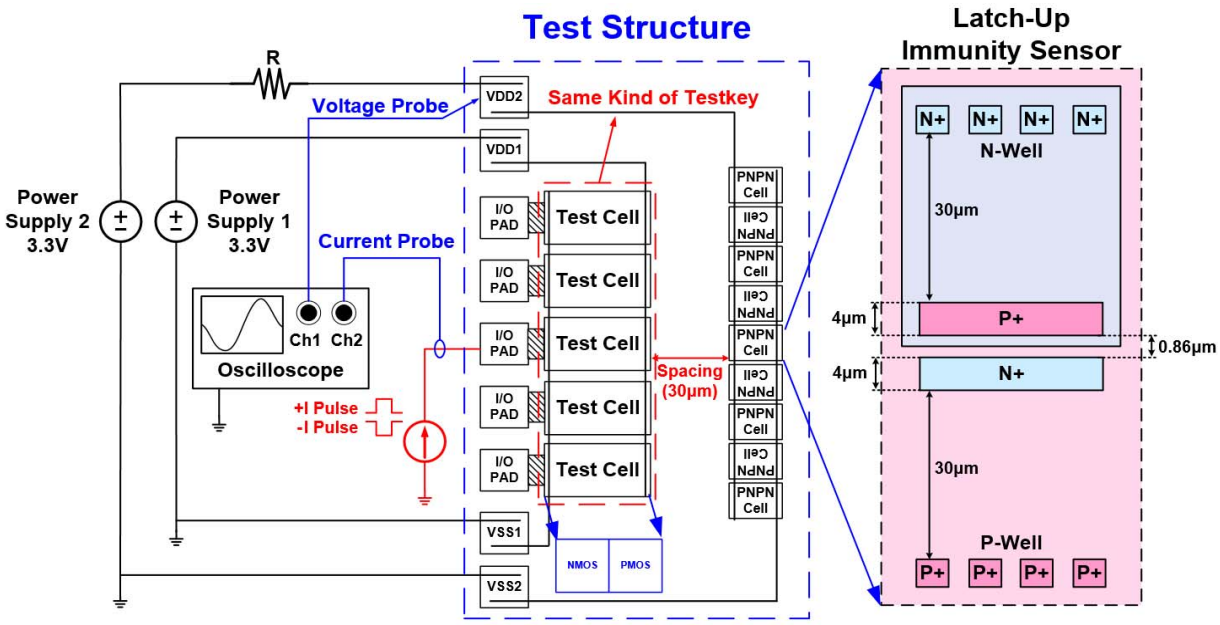

Fig. 7. Latch-up test structure to examine the latch-up immunity of testkey.

internal p-n-p-n cells (latch-up immunity sensor) toward the external trigger source is affected by the testkeys arranged in the test cells, as well as the distance between the test cells and the p-n-p-n cells. The latch-up immunity sensor is composed of a p-n-p-n structure which is drawn with the minimum design rule of 0.86 μm from p+ to n+ diffusions in the given 0.18-μm 1.8-/3.3-V CMOS process, as that indicated in Fig. 7. The test cells are drawn and placed in parallel to p-n-p-n cells with a 30-μm spacing between test cells and the p-n-p-n cells (latch-up immunity sensor). Since the holding voltage of the latch-up immunity sensor drawn with a minimum design rule of 0.86 μm from p+ to n+ diffusions is typically lower than 1 V, a large current will be conducted if the latch-up event happens on the p-n-p-n cells (latch-up immunity sensor) under 3.3-V power supply. As a result, the occurrence of latch-up event can be detected by monitoring the current or voltage waveforms at V_{DD2}. To avoid the burn-out issue on the p-n-p-n cells (latch-up immunity sensor) when the latch-up path is activated, a small resistor (R) of 100 Ω is added between the pad of V_{DD2} and the external power supply (3.3 V), as shown in Fig. 7. To investigate the latch-up immunity, the test methods as described in [15] and [17] are used.

III. Experimental Results

A. Latch-Up Trigger Current Test

The latch-up test structures with different testkeys have been fabricated by 0.18-μm 1.8-/3.3-V CMOS technology. The dc I–V curve of p-n-p-n cell measured by the curve tracer Tek370B is shown in Fig. 8, where the holding voltage is ~0.92 V. The latch-up I-test is specified in the JEDEC standard (JESD78E) to verify the latch-up immunity. The measurement setup applied to the test structure has been shown in Fig. 7 with two 3.3-V power supplies biased to V_{DD1} and V_{DD2} pads, respectively, and V_{SS1} and V_{SS2} pads being grounded. A current pulse generator applied to the I/O pin, and an oscilloscope is used to monitor the waveforms of the V_{DD2} voltage and the injected current pulse. In addition, the V_{DD2} pin is connected in series with a 100-Ω resistor to the 3.3-V voltage source to limit the huge current generated during the latch-up event. The trigger current pulse with a 10-ms pulsewidth is injected into I/O pad to investigate the latch-up occurrence in latch-up immunity sensor under latch-up I-test.

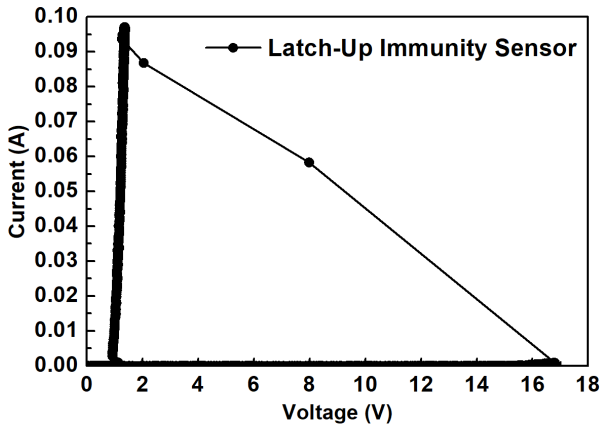

Fig. 8. Measured dc I–V curve of the latch-up immunity sensor with a holding voltage of 0.92 V.

Fig. 9(a) and (b) shows the measured results of the ESD devices (the test cells in Fig. 7) with the proposed optimization design of active guard ring and the traditional guard ring, respectively, under positive I-test with a 50-mA trigger current and a 10-ms pulsewidth applied to the I/O pad. In Fig. 9(a), the trigger current did not generate enough substrate current to induce latch-up in p-n-p-n cells, and therefore, the voltage level at the V_{DD2} pad is still kept at 3.3 V after the latch-up trigger current applied to the I/O pad. However, since the

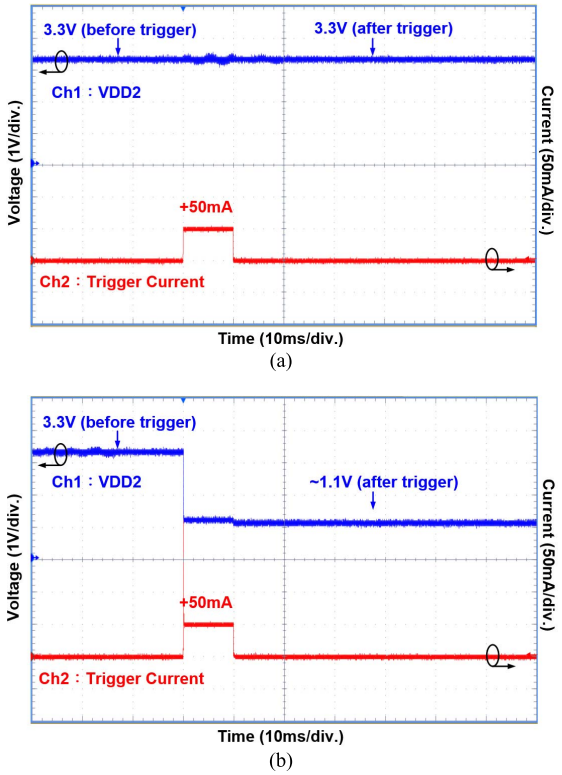

Fig. 9. Measured waveforms of the ESD devices with (a) proposed optimization design of active guard ring and (b) traditional guard ring, under positive I-test with a 50-mA trigger current and a 10-ms pulsewidth applied to the I/O pad.

I/O test cell with traditional guard ring cannot efficiently reduce the injecting substrate current under such a latch-up I-test verification, the voltage level at the V_{DD2} pad is pulled down to 1.1 V, as that shown in Fig. 9(b), where the latch-up occurrence happened in the internal p-n-p-n cells (latch-up immunity sensor).

More detailed examinations to investigate the latch-up immunity are measured by the latch-up tester (Thermo Scientific MK.1) with 10-ms pulsewidth and 5-mA current step. The latch-up positive and negative I-test results for the testkeys with the traditional guard ring, the proposed design (optimization design of active guard ring), and the proposed design with a large-dimensional M_P are shown in Fig. 10(a) and (b), respectively, under different temperatures. According to these figures, the optimized design of active guard ring shows a higher latch-up immunity level than that with the traditional guard ring, under both positive and negative I-test. Moreover, the negative latch-up immunity of the proposed design somewhat degrades at high temperature because p-n-p-n cells are far away from M_N, where the negative current mainly injects into p-substrate. Even if more trigger current is injected into p-substrate, the guard rings placed between M_N and latch-up immunity sensors will absorb this substrate current. In addition, the proposed design with large-dimension M_P really improves the latch-up immunity level under negative I-test.

After the current pulse is applied to the I/O pad to investigate the latch-up immunity level, Emission Microscope (EMMI) analysis is taken to show the location of the

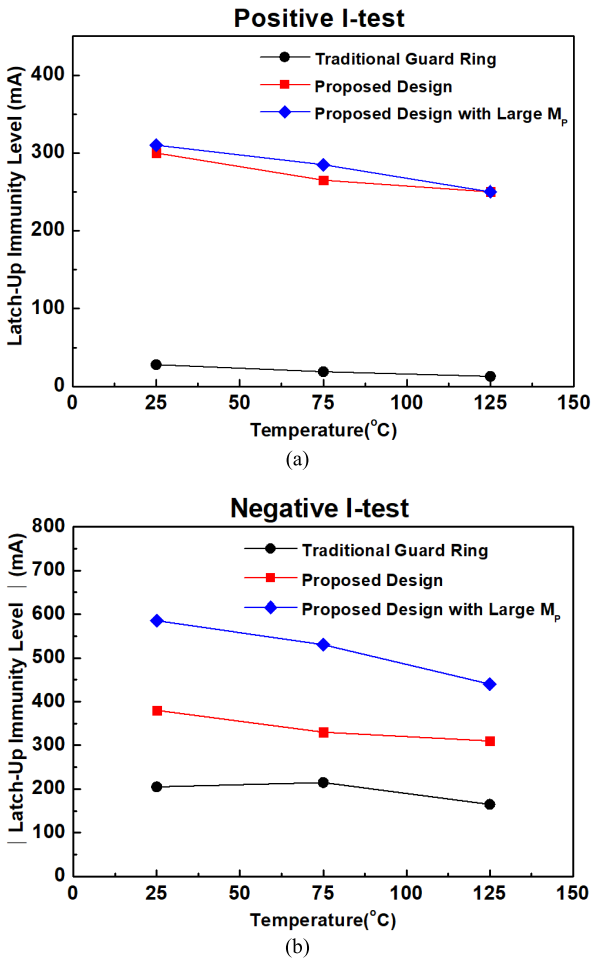

Fig. 10. Latch-up immunity levels of the testkeys at different temperatures under (a) positive and (b) negative I-test.

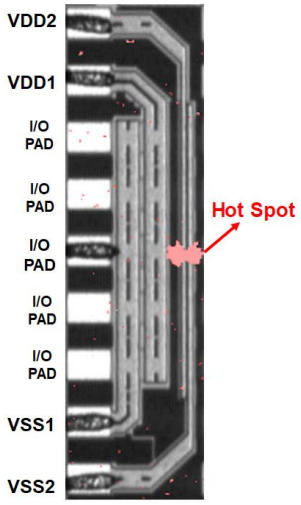

Fig. 11. EMMI photograph of the latch-up test result for the I/O pad of test cell with traditional guard ring under 30-mA positive current pulse.

abnormal current. Fig. 11 shows the EMMI photograph of the latch-up test result for the test cell with a traditional guard ring under 30-mA positive current pulse. The location of hot spot is at the nearest p-n-p-n cell from the I/O pad of the test cell where the trigger current is applied to.

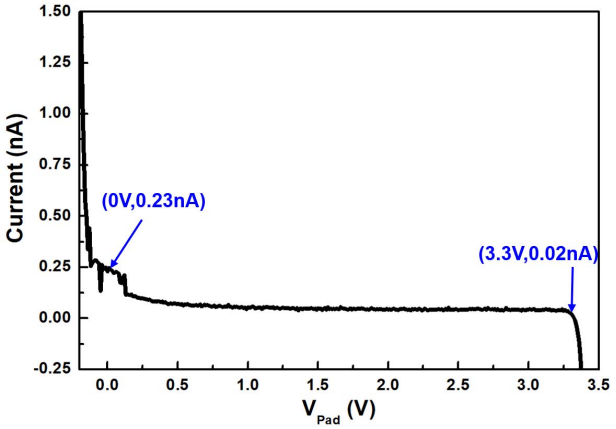

Fig. 12. Measured waveforms of standby current on the I/O pad of test cell with the proposed optimization design of active guard ring under dc sweep of V_{Pad} from −0.5 to 3.5 V.

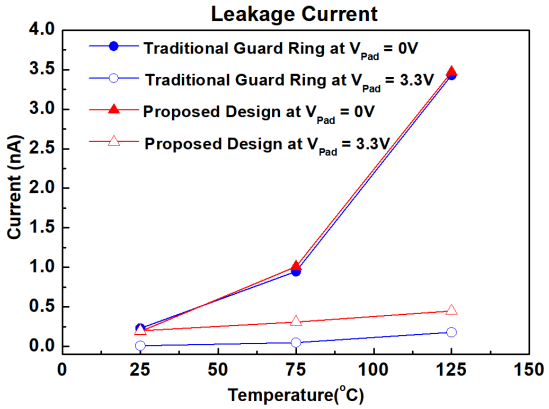

Fig. 13. Standby leakage current on the I/O pad of test cell (ESD devices) with the proposed optimization design of active guard ring or the traditional guard ring when V_{Pad} biased at 0 –3.3 V, respectively, under different temperatures.

B. Leakage Current

To observe the leakage current under different voltage levels at the I/O pad (V_{Pad}) and temperatures, the measurement equipment of Keysight 4156C was used. The measured waveforms of standby current on the I/O pad of test cell with the proposed optimization design of active guard ring under dc sweep of V_{Pad} from −0.5 to 3.5 V is shown in Fig. 12. In comparison with the prior art [16], there is no diode string providing the voltage reference in the proposed design. The standby current of I/O pad of test cell (ESD devices) with the proposed design is almost the same as that of I/O pad of test cell with traditional guard ring, as shown in Fig. 13, where the leakage currents are captured with the V_{Pad} biased at 0 or 3.3 V under different temperatures. The device dimensions of ESD devices in the I/O pads of test cells with the proposed active guard ring design or the traditional guard ring have been listed in Table VI, where the total device dimensions and the drain diffusions (connected to the I/O pad) in layout are kept the same for this leakage current comparison.

C. ESD Robustness

The ESD robustness of the I/O cells with the optimized active guard ring design and the traditional guard ring is tested with a commercial ESD tester (HED-W5100D) for the human-body model (HBM). The ESD levels of I/O cells (with ESD devices) of all testkeys under PS (positive-to-V_{SS}) mode and ND (negative-to-V_{DD}) mode of HBM ESD stresses are listed in Table VII. The HBM levels of I/O cells (ESD devices) with the proposed optimization active guard ring design are even better, in comparison with that with traditional guard ring, when the ESD levels are normalized to the silicon area of ESD devices. Especially in the ND mode, the ESD robustness of the I/O cells (ESD devices) with the proposed optimization active guard ring design is more improved.

TABLE VII
ESD ROBUSTNESS OF THE I/O CELLS (ESD DEVICES) WITH ALL TESTKEYS UNDER PS-MODE AND ND-MODE HBM ESD TEST

Testkeys		ESD Devices with Traditional Guard Ring	ESD Devices with the Proposed Design
Dimension of ESD devices	M_P	35 μm*16	35 μm*13
	M_N	35 μm*16	35 μm*13
HBM ESD-Stress mode	PS mode	7.8kV	6.4kV
	ND mode	-4.6kV	-5.8kV
HBM/Area of ESD devices	PS mode	3.43V/μm²	3.46V/μm²
	ND mode	-2.02V/μm²	-3.14V/μm²

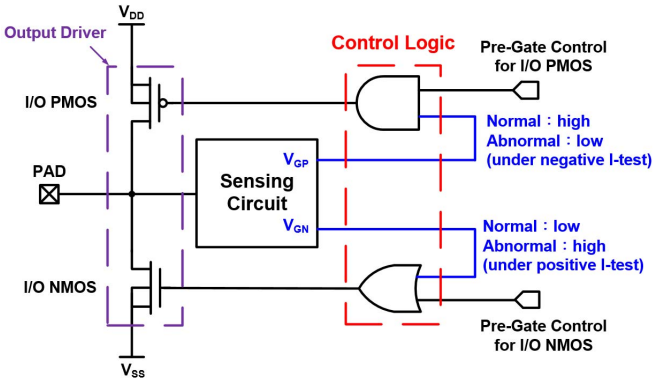

Fig. 14. Concept of the output driver codesigned with the proposed optimization active guard ring design (sensing circuit) and the control logic.

IV. APPLICATIONS

The proposed active guard ring design can also be applied to the output drivers. The concept of the output driver codesigned with the proposed active guard ring and the control logic is shown in Fig. 14. An "AND" gate is added between V_{GP} of the sensing circuit and the pregate control for I/O pMOS of the output driver. Furthermore, an "OR" gate connects between V_{GN} of the sensing circuit and the pregate control for I/O nMOS of the output driver. The sensing circuit has been shown in Fig. 3, which is surrounded by a red dashed line. Under normal circuit operation, V_{GP} is kept at logic "1" and V_{GN} is kept at logic "0." During latch-up I-test, the logic states of V_{GP} and V_{GN} will be changed by the sensing circuit to run the function of "active guard ring." When a negative I-test is applied to the output pad, V_{GP} will be pulled low due to the operation of the sensing circuit (active guard ring), which in turn turns

on the I/O pMOS. Therefore, some positive current will flow from V_{DD} to the pad through the channel of I/O pMOS, and to compensate the negative current injected to the pad. On the contrary, when a positive I-test is performed on the output pad, V_{GN} will be pulled high due to the operation of sensing circuit (active guard ring), which in turn turns on the I/O nMOS. Therefore, the positive latch-up trigger current applied to the pad will be conducted to V_{SS} through the channel of I/O nMOS and to compensate the positive current injected to the pad. Hence, the latch-up trigger current injecting into p-substrate can be reduced significantly. The overall latch-up immunity of the output driver can be effectively improved. Moreover, the spacing between I/O cells and core circuits can be closer to reduce the chip area, as well as the latch-up immunity is not degraded. The circuit implementation of the control logic in Fig. 14 with the inputs of V_{GP}, V_{GN}, and the pregate control signals should be carefully designed with tapped buffer to drive the large-dimensional MOSFETs in the output driver.

V. Conclusion

The new proposed optimized active guard ring design has been successfully verified to improve latch-up immunity of CMOS ICs in 0.18-μm 1.8-/3.3-V CMOS technology. The new proposed design can further save 42% silicon area and not suffer standby leakage current, as compared to the prior work [16]. The layout to enable the proposed optimization active guard ring design from the I/O cell with traditional guard ring can be simply achieved by changing the metal connection to the gates of ESD devices (GGNMOS and GDPMOS) with the resistors R_P–V_{DD} and R_N–V_{SS}, respectively. In other words, if the latch-up immunity level of some I/O cells in a CMOS IC did not meet the requested specification of applications, the proposed optimization active guard ring design will be a cost-efficient solution for latch-up immunity improvement. In addition, the ESD robustness of I/O cells can become even better, when the optimization active guard ring design is applied on the I/O cells.

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