Design of High-Voltage-Tolerant Power-Rail ESD Protection Circuit for Power Pin of Negative Voltage in Low-Voltage CMOS Processes

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***Abstract*— In the implanted biomedical devices, the silicon chips with monopolar stimulation design have been widely applied. To protect the negative-voltage pins of the implanted silicon chip from the electrostatic discharge (ESD) damage, the ESD protection circuit should be carefully designed to avoid any wrong current path under normal circuit operation with the negative voltage. In this article, a new power-rail ESD clamp circuit for the application with an operating voltage of −6 V has been proposed and verified in a 0.18-μm 3.3-V CMOS process. The proposed circuit, realized with only 3.3-V nMOS/pMOS devices, is able to prevent the gate-oxide reliability issue under this −6-V application. With the proposed ESD detection circuit, the turn-on speed of the main ESD clamp device, which is a stacked-nMOS (STnMOS), can be greatly enhanced. The STnMOS with a width of 400 μm can sustain over 8-kV human body model (HBM) ESD stress and perform low standby leakage current of ∼5.4 nA at room temperature under the circuit operating condition with −6-V supply voltage.**

***Index Terms*— Electrostatic discharge (ESD), high-voltage-tolerant ESD clamp circuit, negative voltage supply, power-rail ESD clamp circuit.**

I. Introduction

IN RECENT years, the implanted biomedical devices are used to treat a variety of neurodiseases or disorders. More and more implantable medical devices have been employed with stimulation function. In the multitude of architectures, a pair of positive and negative stimulus pulses is defined as biphasic stimulation. According to the electrode configuration, the stimulus methodologies are divided into two groups [1]: one with two leads per site (bipolar stimulation) and the other with one lead per site (monopolar stimulation). Among them, dual supply voltage configuration is requested to generate the anodic and cathodic stimulation for the monopolar architecture. Therefore, both positive- and negative-voltage supplies are required in such monopolar stimulation [2], [3]. The monopolar biphasic simulators realized in the various processes had been reported [4]–[6]. Fig. 1 shows the diagram of a monopolar stimulator. The local digital controller is supplied with pads of VDD and GND. To convert the signals from the digital controller, the positive-voltage digital-to-analog converter (DAC) and the negative-voltage DAC are designed for the stimulus driver circuit. The supply voltages of the positive-voltage DAC are biased with VDDH and GND. Meanwhile, the negative-voltage DAC is supplied with the power supplies of GND and VSSH. In this design, the voltage level of VDDH is 2 × VDD (+6 V) and VSSH is −2 × VDD (−6 V). After the signal process through the DAC, the signals are delivered to the stimulus driver circuit.

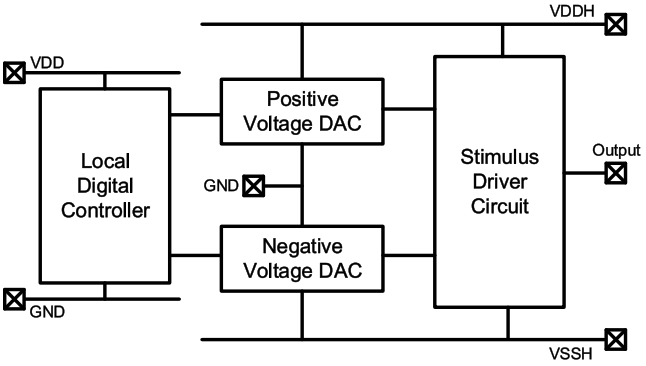

Fig. 1. Diagram of the monopolar stimulator.

According to the requirement of high reliability for the implanted biomedical devices, the power-rail electrostatic discharge (ESD) clamp circuits should be installed between VDDH and GND pads and between GND and VSSH pads to avoid the damage caused by ESD stresses [7]. Furthermore, the ESD protection circuits of those pins should be able to sustain high operating voltage. Although the high-voltage-tolerant ESD protection circuit for positive voltage has been proposed in some prior works [8]–[11], the ESD

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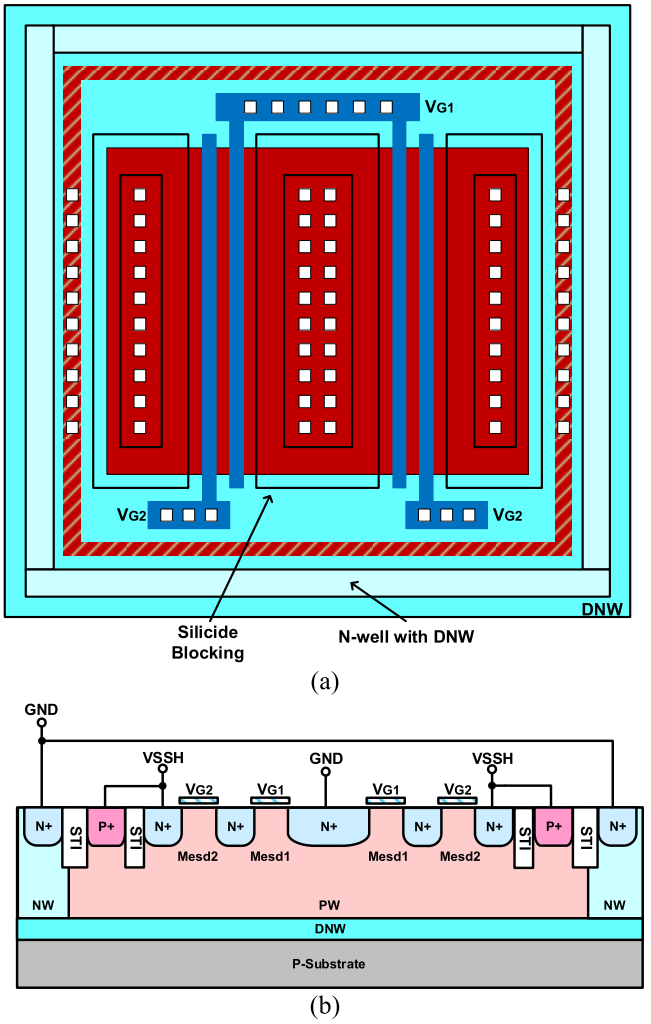

Fig. 2. (a) STnMOS drawn in the type-A layout style. (b) Corresponding cross-sectional view of the type-A STnMOS device.

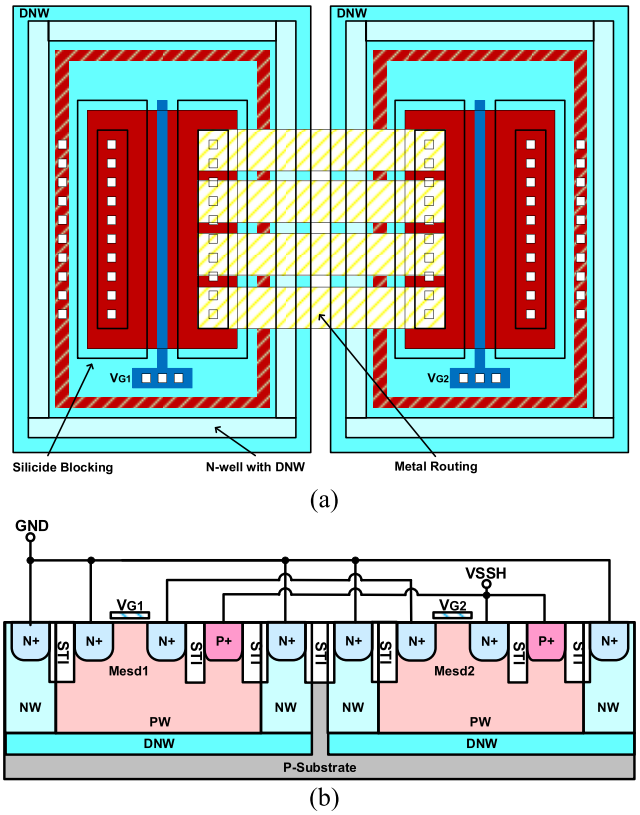

Fig. 3. (a) STnMOS drawn in the type-B layout style. (b) Corresponding cross-sectional view of the type-B STnMOS device.

protection circuit that operates under negative voltage supply with common-grounded p-type substrate was never reported.

In this article, a new 2 × VDD-tolerant power-rail ESD clamp circuit for power pin of negative voltage is proposed. The new power-rail ESD clamp circuit is implemented with 3.3-V nMOS/pMOS devices, which can meet the −6 V application without suffering gate-oxide reliability issue. Besides, the ESD detection circuit in the proposed circuit can greatly enhance the turn-on efficiency of the main ESD clamp device.

II. New Power-Rail ESD Clamp Circuit for Power Pin of Negative Voltage

A. Stacked-nMOS Device

In order to meet the gate-oxide reliability during the normal circuit operating condition with VSSH of −6 V, the ESD clamp device is composed of two 3.3-V nMOS devices in the stacked configuration.

The stacked-nMOS (STnMOS) drawn in the type-A layout style and the corresponding cross-sectional view of the type-A STnMOS device are shown in Fig. 2, which includes one pair of nMOS transistors connected in a stacked configuration [12]. The type-A STnMOS device includes a first transistor (Mesd1), having a drain connected to the GND and a gate (V_{G1}) connected to the VSS (−3 V) through a resistor. A second nMOS transistor (Mesd2) of the nMOS transistor pair is merged into the same active area of the Mesd1, having a gate (V_{G2}) connected to the VSSH (−6 V) through a resistor. The drain of Mesd2 and the source of Mesd1 share the common N+ diffusion region in the type-A layout style. Silicide blocking option which is supported by foundry is used to improve the ESD robustness of the ESD clamping STnMOS [13]. The STnMOS is isolated from the common P-substrate by n-well (NW) and deep n-well (DNW), which is biased to GND (0 V).

In order to increase the holding voltage (V_h) of STnMOS device for high-voltage application, a STnMOS drawn in the type-B layout style is realized to compare with that of the type-A STnMOS device. Fig. 3 shows the STnMOS drawn in the type-B layout style and the corresponding cross-sectional view of the type-B STnMOS device. The type-B STnMOS device includes a first transistor (Mesd1), having a drain connected to the GND and a gate (V_{G1}) connected to the VSS through a resistor and a second nMOS transistor (Mesd2), having a drain connected to the source of the Mesd1 by the metal routing and a gate (V_{G2}) connected to the VSSH through a resistor. The layout area of the type-B STnMOS device would be larger than that of the type-A STnMOS device due to the isolation rings those individually surrounding the ESD devices. The Mesd1 and Mesd2 in the type-B layout

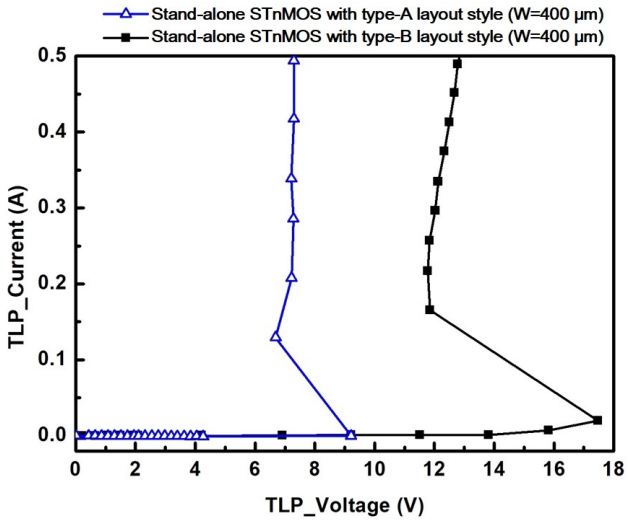

Fig. 4. Zoomed-in view of TLP-measured *I–V* characteristics between the stand-alone type-A STnMOS device and the stand-alone type-B STnMOS device under a positive GND-to-VSSH TLP stress.

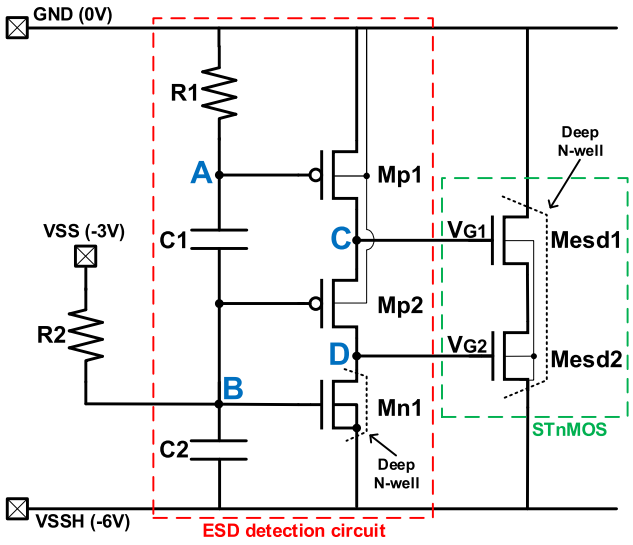

Fig. 5. Proposed 2 × VDD-tolerant power-rail ESD clamp circuit with 3.3-V devices for the negative voltage supply of −6 V at VSSH pin.

are implanted in the separated p-wells, which can cause a higher total holding voltage (V_h) on STnMOS for high-voltage application.

The transmission-line-pulsing (TLP)-measured I–V characteristics of the stand-alone STnMOS devices with type-A and -B layout styles are shown in Fig. 4. The holding voltage (V_h) of the stand-alone type-A STnMOS device is around 7 V. On the other hand, the holding voltage (V_h) of the stand-alone type-B STnMOS device is around 12 V, which is too high for 0 to −6-V power pin application. Thus, the STnMOS device with type-A layout style is selected as the main ESD clamp device in the proposed power-rail ESD clamp circuit.

B. Circuit Implementation

To ensure that the power-rail ESD clamp circuit can be correctly operating under the power pin of negative voltage, any parasitic path in the devices should be carefully considered. A new power-rail ESD clamp circuit for the negative voltage supply is proposed and shown in Fig. 5. The main ESD clamp device is a STnMOS with type-A layout style. The ESD detection circuit is realized with gate-driven technique to turn on the STnMOS during ESD stress. The STnMOS with the gate-driven circuit can be turned on first in the MOS mode and then in the bipolar mode to discharge the ESD current [14]. The typical RC time constant of 100 ns is selected with the resistor R_1 of 100 kΩ and the total capacitance of 1 pF (C1 in series with C2, C1 = C2 = 2 pF) [15]. To avoid node B floating, a resistor R_2 of 100 kΩ is connected to VSS (−3 V). The VSS is connected to the same bias with internal circuits. To investigate the impact of the main ESD device size on the ESD robustness, the channel width of Mesd1 (Mesd2) is drawn with 400, 600, and 800 μm, respectively. The PMOS Mp1 and Mp2 are used to control the dual gates of STnMOS. Node C which is connected to the drain of Mp1 and source of Mp2 is used to control the gate (V_{G1}) of Mesd1.

TABLE I
DESIGN PARAMETERS OF THE PROPOSED POWER-RAIL ESD CLAMP CIRCUIT

Capacitor (pF)	Resistor (Ω)	PMOS W/L (μm/μm)	NMOS W/L (μm/μm)	Main ESD clamping STnMOS W/L (μm/μm)
C1=2 pF C2=2 pF	R1=100 k R2=100 k	Mp1=200/0.3 Mp2=200/0.3	Mn1=50/0.35	400/1 600/1 800/1

Node D which is connected to the drain of Mp2 and Mn1 is used to control the gate (V_{G2}) of Mesd2. The channel widths of Mp1 and Mp2 are both selected as 200 μm to have STnMOS triggered on promptly during ESD stress. To isolate the bulk (p-well) of STnMOS and Mn1 from the grounded P-substrate, the isolation ring configured with NW and DNW is used. The design parameters of the device dimensions in the proposed power-rail ESD clamp circuit are listed in Table I.

C. Circuit Simulation

1) ESD-Like Waveform Condition: In the simulation of ESD-like waveform, the rising time of 10 ns and the pulsewidth of 100 ns are selected on the basis of a human body model (HBM) [16]. In order to simulate the circuit function under HBM ESD event before the nMOS drain breakdown, the voltage of ESD-like waveform is selected as 6 V. Fig. 6 shows the simulated transient voltage on each node of the proposed circuit. When a positive ESD voltage is applied to the GND node with VSSH grounded and VSS floating, the voltage at nodes A and B was kept at a low level due to the RC time delay. Then, the devices Mp1 and Mp2 are turned on and make the voltage levels of nodes C and D rise to the voltage of the applied ESD-like waveform. Thus, Mesd1 and

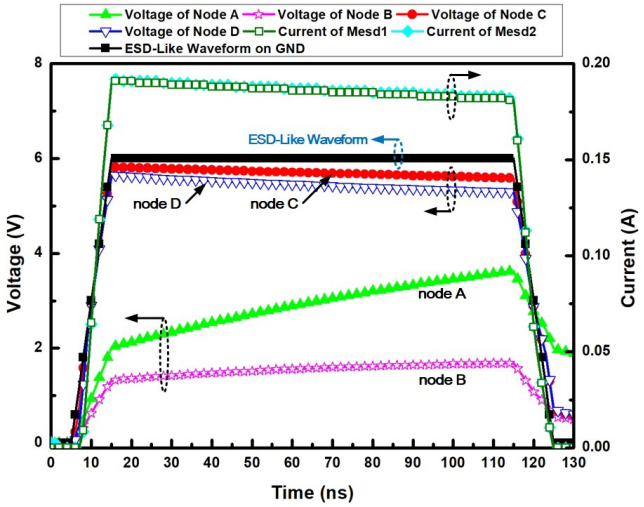

Fig. 6. HSPICE-simulated waveforms on the node voltages of the ESD detection circuit and the current through the STnMOS device, when a 0–6-V ESD-like voltage pulse is applied.

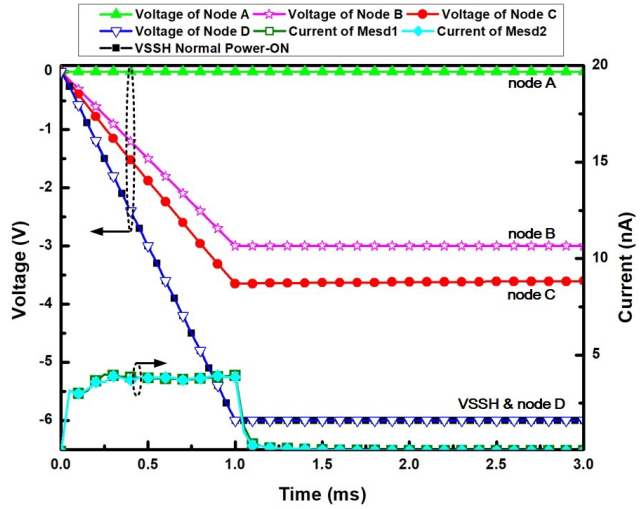

Fig. 7. HSPICE-simulated waveforms on the node voltages of the ESD detection circuit and the leakage current of the STnMOS device under the normal power-ON condition with GND of 0 V, VSS of −3 V, and VSSH of −6 V.

Mesd2 are turned on when the voltage levels at their gates are raised above the threshold voltage. Finally, the ESD current is conducted through STnMOS from GND to VSSH. Fig. 6 also shows the simulated currents of Mesd1 and Mesd2 under the ESD transient event to prove that the ESD current can be discharged by the proposed circuit.

2) Normal Power-ON Condition: Fig. 7 shows the simulation voltage on each node and leakage current of the proposed circuit under normal power-ON condition. During the normal circuit operation condition with GND of 0 V, VSS of −3 V, and VSSH of −6 V, node B is biased at −3 V to turn on Mn1. The normal power-ON voltage waveform typically has a rising time in the order of millisecond (ms), so the rising time of normal power-ON condition is chosen as 1 ms. The voltage at node A can follow the GND voltage in time due to the slow-rising power-ON voltage. On the other hand, Mp1 is

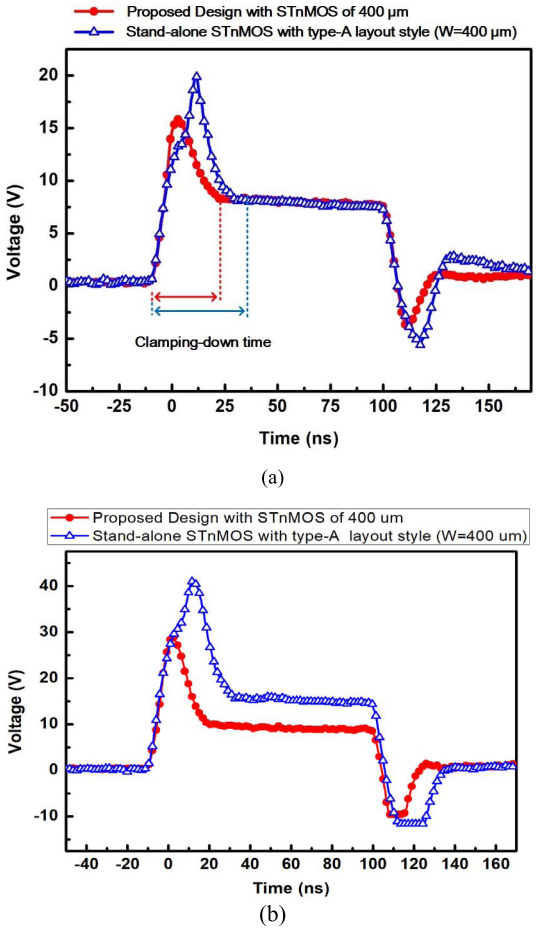

Fig. 8. Measured voltage waveforms clamped by the stand-alone type-A STnMOS device and the proposed ESD clamp circuit (a) by applying a 15-V TLP pulse and (b) by applying a TLP current around 1 A from GND to VSSH.

kept in the OFF state, and no current flows from GND through Mp1, Mp2, and Mn1 to VSSH. The voltage levels of nodes C and D are about −3.5 and −6 V, respectively. Therefore, the STnMOS is kept in OFF state. Only a little leakage current of nanoampere flowing through the STnMOS from GND to VSSH is found at the rising period of the normal power-ON condition. From the simulation result, the voltage differences across the gate-to-source, gate-to-drain, and gate-to-bulk terminals of all devices in the proposed ESD detection circuit did not exceed the process limitation (3.63 V for 3.3-V device in a 0.18-μm CMOS process). Therefore, under the normal circuit operating condition, the ESD detection circuit can be ensured against the gate-oxide reliability issue.

III. Experimental Results

The width of STnMOS devices in the ESD clamp circuit is varied with 400, 600, and 800 μm in the test chip to verify the corresponding ESD robustness. The resistors are realized by the p-type poly resistors, and the capacitors are adopted by the metal–insulator–metal capacitors.

A. Turn-on Verification

The turn-on speed of an ESD clamp device during the ESD stress condition can be enhanced by the proposed

TABLE II
ESD ROBUSTNESS OF THE PROPOSED 2 × VDD-TOLERANT POWER-RAIL ESD CLAMP CIRCUIT WITH DIFFERENT WIDTH STnMOS DEVICES AND THE STAND-ALONE STnMOS DEVICE

Device Name	Width of nMOS	I_{t2} Current	HBM ESD Level
Proposed 2×VDD-tolerant power-rail ESD clamp circuit with type-A layout style	400 μm	4.57 A	>8 kV
	600 μm	6.92 A	>8 kV
	800 μm	8.21 A	>8 kV
Stand-alone STnMOS with type-A layout style	400 μm	3.54 A	6.5 kV

2 × VDD-tolerant power-rail ESD clamp circuit. The voltage waveform measured by the TLP system on the GND pin clamped by the ESD clamp circuit is shown in Fig. 8(a) and (b). By using the type-A STnMOS device, the applied 15-V TLP pulse can be clamped down to about 7.5 V. Although the type-A STnMOS device with or without ESD detection circuit clamped the pulse voltage to the same voltage level (∼7.5 V), the STnMOS with the ESD detection circuit can clamp down the overshooting voltage faster. In this article, the clamping-down time is defined as the demand time of voltage dropping down to the holding voltage (V_h), as that marked in Fig. 8(a). The clamping-down time of the stand-alone STnMOS device with type-A layout style is about 36.08 ns. On the other hand, the clamping-down time of the proposed ESD clamp circuit, which has an ESD detection circuit, is about 27.72 ns. The overshooting peak voltage of the proposed ESD clamp design is also lower than that of the stand-alone STnMOS; therefore, the internal circuits can have lower risk to the gate-oxide overstress issue.

Fig. 8(b) shows the measured voltage waveforms clamped by the stand-alone type-A STnMOS device and the proposed ESD clamp circuit, when the TLP current is around 1 A. The overshooting voltage difference between them is more than 10 V, so the proposed design can provide better ESD protection performance and capability to protect the internal circuits than that of the stand-alone STnMOS device. From the measured overshooting voltage waveforms in Fig. 8(a) and (b), the turn-on speed of the STnMOS device can be indeed improved by the proposed ESD detection circuit.

B. ESD Robustness

The failure criterion was defined with 20% variance from the original leakage current under 6-V bias after three continuous ESD zaps at every ESD test level. Table II shows the results of ESD test on the proposed circuit and the stand-alone STnMOS device. The HBM ESD robustness of the proposed 2 × VDD-tolerant power-rail ESD clamp circuit with the STnMOS width of 400, 600, and 800 μm is over 8 kV.

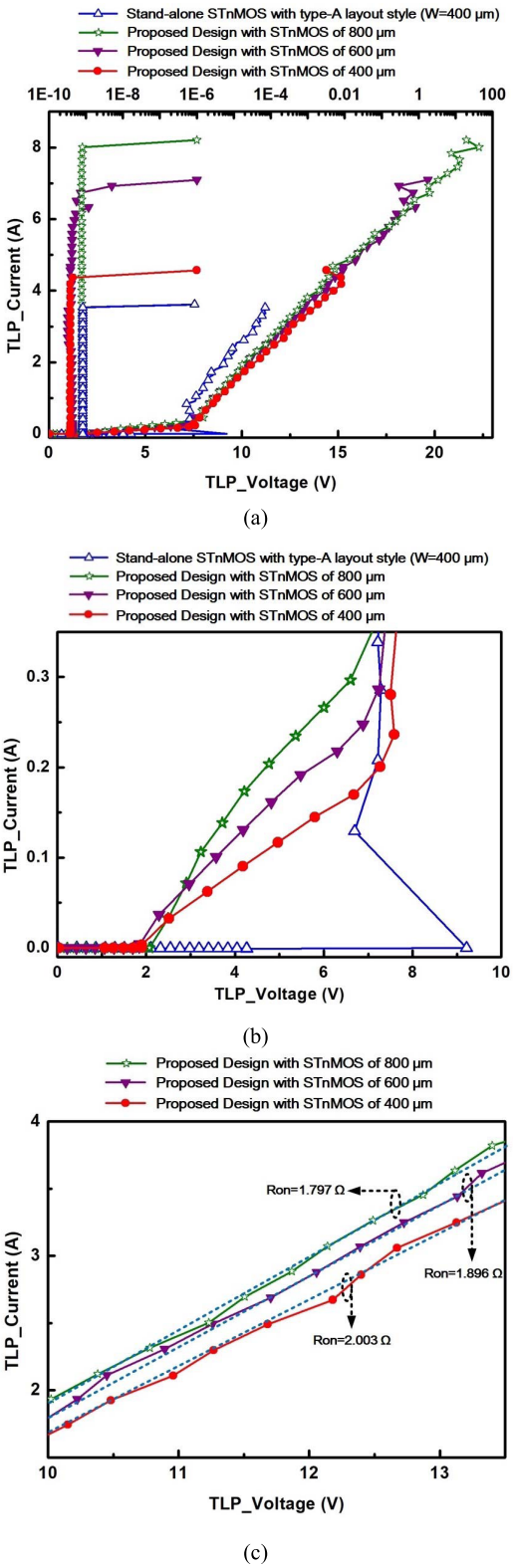

Fig. 9. (a) TLP-measured *I–V* characteristics of the proposed 2 × VDD-tolerant power-rail ESD clamp circuit with STnMOS device of different widths and the stand-alone STnMOS device under positive GND-to-VSSH TLP stress. (b) Zoomed-in view for investigating the trigger voltage (V_{t1}). (c) Zoomed-in view for investigating the turn-on resistance (R_{on}).

The HBM ESD robustness of the stand-alone type-A STnMOS device can only reach 6.5 kV. The proposed circuit assisted with the ESD detection circuit can reach a better ESD level.

C. TLP Measurement

To investigate the I–V characteristics of the proposed circuit during HBM ESD stress, the TLP generator [17] with a pulsewidth of 100 ns and rising time of 10 ns is used to measure the second breakdown current (I_{t2}) of the proposed 2 × VDD-tolerant power-rail ESD clamp circuit. Fig. 9(a) shows the TLP-measured I–V characteristics of the proposed ESD clamp circuit with STnMOS of different widths under positive GND-to-VSSH TLP stress. The TLP measured I–V curves of the stand-alone STnMOS in type-A layout style are also shown in Fig. 9(a). In Fig. 9(b), the stand-alone type-A STnMOS device has the snapback phenomenon because the device is triggered on by the junction breakdown operation of the parasitic BJT. The trigger voltage (V_{t1}) of the type-A STnMOS device is 9.2 V. V_{t1} of the proposed 2 × VDD-tolerant power-rail ESD clamp circuit with different nMOS widths is about 2.4 V. The holding voltages (V_h) of the proposed 2 × VDD-tolerant power-rail ESD clamp circuit and the stand-alone type-A STnMOS device are around 7 V. The holding voltage (V_h) is higher than the voltage level of GND-to-VSSH (0 to −6 V) under the normal circuit operating condition. Thus, the proposed 2 × VDD-tolerant power-rail ESD clamp circuit is free from the latchup issue in the circuit applications with the voltage level of GND-to-VSSH as 0 to −6 V. Fig. 9(c) also shows the zoomed-in view on the TLP-measured I–V characteristics from 10 to 13.5 V. Three dashed lines have been added to the figure with the calculated R_{on} of each line. R_{on} of the proposed design with STnMOS of 400, 600, and 800 μm is 2.003, 1.896, and 1.797 Ω, respectively. The STnMOS with a larger device size indeed has a smaller value of R_{on}. The test chip fabricated in silicon to verify this article with the proposed ESD clamp circuit and the STnMOS device was limited to the available silicon area. The metal routing that connected the test device/circuit to the bond pad was longer. The layout issue in this article may cause some effect on the value of R_{on}. Thus, the difference between the values of R_{on} among the designs with three device dimensions was not so obvious in Fig. 9(a).

The second breakdown currents (I_{t2}) of the proposed ESD clamp circuit and the stand-alone STnMOS device are also listed in Table II. The I_{t2} current of the proposed 2 × VDD-tolerant power-rail ESD clamp circuit with STnMOS width of 400, 600, and 800 μm is 4.57, 6.92, and 8.21 A, respectively. Therefore, the proposed 2 × VDD-tolerant power-rail ESD clamp design with type-A layout style has a good ESD robustness, fast turn-on speed, and without latchup issue.

D. Leakage Current

Fig. 10 shows the dc I–V curves of the proposed 2 × VDD-tolerant power-rail ESD clamp circuit with type-A STnMOS device at low (25 °C) and high (125 °C) temperatures. The applied VSSH voltage is swept from 0 to −6 V, and the leakage current at −6 V is specially noticed. In Fig. 10, the leakage current of the proposed ESD clamp circuit was increased around −5 V, but still kept in the nanoampere level.

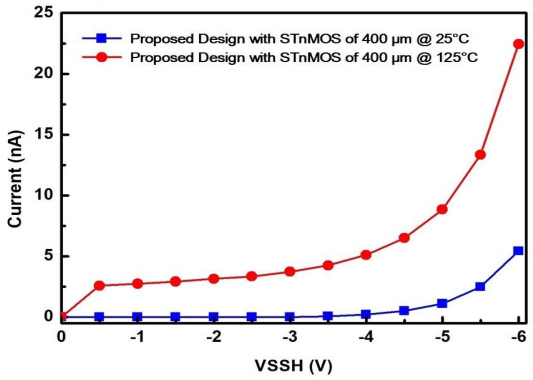

Fig. 10. Leakage currents of the proposed 2 × VDD-tolerant power-rail ESD clamp circuit with type-A STnMOS device at 25 °C and 125 °C.

The measured leakage currents of the proposed ESD clamp circuit at 25 °C and 125 °C are 5.4 and 22.4 nA, respectively. According to the measured results, the proposed ESD clamp circuit can effectively keep the leakage current of STnMOS under a very low level.

IV. Conclusion

A 2 × VDD-tolerant power-rail ESD clamp circuit for power pin of negative voltage with STnMOS has been successfully verified in a 0.18-μm 3.3-V CMOS process, which is realized with only 1 × VDD devices without suffering the gate-oxide reliability issue. The standby leakage current of the proposed 2 × VDD-tolerant power-rail ESD clamp circuit under −6-V operating condition is as low as 5.4 nA at 25 °C. The newly proposed 2 × VDD-tolerant power-rail ESD clamp circuit is a good solution to enhance the ESD robustness of implanted biomedical devices, which have the power pin of negative voltage.

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