On-Chip Over-Voltage Protection Design Against Surge Events on the CC Pin of USB Type-C Interface

Chao-Yang Ke and Ming-Dou Ker, *Fellow, IEEE*

***Abstract*— As fast charging being a comprehensive application in universal serial bus (USB) type-C products, the high-power delivery may cause the USB type-C interface in the high risk of surge events. Therefore, a switch realized by high voltage N-type metal oxide semiconductor transistor (HVNMOS) has been added to the configuration channel (CC) pin to prevent the internal circuits from surge damage. However, hot carrier degradation (HCD) on the HVNMOS was induced by surge events, especially when the HVNMOS was operating in the ON-state. To mitigate HCD on the HVNMOS switch during surge events, a new over-voltage protection (OVP) design with selected voltage-level detection was proposed and verified in a 0.15-μm BCD technology. The proposed OVP circuit with a positive feedback is designed to turn off the gate of the HVNMOS switch for a longer time when surge zapping on the CC pin. The experimental results from silicon chip have successfully verified the proposed OVP structure in device level and circuit level, respectively.**

***Index Terms*— Electrical overstress (EOS), hot carrier degradation (HCD), overvoltage protection (OVP), surge protection, surge test, universal serial bus (USB) type-C.**

I. Introduction

USB type-C interface recently has become popular and drawn much attention due to the advantages of high power delivery, fast charging, and high-speed data transmission. According to the universal serial bus (USB) type-C specification [1], [2], in power delivery mode, the maximum voltage level and driving current of the V_{BUS} pin can increase up to 20 V and 5 A, respectively. Such high power delivery application makes the USB type-C interface system to be in the risk of surge damage. Thus, not only USB type-C products were done with ESD testing, but they were also requested with surge testing.

For surge immunity testing, International Electrotechnical Commission's international standard (IEC 61000-4-5) has defined the method with test procedures to investigate the surge immunity with both positive and negative surges for electronic devices [3]. The measured surge waveform of the calibrated open-circuit voltage with 28-V peak voltage is shown in Fig. 1, with the front time of 1.2 μs and the duration time of 50 μs. Such a calibrated open-circuit voltage surge is used in this work to investigate the hot carrier degradation (HCD) of the high voltage N-type metal oxide semiconductor transistor (HVNMOS) in device level and the circuit operation of the proposed over-voltage protection (OVP) structure in circuit level.

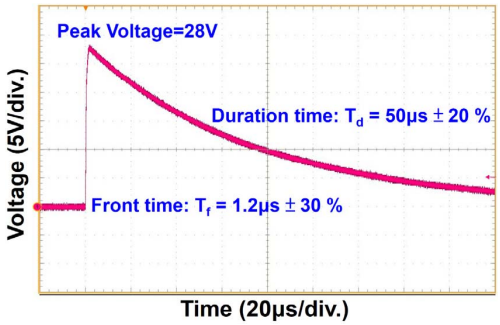

Fig. 1. Calibrated 1.2/50-μs open-circuit voltage surge waveform with a 28-V zapping voltage.

The configuration channel (CC) pin in the USB type-C interface plays an important role of system protocol, including detecting attachment of USB ports, resolving cable orientation, and twist connections to establish USB data bus routing, discovering, and configuring V_{BUS}, as well as configuring V_{CONN} mode, alternate mode, and accessory mode. Therefore, if the function of the CC pin was wrong, the battery charging or power supply for electronic devices could not work correctly, which may cause the whole electronic system in a dangerous situation. As a result, the reliability of the CC pin is really critical. Although the discrete transient voltage suppressor (TVS) device adding to the CC pin on the printed circuit board (PCB) had been a solution, on-chip OVP design is still strongly desired by industry for safety consideration. In recent years, some methods have been proposed against electrical overstress (EOS) or surge events for USB type-C interfaces [4]–[9].

In this article, a novel OVP structure with the concept of voltage-level detection was proposed as shown in the block diagram (Fig. 2). In order to limit the overstress voltage entering into the CC pin of USB type-C IC, HVNMOS used as

Manuscript received March 25, 2020; revised April 25, 2020; accepted May 1, 2020. Date of publication May 18, 2020; date of current version June 19, 2020. This work was supported in part by the Ministry of Education (MOE) through the SPROUT Project—Center for Neuromodulation Medical Electronics Systems of National Chiao Tung University, Taiwan and in part by the Ministry of Science and Technology (MOST), Taiwan, under Contract MOST 108-2622-8-009-001-TE1. The review of this article was arranged by Editor C. Duvvury. *(Corresponding author: Ming-Dou Ker.)*

The authors are with the Institute of Electronics, National Chiao Tung University, Hsinchu 300, Taiwan (e-mail: mdker@ieee.org).

Color versions of one or more of the figures in this article are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TED.2020.2992383

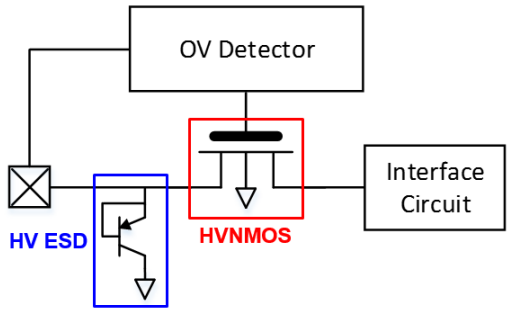

Fig. 2. Block diagram of the new proposed OVP structure for the CC pin of USB type-C interface.

a pass transistor must be placed between the bond pad and the interface circuit of the CC pin. Moreover, a HV ESD device is necessary to be added at the bond pad of the CC pin to clamp ESD and surge stresses. In spite of the fact that the HVNMOS can limit the unexpected overstress, if the HVNMOS was always in ON-state during surge events, HCD could be induced by many times surge zapping. HCD of device characteristics in HV devices has been investigated in the past [10]–[14]. It has been verified that by controlling the gate bias and decreasing the big current flowing into the switch device, it can mitigate the HCD of the transistor significantly.

A test chip fabricated in a 0.15-μm BCD technology with stand-alone HVNMOS devices and the two OVP circuits has been practically measured. First, the continuous voltage surge cycles were used to investigate the HCD of the stand-alone HVNMOS in the device level. Then, in circuit level, the proposed OVP structure was measured during surge zapping on the CC pin. Based on the experimental result, surge stress really caused HCD on the stand-alone HVNMOS. Thus, it is necessary to add the OVP structure on the CC pin of USB type-C interface to further enhance the reliability of the USB type-C IC products.

II. Surge-Induced HCD

A. Calibrated Surge Voltage Waveform and Device Structure

In order to limit the overstress voltage entering into the internal circuits of the CC pin, the HVNMOS is often used as the pass gate at the CC pin. However, surge events may cause overstress impact on the drain side of the HVNMOS. HCD on the HVNMOS will still happen during the surge events when the gate of the HVNMOS is in turn-on state.

To investigate the HCD carrier reliability with surge impacts on the HVNMOS, the device was stressed by the surge voltage waveform of many times (up to 10 000 times) with 28-V zapping voltage, where the calibrated 1.2/50-μs open-circuit surge voltage waveform with a 28-V zapping voltage can be referred to Fig. 1. The surge peak voltage was chosen to be 28 V, corresponding to the specification used in the industry [5]. Fig. 3 shows the measured waveform of the continuous surge voltage cycles used in the device-level HCD test. The overstress cycles are 5000 and 10 000 times, and the interval time of each surge voltage cycle is 1 s. The device cross-sectional view of a stand-alone HVNMOS for

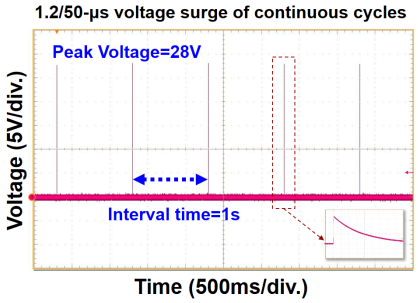

Fig. 3. Measured voltage waveform of the continuous surge cycles used in the device-level HCD test.

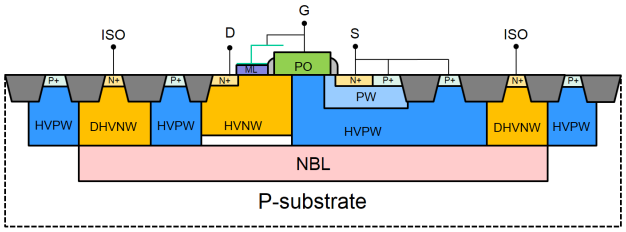

Fig. 4. Device cross-sectional view of the 30-V HVNMOS used for the device-level HCD test.

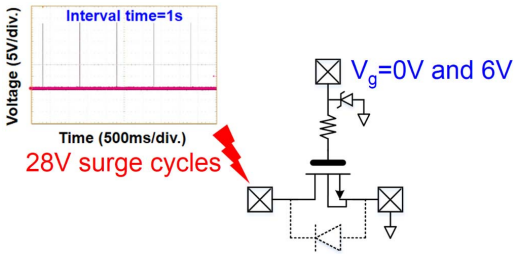

Fig. 5. Schematic of measurement set-up for the device-level HCD test by surge cycles.

the test is shown in Fig. 4, which was fabricated in a 0.15-μm BCD technology. The surge voltage patterns were applied to the drain of stand-alone HVNMOS device with its source grounded, as well as its gate was biased at 6 and 0 V under surge test, respectively, and the schematic illustrating the test set-up is shown in Fig. 5.

B. Measurement Results of the HVNMOS After the HCD Test

After the continuous surge voltage cycles test, the I–V curves and some electrical parameters of the standalone HVNMOS are remeasured and compared to seek the degradation due to surge stress.

First, the $I_d - V_d$ characteristics of the HVNMOS after the surge tests of 5000 and 10 000 times under V_g biases of 6 and 0 V were shown in Fig. 6(a) and (b), respectively. The insets in Fig. 6(a) and (b) were the zoomed-in parts on the linear region of the $I_d - V_d$ characteristics. Surge stresses really caused degradation on HVNMOS under the gate voltage (V_g) of 6 V. On the contrary, there is no obvious change after surge stresses on the HVNMOS under V_g of 0 V.

Furthermore, single point measurement was also carried out to obtain I_{dlin} (V_d of 0.1 V, V_g of 6 V) of the HVNMOS,

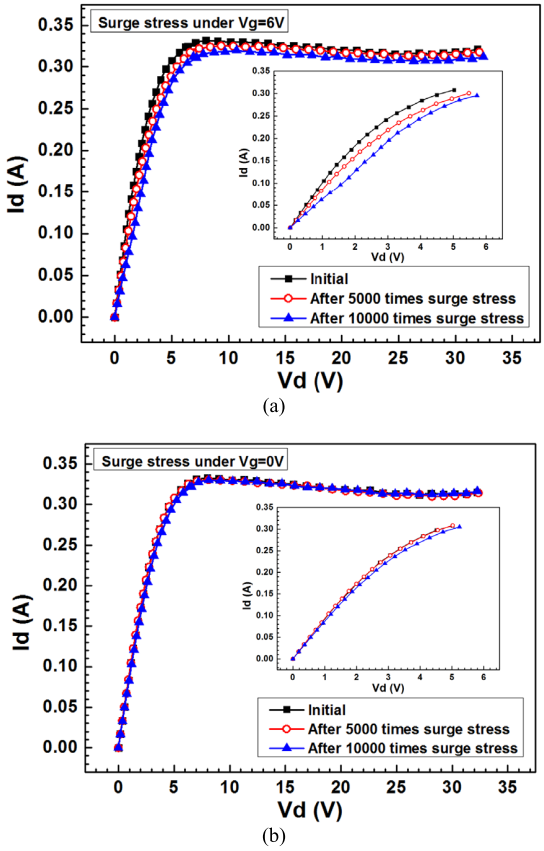

Fig. 6. Measured $I_d - V_d$ characteristics of the stand-alone HVNMOS after surge stresses of 5000 and 10 000 times under V_g of (a) 6 and (b) 0 V.

in the early linear region. In Fig. 7(a), the degradation of I_{dlin} of the HVNMOS, which was tested under V_g of 6 V after surge stressing of 5000 and 10 000 times, is more serious than that under V_g of 0 V. Surge stresses really caused I_{dlin} degradation of ~26% on the HVNMOS that stressed under V_g of 6 V. Finally, the threshold voltage (V_{th}) and maximum transconductance ($G_{m,max}$) is derived from the measured $I_d - V_g$ characteristics. The shifting percentages of V_{th} and $G_{m,max}$ on the HVNMOS after surge stresses of 5000 and 10 000 times under V_g biases of 6 and 0 V are shown in Fig. 7(b) and (c), respectively. Surge stresses really caused 1.6% increment on V_{th} of the HVNMOS that stressed under V_g of 6 V after 10 000 times stressing, and that stressed under V_g of 0 V showed no change almost. The degradation of $G_{m,max}$ on the HVNMOS that stressed under V_g of 6 V after surge stressing of 5000 and 10 000 times is more serious than that stressed under V_g of 0 V. As shown in Fig. 7(c), surge stresses caused degradation of ~9.7% on the $G_{m,max}$ of HVNMOS that stressed under V_g of 6 V after 10 000 times surge stressing.

Therefore, the on-chip OVP circuit is strongly requested to prevent HVNMOS against surge events and HCD degradation for using in the CC pin of USB type-C interface IC.

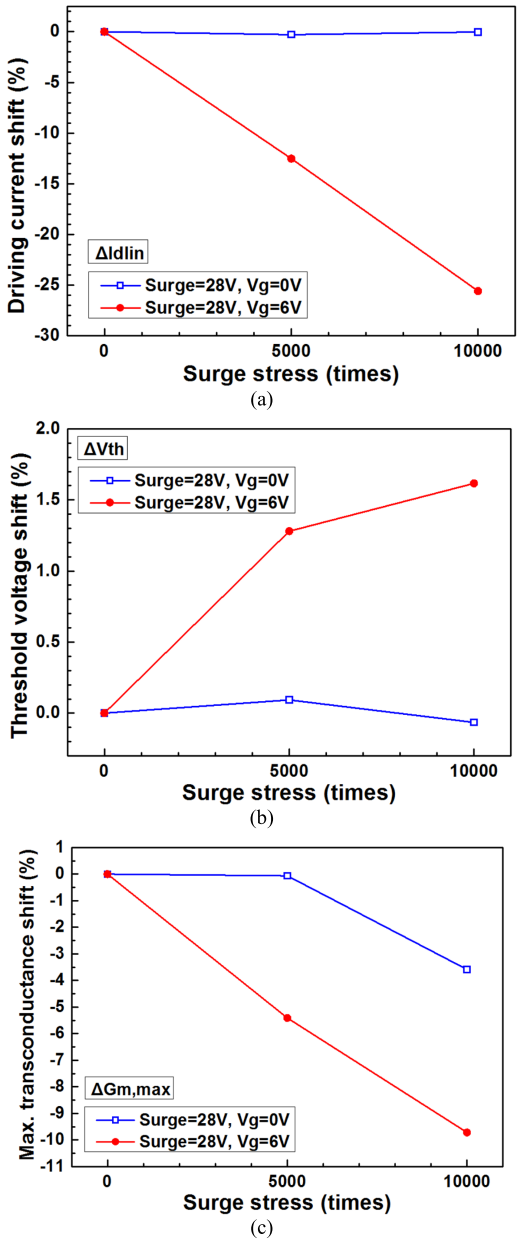

Fig. 7. Shifting percentages of (a) I_{dlin}, (b) V_{th}, and (c) $G_{m,max}$ of the HVNMOS after surge stresses of 5000 and 10 000 times under V_g of 6 and 0 V, respectively.

III. Surge OVP Circuit

A. Design Consideration

The schematic diagrams of the proposed OVP circuits were shown in Fig. 8(a) and (b). In order to limit the overstress voltage entering into the CC pin of USB type-C IC, HVNMOS must be used as a pass transistor at the CC pin and the size of the HVNMOS should be large enough to drive the output current (at least 200 mA) in the condition of V_{CONN} mode, which is a specified operation of USB Type-C interface. Furthermore, there is a function of the CC pin called dual role port, which allows the CC pin to be downstream facing port (source port) or upstream facing port (sink port) according to the system protocol.

Owing to surge currents passing through the triggering path of the detection circuit, it is essential to limit the current flowing into the Zener diode (ZD). As a result, current-limiting resistors R_1 and R_2 are added on the triggering path to avoid the ZD getting burned out immediately during surge events.

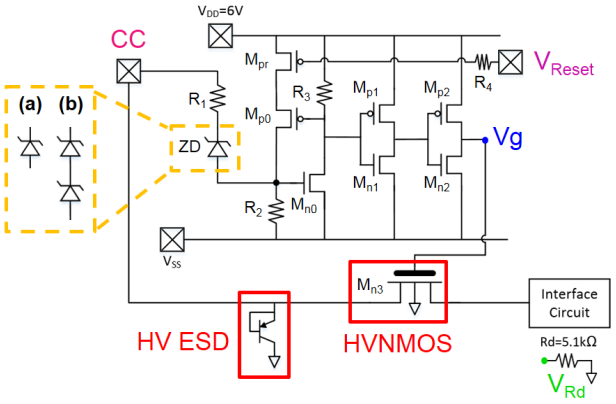

Fig. 8. Proposed OVP circuits to detect the overstress events with (a) one ZD and (b) two ZDs in stacked configuration.

TABLE I
DEVICE DIMENSIONS USED IN THE PROPOSED OVP STRUCTURES

Devices	M_{pr}	M_{p0}	M_{n0}	M_{p1}	M_{n1}	M_{p2}	M_{n2}	M_{n3}
W/L (μm/μm)	**20/0.6**	**20/0.6**	**20/0.6**	**2/0.6**	**1/0.6**	**4/0.6**	**2/0.6**	**1020/0.6**

Meanwhile, the ZD should be suitably sizing large enough to guarantee self-protection under surge stresses.

The gate voltage of HVNMOS should be pulled to 0 V during surge zapping. The ZD in the OVP circuit is used to detect the overstress voltage level zapping to the CC pin. Different over-voltage detection levels can be achieved by different stacked number of ZDs, those are called as lower voltage trigger (LVT) and higher voltage trigger (HVT) designs in this work.

When the voltage of the CC pin is in normal operating voltage (5 V), the node of V_g is set to 6 V, and the HVNMOS is in ON-state to pass the signal into the interface circuit. When the overstress voltage onto the CC pin is high enough, the circuit is triggered to pull down the node of V_g to 0 V; therefore, the HVNMOS is in OFF-state to prevent the overstress voltage and large current entering into the interface circuit. Furthermore, a positive feedback which is composed of M_{n0}, M_{p0}, R_2, and R_3 is used to enhance the turn-off time of the HVNMOS during surge events.

An on-chip HV ESD device is necessary to be added to the CC pin to clamp the overstress from ESD and surge events. The ESD device with nonsnapback characteristic is needed to avoid the latch-up-like issue during surge events, when the zapping voltage is higher than the trigger voltage (V_{t1}) of the device. As a result, the V_{t1} and holding voltage (V_h) of the HV ESD device is selected higher than the normal operating voltage (5 V), but lower than the breakdown voltage of the pass transistor (HVNMOS). In summary, the design parameters of the devices among the proposed OVP structures are listed in Tables I and II. The difference between OVP circuits with LVT and HVT designs is only the stacked number of ZDs.

B. Measurement Results of OVP Circuit With LVT Design

The proposed OVP circuits have been fabricated in a 0.15-μm BCD technology. The die photograph of the proposed

TABLE II
RESISTORS AND ESD DEVICE USED IN THE PROPOSED OVP STRUCTURES

Devices	ZD	R_1	R_2	R_3	R_4	HV ESD
Design Parameters	Width of 24μm	6 kΩ	6 kΩ	12 kΩ	1 kΩ	Width of 2000 μm

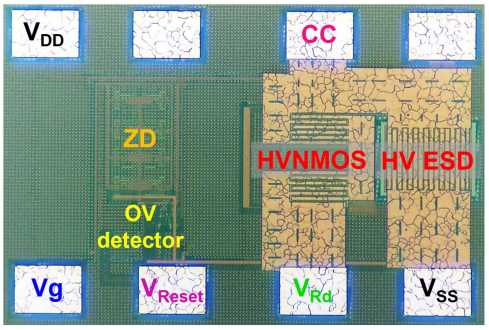

Fig. 9. Die photo of the proposed OVP circuit with LVT design.

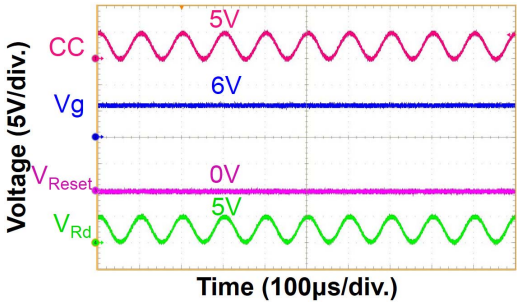

Fig. 10. Measured voltage waveforms of a 5-V sine wave passing through the HVNMOS of the OVP circuit into the CC pin referred to Fig. 7(a) with LVT design.

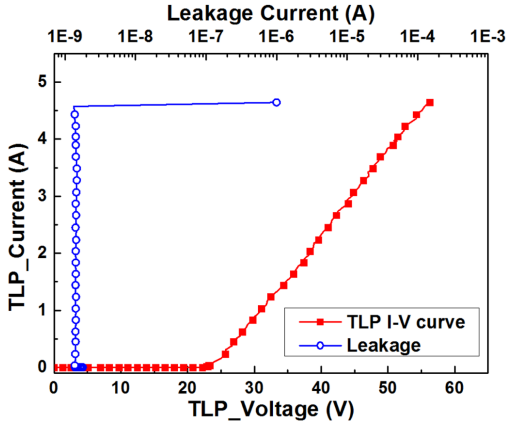

Fig. 11. Measured TLP *I–V* characteristic of the HV ESD device [p-n-p bipolar junction transistor (BJT)] added to the CC pin.

OVP circuit with LVT design is shown in Fig. 9. First of all, the normal operating voltage of CC pin in USB type-C is within 0–5 V. Fig. 10 shows the measured voltage waveforms of a 5-V sine wave successfully passing through the OVP circuit with LVT design from the CC pin to the internal load of 5.1-kΩ resistor (R_d), as referred to the circuit of Fig. 8(a).

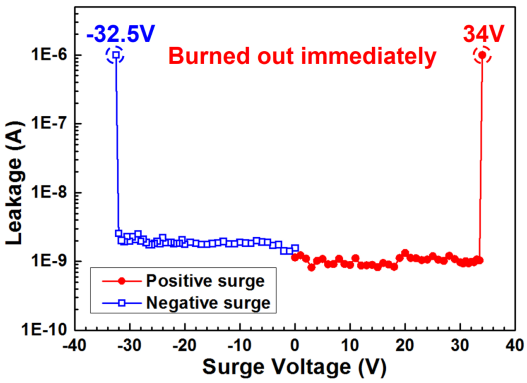

Fig. 12. Measured surge levels of the HV ESD device (p-n-p BJT) under the positive stressing or negative stressing.

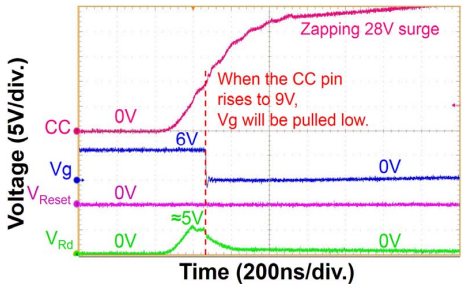

Fig. 13. Measured waveforms to verify the voltage detection level of the proposed OVP circuit with LVT design referred to Fig. 8(a).

The total width of the HV ESD device (realized by p-n-p BJT) added to the CC pin is 2000 μm (100 μm $\times$ 20 fingers). The 100-ns TLP-measured I–V characteristic of such a HV ESD device is shown in Fig. 11, with V_{t1} of 23.5 V, I_{t2} of 4.6 A, and nonsnapback characteristic. Moreover, the OVP circuit was proposed against surge events, so the surge level of this HV ESD device must be investigated. Fig. 12 shows the measured surge levels of the stand-alone HV ESD device (p-n-p BJT) under the positive stressing or negative stressing. The HV ESD device used in the OVP design can directly sustain the surge stresses of +34 and −32.5 V, respectively, that was higher than the specification of 28 V by the industry [5].

The measured waveforms during surge zapping, which verify the voltage detection level of the proposed OVP circuit with LVT design referred to Fig. 8(a) is shown in Fig. 13. When the surge voltage at the CC pin was raised over 9 V, the ZD broke down immediately to generate a voltage drop across R_2. At the same time, the voltage across R_2 will bias the gate of M_{n0} to turn M_{n0} on and the voltage at drain side of M_{n0} is pulled down to logic *low* (0 V). Then, the logic-low signal is transmitted through the buffer of two-stage inverters to the gate of the HVNMOS, thus the HVNMOS is turned off. As a result, the surge voltage at the pad is blocked from the internal circuits of the CC pin; therefore, the voltage reaching to internal load (R_d) is dropping to 0 V.

The circuit operations of the proposed OVP circuit with LVT design under different surge zapping voltages have been verified in the following experiments. Fig. 14(a)–(d) shows the measured waveforms on the circuit operations referred to

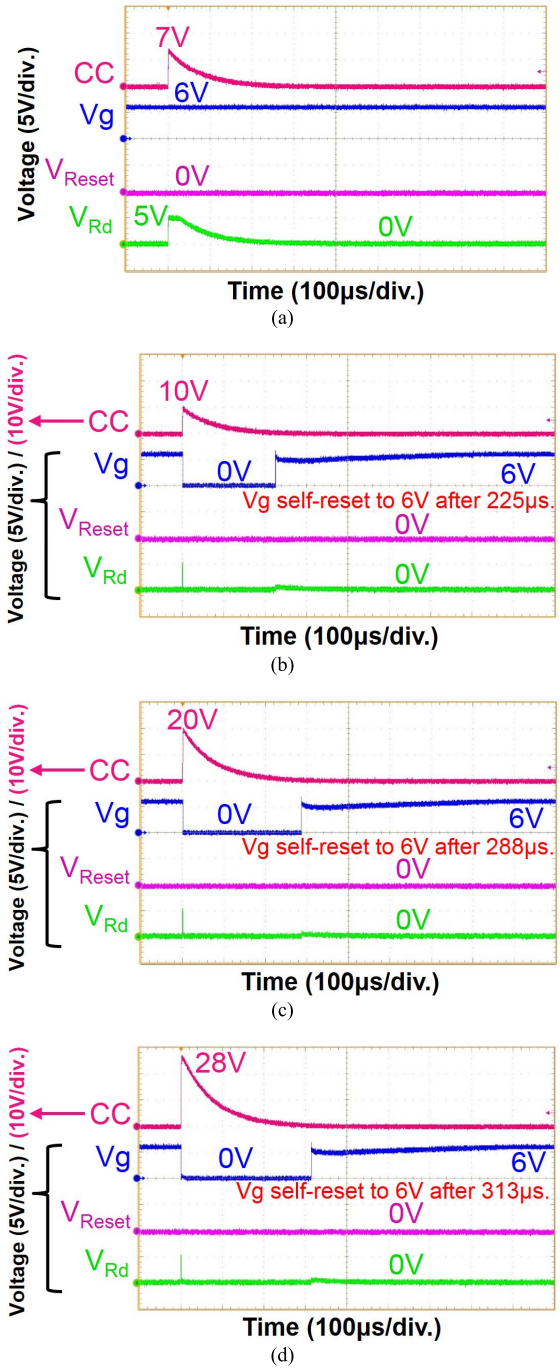

Fig. 14. Measured voltage waveforms of the proposed OVP circuit with LVT design referred to Fig. 8(a) during different surge zapping voltages of (a) 7, (b) 10, (c) 20, and (d) 28 V.

Fig. 8(a) during surge stressing at CC pin with the applied peak voltages of 7, 10, 20, and 28 V, respectively. Moreover, V_{Reset} is tied to V_{SS} during different surge zapping voltages test.

In Fig. 14(a), when the surge voltage is 7 V, lower than the detection level of 9 V, the ZD cannot break down. The voltage drop across R_2 is 0 V, and the voltage at drain side of M_{n0} is kept at 6 V. Then, the 6-V signal is transmitted through the buffer to the gate of HVNMOS, so the HVNMOS is kept in ON-state (6 V). Although the HVNMOS is in

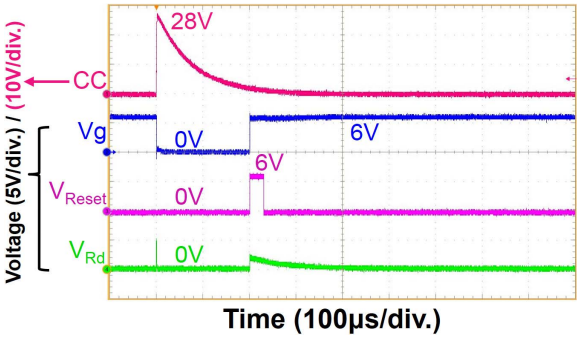

Fig. 15. Measured voltage waveforms of the OVP circuit operation when a 6-V reset signal is given after the 28-V surge zapping on the CC pin.

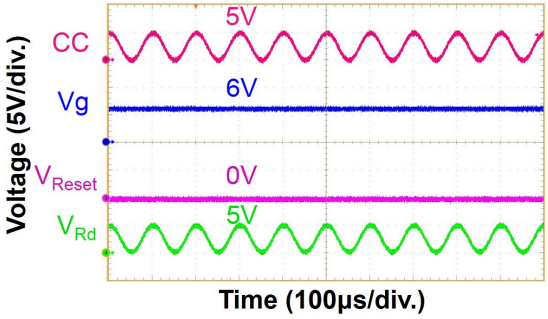

Fig. 16. Measured voltage waveforms of a 5-V sine wave passing through the HVNMOS of the OVP circuit into the CC pin referred to Fig. 8(b) with HVT design.

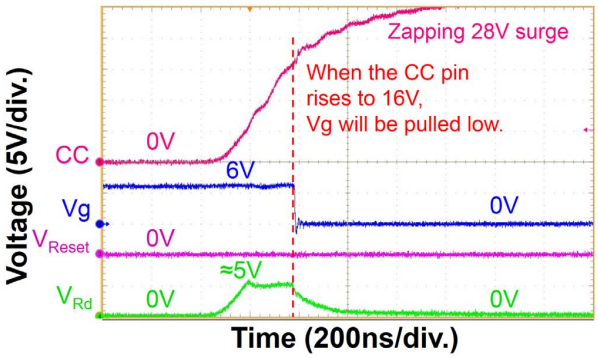

Fig. 17. Measured waveforms to verify the voltage detection level of the proposed OVP circuit with HVT design referred to Fig. 8(b).

ON-state during 7-V surge stress, the peak voltage entering into the internal load (R_d) is limited by the HVNMOS to only ~5 V, which is the nominal voltage of the CC pin in USB type-C interface. Because the V_{th} of the HVNMOS is around 1 V, in order to keep the HVNMOS in ON-state theoretically, the maximum voltage drop at the source side is equal to "$V_g - V_{th}$." Thus, the internal circuits of the CC pin can be prevented from overstress.

In Fig. 14(b), when the surge voltage is 10 V, higher than the detection level of 9 V, the ZD broke down. Meanwhile, it generates a voltage drop across R_2 to turn on M_{n0} on and the voltage at drain side of M_{n0} is pulled down to logic low (0 V). Because the drain side of M_{n0} is pulled down to logic low, there is a voltage drop across R_3 biasing the gate of M_{p0} to turn M_{p0} on. As a result, a positive feedback is generated with M_{n0} and M_{p0} both in ON-state to lock the detection result of a surge event for a long time. Finally, the logic-low signal is transmitted through buffer to the gate of the HVNMOS, and the HVNMOS is turned off for 225 μs, which is long enough during surge events because the maximum energy of surge events is always within ~50 μs. With sufficient turn-off time, the robustness against HCD can be improved efficiently. Moreover, the internal circuits of the CC pin can be prevented from being damaged by surge events, as the voltage reaching to internal load (R_d) is dropping to 0 V during the whole surge event.

As shown in Fig. 14(c) and (d) with the surge voltages of 20 and 28 V, respectively, higher than the detection level of 9 V, the ZD broke down as well to enable the detection function of the OVP circuit. Therefore, the mechanism of the circuit operation is the same as that under the surge voltage of 10 V. However, it is worth mentioning that the turn-off times of the HVNMOS are different among the zapping voltages of 10, 20, and 28 V, which are 225, 288, and 313 μs, respectively. With the higher surge zapping voltage, the longer turn-off time of the HVNMOS can be achieved, which can be ascribed to the fact that the higher zapping energy can keep the positive feedback to maintain for longer time.

Finally, the reset function of the proposed OVP circuit with LVT design has been also verified and the measured voltage waveforms are shown in Fig. 15. First, a 28-V surge voltage is applied to the CC pin and the positive feedback is generated to lock the gate voltage (V_g) of HVNMOS at 0 V. Later than the surge zapping (after 200 μs), a 6-V reset signal (V_{Reset}) is added to the gate of M_{pr} which interrupts the positive feedback. When the gate of M_{pr} is applied by 6-V reset signal, its V_{gs} becomes 0 V to turn itself off. As a consequence, the voltage at drain side of M_{n0} is repulled up to 6 V. The 6-V signal is transmitted through the buffer to the gate of HVNMOS and the HVNMOS is retuned in ON-state. Therefore, the voltage (V_{Rd}) on the internal load (R_d) was followed with the residual surge voltage on the CC pin at the same time.

C. Measurement Results of OVP Circuit With HVT Design

Two ZDs were stacked in the OVP circuit of HVT design to get a higher triggering voltage. It can make the triggering path stronger against EOS events and make the OVP circuit possess better reliability. Fig. 16 shows the measured waveforms of a 5-V sine wave successfully passing through the OVP circuit with HVT design from the CC pin to the internal load of 5.1-kΩ resistor (R_d), referred to the circuit in Fig. 8(b). The HV ESD device (p-n-p BJT) is the same as that used in the LVT design with a V_{t1} of 23.5 V.

The measured voltage waveforms to verify the voltage detection level of the proposed OVP circuit with HVT design during surge zapping is shown in Fig. 17. When the surge voltage at the CC pin was raised over 16 V, the ZD broke down immediately to generate a voltage drop across R_2. At the same time, the voltage across R_2 turn M_{n0} on and the voltage

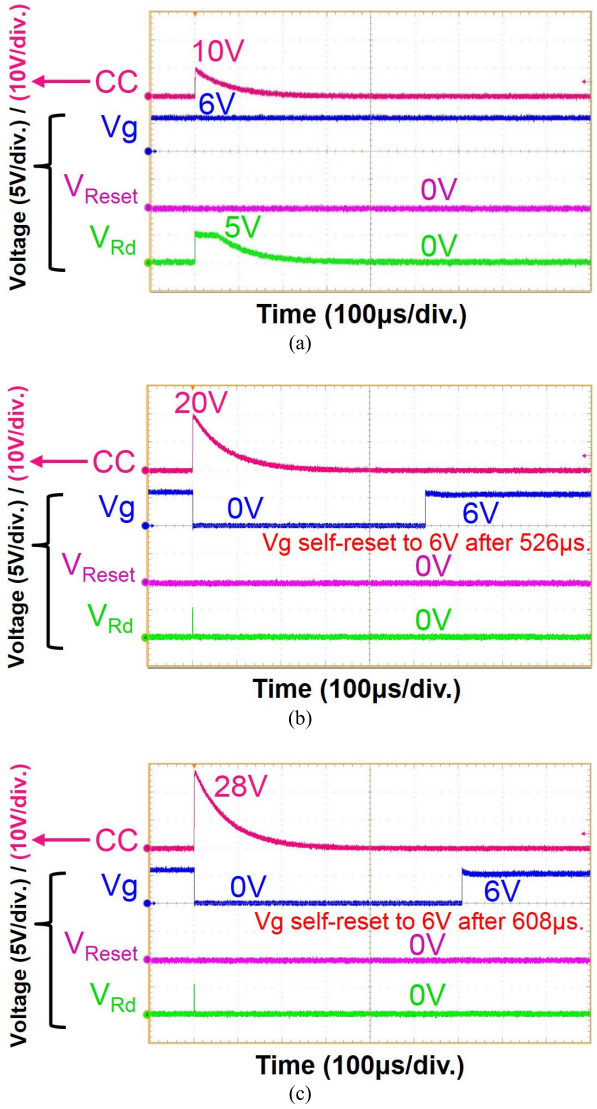

Fig. 18. Measured voltage waveforms of the proposed OVP circuit with HVT design referred to Fig. 8(b) during different surge zapping voltages of (a) 10, (b) 20, and (c) 28 V.

at drain side of M_{n0} is pulled down to logic low (0 V). Then, the logic-low signal is transmitted through the buffer to the gate of the HVNMOS; therefore, the HVNMOS is turned off. As a result, the surge voltage is blocked from the internal circuits of the CC pin, so the voltage reaching to internal load (R_d) is dropping to 0 V.

In Fig. 18(a), when the surge voltage is 10 V, lower than the detection level of 16 V, the ZD cannot break down. The voltage drop across R_2 is 0 V, and the voltage at drain side of M_{n0} is still kept in 6 V. Therefore, the HVNMOS is still kept in ON-state. Although the HVNMOS is in ON-state during 10-V surge stress, the peak voltage entering into the internal load (R_d) is limited by the HVNMOS to ~5 V which is the nominal voltage of the CC pin in USB type-C interface. Thus, the internal circuits of the CC pin can be prevented from being damaged by surge overstress.

In Fig. 18(b), when the surge voltage is 20 V, higher than the detection level of 16 V, the ZD broke down to generate a

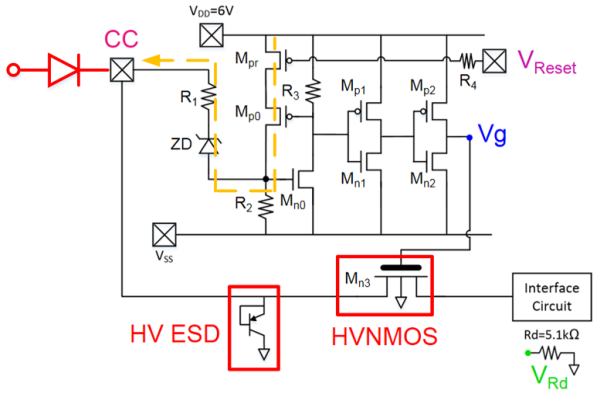

Fig. 19. Schematic of the OVP circuit for the investigation of self-reset phenomenon.

voltage drop across R_2 to turn M_{n0} on. The voltage at drain side of M_{n0} is pulled down to logic low and a voltage drop across R_3 biasing the gate of M_{p0} to turn M_{p0} on. As a result, a positive feedback is generated with M_{n0} and M_{p0} both in ON-state to lock the detection result for a long time. Therefore, the voltage at drain side of M_{n0} can be pulled down to logic low for sufficiently long time as well. Finally, the logic-low signal is transmitted to the gate of the HVNMOS and the HVNMOS is turned off for 526 μs, which is long enough during surge events, because the maximum energy of surge events is within ~50 μs. With sufficient turn-off time, the HCD robustness can be improved efficiently. Moreover, the internal circuits of the CC pin can be prevented from being damaged by surge events, and the voltage reaching to internal load (R_d) is dropping to 0 V during the whole surge event.

In Fig. 18(c), with the surge voltage of 28 V, higher than the detection level of 16 V, the ZD broke down as well. Therefore, the mechanism of the circuit operation is the same as that under the surge voltage of 20 V. However, it is worth mentioning that the turn-off times of the HVNMOS are different between surge zapping voltage of 20 and 28 V, which are 526 and 608 μs, respectively. The higher zapping voltage, the longer turn-off time of HVNMOS can be achieved, which can be ascribed to the fact that the higher zapping energy can keep the positive feedback for longer time.

The reset function of the proposed OVP circuit with HVT design has also been verified, and the measured voltage waveforms are the same as those shown in Fig. 15. The reset function is provided to early remove the lock state of detection result for system control with feasible applications. If no additional control signal applied to the reset node, its normal bias is kept at 0 V to enable the OVP circuit function and the reset function will be automatically executed by OVP circuit itself.

IV. Discussion

To investigate the self-reset mechanism in the OVP circuit, the following experiments had been done to investigate the root cause of self-reset. In Fig. 19, by adding an external diode outside the bond pad of CC pin, when the surge voltage is higher than the detection level, the gate voltage (V_g) of the

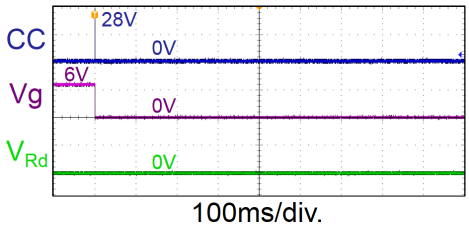

Fig. 20. Measured voltage waveforms of the proposed OVP circuit with an external diode outside the bond pad of the CC pin during 28-V voltage surge zapping.

HVNMOS can be pulled to logic low for the whole residual time, as the measured waveforms shown in Fig. 20. As a result, the self-reset phenomenon can be ascribed to the leakage path with the yellow dotted line shown in Fig. 19. When there is an extra diode adding into the triggering path (R_1, ZD, and R_2), the current in the positive feedback cannot leak through the yellow dotted line to the pad after the surge events. As a result, the positive feedback can always be kept to further keep the HVNMOS in OFF-state. Therefore, the ON-resistance along the devices on the yellow dotted line (M_{pr}, M_{p0}, ZD, and R_1) and the latch strength (formed by M_{p0}, R_3, M_{n0}, and R_2) can decide the minimum "self-reset time" of the OVP circuit.

Because the normal operating voltage of the CC pin is 5 V, it is recommended to design the minimum "self-reset time" which is the timing when the voltage of the CC pin is dropping to 5 V. Such a desired "self-reset time" can be well adjusted by additional circuit design with Simulation Program with Integrated Circuit Emphasis (SPICE) simulation on the device dimensions (M_{p0}, M_{n0}, M_{pr}, and ZD) and the resistors (R_3, R_2, and R_1) in the latch loop. For more precision operation on the rest time to restart the OVP circuit back to its original detection mode, the V_g signal of the OVP circuit can be used to trigger a digital timing circuit with the selected/desired reset time, and then the digital timing circuit sends out a signal (logic *high*) to the node of V_{Reset} to turn M_{pr} off. Therefore, the latch mode in the OVP circuit can be released earlier by the additional digital timing circuit with a precision timing control for applications.

V. Conclusion

Different from the measurement on HCD by dc stress, this work has verified that HCD issue on HVNMOS indeed happened by ac stress, such as surge events, especially when the HVNMOS was kept at ON-state. Based on the device-level HCD test results under surge stresses, the HVNMOS to prevent the internal circuits of the CC pin against surge events needs an over-voltage detector to detect surge events and then to turn the HVNMOS off when surge events happen on the CC pin. Different over-voltage detection levels of the proposed OVP circuit can be achieved by ZDs with different stacked numbers. A positive feedback in the OVP circuit is used to lock the detection result for a longer time. Moreover, a reset function is also provided to early remove the lock state of detection result for feasible control in system applications. The proposed OVP circuit has been successfully verified in a 0.15-μm BCD technology, which can be fully on-chip integrated into the USB type-C IC products to enhance the robustness against surge events.

Acknowledgment

The authors thank Jian-Hsing Lee, Shao-Chang Huang, Yeh-Ning Jou, Chih-Hsuan Lin, Li-Fan Chen, Ting-You Lin, Hsien-Feng Liao, Hwa-Chyi Chiou, Yeh-Jen Huang, and Chun-Chih Chen of the Device Engineering Division, VIS, for their valuable technical suggestions. The chip fabrication was supported by Vanguard International Semiconductor Corporation (VIS), Taiwan.

References

[1] *Universal Serial Bus 3.1 Specification*, USB Implementers Forum, Beaverton, OR, USA, 2013.
[2] *Universal Serial Bus Type-C Cable and Connector Specification*, USB Implementers Forum, Beaverton, OR, USA, 2019.
[3] *Electromagnetic Compatibility (EMC)—Part 4–5: Testing and Measurement Techniques—Surge Immunity Test*, Standard IEC 61000-4-5, 2014.
[4] X. Liu, A. Yazdi, S. Kwaaitaal, C. Speelman, and X. Zhang, "Voltage clamp circuit for surge protection," U.S. Patent 20 190 020 194 A1, Jan. 17, 2019.
[5] H. I. Oporta, S. P. Mane, T. O'Brien, and C. G. Sporck, "Over-voltage protection systems and methods," U.S. Patent 10 431 939 B2, Oct. 1, 2019.
[6] P. Mondal, A. Khamesra, and H. P. Vispute, "Overvoltage protection for universal serial bus type-C (USB-C) connector systems," U.S. Patent 10 218 129 B1, Feb. 26, 2019.
[7] N. A. Bodnaruk and D. W. Mattos, "Voltage protection for universal serial bus type-C (USB-C) connector systems," U.S. Patent 10 381 787 B1, Aug. 13, 2019.
[8] S.-E. Liu, H.-S. Huang, Y.-H. Lin, and M.-T. Lin, "Interface circuits to monitor and prevent overstress damage," U.S. Patent 20 180 102 639 A1, Apr. 12, 2018.
[9] S. E. Liu *et al.*, "Type-C interface reliability concern of electrical overstress and design for mitigation," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, Apr. 2017, pp. 3A-5.1–3A-5.4, doi: 10.1109/IRPS.2017.7936280.
[10] D. Varghese *et al.*, "Off-state degradation in drain-extended NMOS transistors: Interface damage and correlation to dielectric breakdown," *IEEE Trans. Electron Devices*, vol. 54, no. 10, pp. 2669–2678, Oct. 2007, doi: 10.1109/TED.2007.904587.
[11] D. Varghese, H. Kufluoglu, V. Reddy, H. Shichijo, S. Krishnan, and M. A. Alam, "Universality of off-state degradation in drain extended NMOS transistors," in *IEDM Tech. Dig.*, Dec. 2006, pp. 1–4, doi: 10.1109/IEDM.2006.346895.
[12] K. M. Wu *et al.*, "Effects of gate bias on hot-carrier reliability in drain extended metal-oxide-semiconductor transistors," *Appl. Phys. Lett.*, vol. 89, no. 18, Oct. 2006, Art. no. 183522, doi: 10.1063/1.2374881.
[13] J. F. Chen, K.-M. Wu, K.-W. Lin, Y.-K. Su, and S. L. Hsu, "Hot-carrier reliability in submicrometer 40V LDMOS transistors with thick gate oxide," in *Proc. Int. Rel. Phys. Symp.*, Apr. 2005, pp. 560–564, doi: 10.1109/RELPHY.2005.1493148.
[14] R. Versari and A. Pieracci, "Experimental study of hot-carrier effects in LDMOS transistors," *IEEE Trans. Electron Devices*, vol. 46, no. 6, pp. 1228–1233, Jun. 1999, doi: 10.1109/16.766890.