RF/High-Speed I/O ESD Protection: Co-optimizing Strategy Between BEOL Capacitance and HBM Immunity in Advanced CMOS Process

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***Abstract*— In order to meet the requirement of ultrahigh-speed, low latency, and wide bandwidth (BW) in the next 5G mobile network and internet of things (IoT) applications, the parasitic capacitance specification of electrostatic discharge (ESD) protection devices should become much stricter. Reducing the capacitance always degrades the ESD performance in terms of shrinking the size of the ESD protection device. The distributed ESD protection network is one of the solutions which mitigates the capacitance issue and provides a broadband design. However, while the ESD devices are put under the I/O pad in the distributed ESD protection network, back-end-of-line (BEOL) capacitance starts to play an important role in the advanced 28-nm CMOS process. Therefore, a tapered metal structure is proposed to significantly reduce 30% BEOL capacitance of the ESD device, which can gain a 2.8-GHz increase in the operational BW in the distributed network. Meanwhile, it can enhance the human-body-model (HBM) level up to 16% higher than the original layout style under the same front-end-of-line (FEOL) layout size.**

***Index Terms*— Back-end-of-line (BEOL), distributed ESD protection network, electrostatic discharge (ESD), ESD protection, high-speed I/O, parasitic capacitance, radio frequency (RF).**

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I. Introduction

With consecutive downscaling in CMOS technologies, rapid enhancement of higher operating frequency and wider bandwidth (BW) for both radio frequency (RF) and high-speed circuits is enabled. In order to meet the requirement for the next 5G mobile and internet of things (IoT) network, the overall resistance and capacitance (*RC*) components of the devices should be well optimized [1]–[3]. In particular, the *RC* components contributed by interconnects have become more critical in advanced CMOS technology [4], [5]. However, adding the electrostatic discharge (ESD) protection network is essential to provide high reliability in delicate IC products. In RF and high-speed I/O circuits, large parasitic capacitances contributed by traditional ESD devices would degrade the overall RF performance above the gigahertz (GHz) band. In addition, the human-body model (HBM) should meet the requirement of at least 1 kV, as stated in [6]. The level is scaled down with the technology node due to its inevitable limits [7], [8]. Therefore, in many articles, both ESD device and circuit solutions are introduced to mitigate the parasitic capacitance and to provide a broadband design [9]–[17].

Dual diodes with the distributed ESD protection network are still the reliable ESD protection design for many broadband RF and high-speed I/O applications, as shown in Fig. 1. However, the back-end-of-line (BEOL) design of the diodes at the first stage under the I/O pad adds extra capacitance to influence the circuit BW [17].

In this article, novel layout styles are proposed to optimize the BEOL capacitance to enhance the BW and also to keep the HBM level of the ESD robust. Diodes with a stripe layout style are deployed similar to that in [17]. The BEOL capacitance analysis, RF experiments, ESD results using the HBM tester and the transmission-line-pulsing (TLP) tester, as well as failure analysis (FA) are also demonstrated.

II. BEOL Capacitance Analysis

A. Impact of Technology Options

With dimension shrinkage in the advanced CMOS process, the coupling effect between vertical interconnects is physically increased to provide a more compact method of moments

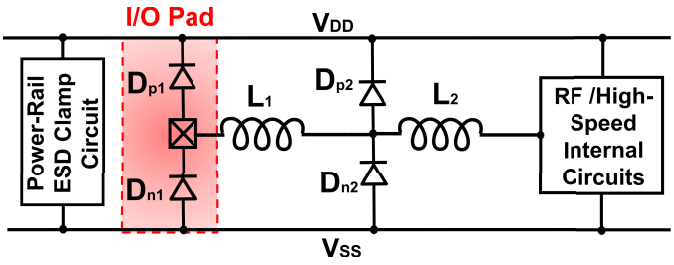

Fig. 1. Distributed network with ESD devices under the I/O pads [17].

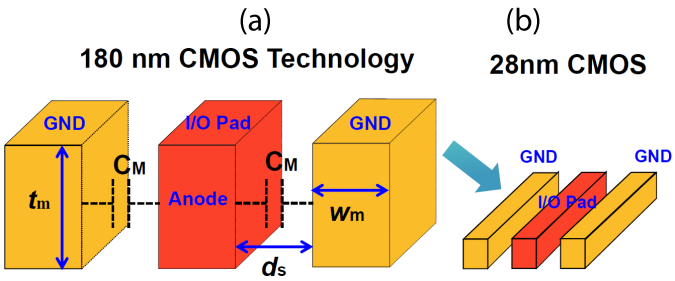

Fig. 2. 3-D view of the bottom metal layer (M_1) in (a) 180-nm CMOS and (b) 28-nm CMOS. The anode connection to the I/O pad is shown by red color, whereas the cathode connection to the device is shown by yellow color.

TABLE I
MINIMUM DESIGN RULE OF SINGLE-METAL LATER (M_1) IN TWO TECHNOLOGY NODES

	t_m (μm)	d_s (μm)	w_m (μm)	C_M (fF/μm) Calculation
180nm CMOS	0.53	0.23	0.23	0.077
28nm CMOS	0.09	0.05	0.05	0.049

(MoM) capacitor design [18]. As shown in Fig. 2, the physical distance (d_s), metal thickness (t_m), and metal width (w_m) are shrunk as the technology scales down from 180 to 28 nm. We compared the M_1 sizes of the minimum design rule in the two technology nodes, and utilized (1) to calculate the capacitance (C_M) of one single-metal layer presented in Table I. Equation (1) indicates that the dimensions of the thickness t_m and the space distance d_s influence the horizontal C_M. The C_M value of M_1 in the 28-nm process is 1.6× lower than the one in the 180-nm process. As a result, the horizontal interconnect capacitance scales down as the more decreasing size of t_m and the less decreasing size of d_s in the 28-nm technology node

$$\mathbf{C_M(fF/\mu m)} = \frac{\boldsymbol{\varepsilon_0} \times \boldsymbol{\varepsilon_d} \times \mathbf{t_m}}{\mathbf{d_s}}. \quad (1)$$

However, even though C_M in each metal layer is reduced in the 28-nm process, the overall BEOL capacitance occupies an evident ratio in the whole ESD protection device. In the following experiments, the ESD protection diodes with the junction of P+/NW (PNW) under the I/O pads are measured using the de-embedding method [2], [20]. The diodes are designed at the same HBM level, respectively, in the 180- and 28-nm processes. The measured results in Fig. 3 show the BEOL capacitance deviation between the two technology nodes and the BEOL capacitance ratio in each technology node. The total capacitance in the 28-nm process is reduced compared to the one in the 180-nm process, but the overall BEOL capacitance significantly occupies 52.8% in the 28-nm CMOS, while it only occupies 28.5% of the total capacitance in the 180-nm process. The difference comes from the extra vertical coupling (C_{mp}) between the I/O pad and cathode metals, as shown in Fig. 4(a). Since the height of each dielectric layer is reduced in the 28-nm process, C_{mp} inevitably contributes more capacitance under the same structure. Therefore, the BEOL obviously starts to dominate the total capacitance in the 28-nm process.

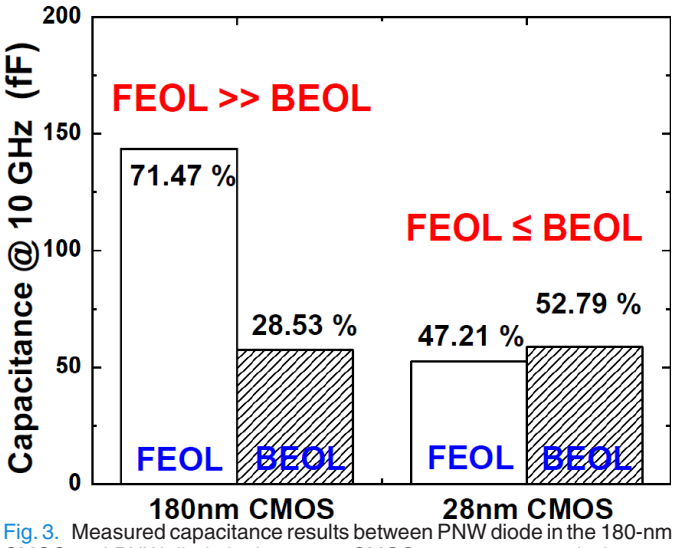

Fig. 3. Measured capacitance results between PNW diode in the 180-nm CMOS and PNW diode in the 28-nm CMOS process, respectively.

B. Model of ESD Protection Diode Under I/O Pad

Considering the ESD protection diodes under the I/O pads, the BEOL capacitance of the structure becomes critical in the 28-nm CMOS technology. Therefore, modeling the physical structures of the network is essential to be built up to investigate the contributions. Fig. 4(a) shows the N-finger cross-sectional view of the BEOL physical structure between the I/O pad (anode) and the ground (cathode) of the P+/NW diode, whereas the N-finger front-end-of-line (FEOL) cross-sectional view in Fig. 4(b) corresponds to the connection in Fig. 4(a). The name of each finger is called F_N. Each F_N is made up of one anode and two cathode fingers, which offers a symmetrical path for the uniform ESD current in each F_N. Fig. 5 shows the diagram to summarize both the parasitic components on the structures in Fig. 4(a) and (b).

For the FEOL parasitic capacitance, the junction between P+ and N-well (NW) is the main capacitance contribution seen by the RF signal path in the real circuit connection. R_{NW} is the series resistance with junction capacitance in the NW. On the other hand, for the BEOL parameters, the interconnects can be modeled as the series of inductor (L_{M0}) and resistor (R_{M0}). It consists of a series RL ladder network due to the skin effect in addition to L_{M0} and R_{M0}.

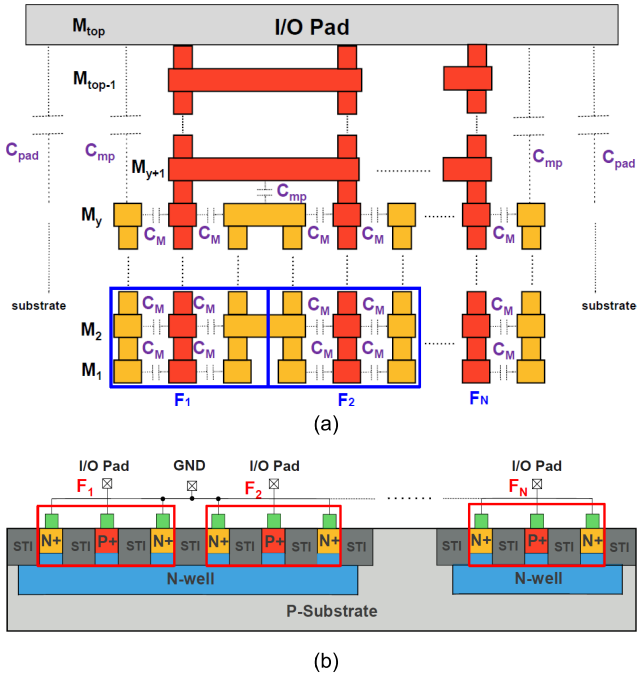

Fig. 4. (a) N-finger cross-sectional view of BEOL. BEOL capacitance is made of C_{pad}, C_{mp}, and C_M. (b) N-finger cross-sectional view of the PNW diode corresponding (a). Like Fig. 2, the anode connection is shown by red color, whereas the cathode connection is shown by yellow color.

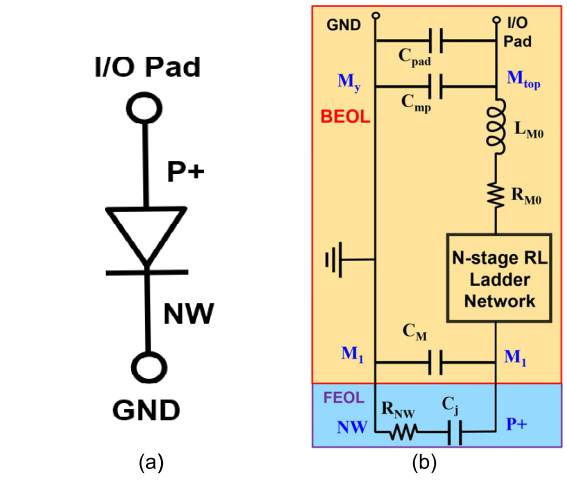

Fig. 5. (a) I/O pad and ground pins on the P+/NW diode. (b) All the parasitic components between I/O pad (anode) and ground (cathode) of the structure. Assume all the substrate parasitics are connected to the ground. Both (a) and (b) can be used to analyze N-finger diode.

The stage of the *RL* ladder depends on the operating frequency range [19]. The definition of C_M, C_{mp}, and C_{pad} is shown in Fig. 4(a). Basically, the C_M describes the horizontal metal coupling between the anode and the cathode, and the C_{mp} and the C_{pad} exist vertically between the I/O pad (M_{top}), the cathode (M_y), and the substrate coupling, respectively. These three capacitances are recognized as one BEOL capacitance. The value of C_{mp} depends on the number of y. The higher the y layer, the more C_{mp} is introduced in the structure. In the following experiments, we design y to be 6 to enlarge the effective metal width at the cathodes to carry enough ESD current.

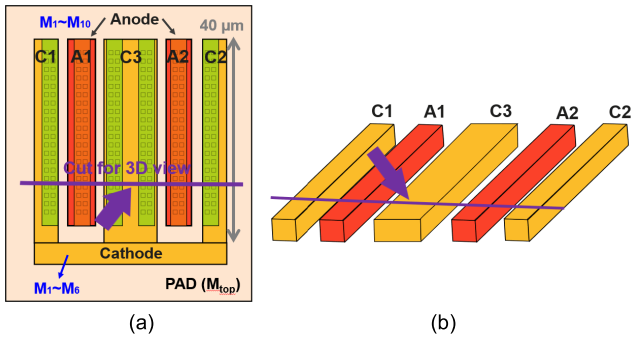

Fig. 6. Structure A. Two-finger full metal with the finger width of 40 μm (a) top view of structure A and (b) 3-D view of bottom metal layer (M_1). Like Figs. 2 and 4, the anode connection is shown by red color, whereas the cathode connection is shown by yellow color.

TABLE II
PARAMETERS OF CUTTING AND SHIFTING METALS

	Structure B (Fig. 7)	Structure C (Fig. 8)
l_a (μm)	4.8	4.8
l_c (μm)	4.8	6
w_{ma} (μm)	0.5	0.5
w_{mc1} (μm)	1	1
w_{mc2} (μm)	2	2
t_m (μm)	0.09	0.09
x (μm)	4	4
d_s (μm)	0.5	0.5

III. Discrete BEOL for Capacitance Reduction

A. Proposed Discrete Metals

Since the result from Fig. 3 reveals the importance of the BEOL capacitance of ESD devices in the advanced 28-nm CMOS process, the BEOL optimization should be proposed to feasibly decrease the ratio. The two-finger PNW diodes are used and the full stripe metal style is shown as the top view in Fig. 6(a) and the 3-D view in Fig. 6(b). It is labeled as structure A. From the hints of (1), C_M can be physically reduced by shrinking the overlapping area between the anode and the cathode horizontally. Intuitively, we cut the metals to decrease the overlapping area in order to keep the same layout area, which is labeled as structure B in Fig. 7. Furthermore, if more capacitance reduction is required, then the metals are cut and shifted to reduce the overlapping area, which is labeled as structure C in Fig. 8. The values of the experimental parameters in structures B and C are listed in Table II. The discrete metals are cut/shifted from M_1 to M_4 at the fingers of the anode and the cathode in structures B and C, while the rest of the used metals are connected as full metals.

B. RF Measurement for Capacitance Extraction

The capacitance is extracted by a two-port *S*-parameter from the RF measurement results using the deembedding method [2], [20]. By using the KS-N5247B PNA-x instrument

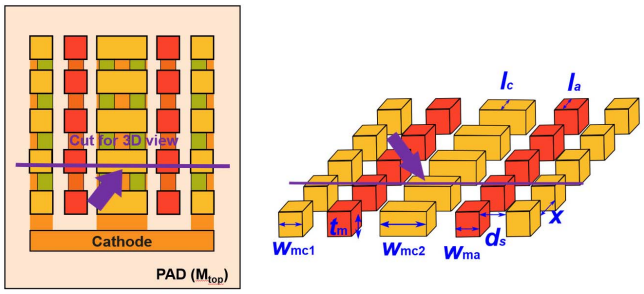

Fig. 7. Structure B. Two-finger structure of cutting M_1–M_4 with x of 4 μm (a) top view of the structure B and (b) 3-D view of M_1. Like Figs. 2, 4, and 6, the anode connection is shown by red color, whereas the cathode connection is shown by yellow color.

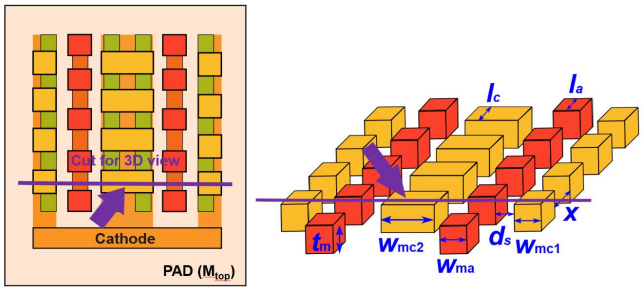

Fig. 8. Structure C. Two-finger structure of cutting and shifting M_1–M_4 with x of 4 μm (a) top view of the structure C and (b) 3-D view of M_1. Like Figs. 2, 4, 6, and 7, the anode connection is shown by red color, whereas the cathode connection is shown by yellow color.

with a frequency range up to 67 GHz, we can measure the S-parameter and convert it into the Y-parameter with a frequency-dependent value which calculates the capacitance by an advanced design system (ADS) software authorized by Keysight. The BEOL capacitance result with a frequency response until 30 GHz is shown in Fig. 9. The result indicates that structure C improves the lower capacitance by 18% at 28 GHz than structure A in terms of the overall BEOL capacitance under I/O pad. This proves that reducing the overlapping area helps to decrease the capacitance under the same layout size of the device.

C. ESD Measurement Results

We use the HED-W5000M HBM tester to evaluate the HBM failure voltage level on the devices. The power supply of Keithley 2410 is used to bias the diodes after each stress so that the failure point can be observed. As shown in Fig. 10, the failure voltage level degrades dramatically as the full metals are cut and shifted. Furthermore, the TLP tester from HED-T5000 is utilized to measure the TLP I–V curve to provide extra information about the failure mechanism [21]. The source of the TLP testing is a 100-ns pulsewidth and 2-ns rise time correlating with the real HBM waveform.

As shown in Fig. 11, the TLP measurement results of all the three structures are demonstrated. The evident I_{t2} degradation is observed from the figure, which matches the result in the HBM test. The I_{t2} degrades from 3.16 to 1.9 A (40%) in

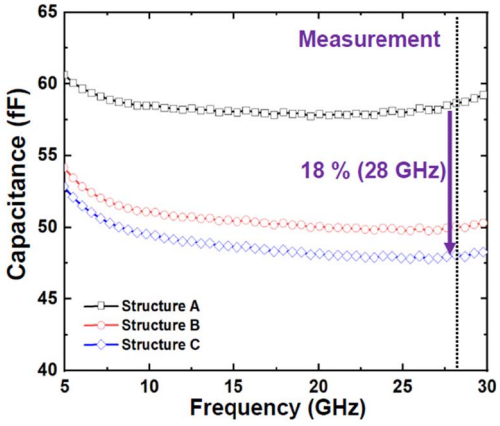

Fig. 9. RF measurement results of all the tests with a two-finger structure of 40-μm finger width. Structure C improves the lower capacitance by 18% than the structure A at 28 GHz.

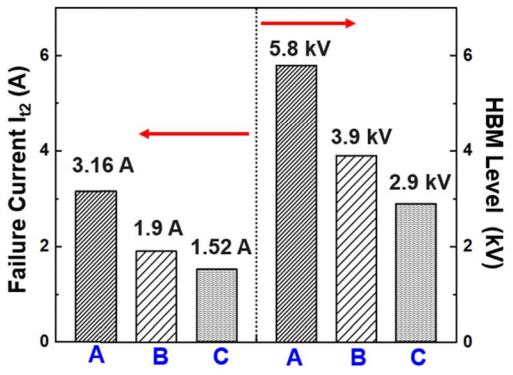

Fig. 10. HBM failure voltage level on the right side. Structure C degrades the voltage level by 50% lower than structure A. The failure current from TLP tester correlates with HBM results on the left side and the TLP I–V curve is shown in Fig. 11.

structure B, while the I_{t2} in structure C degrades from 3.16 to 1.52 A (52%), which is the worst case among the structures.

FA is made to observe the failure spots and explain the failure mechanism. All the metals on top of the contacts are delayered and chemically cleaned. As shown in Fig. 12, for the optical microscopy (OM) photographs, primary information is the nonuniform current path which occurs in structures B and C. Due to the discrete metals, the current path is crowded at region I to cause higher current density, which thermally leads to having a contact spike or burnout in the junction there.

As can be seen from Fig. 11, the leakage current gradually becomes larger in structure A and the TLP I–V characteristic is kept as the same resistive slope, which indicates that the current path through the metals and contacts is still intact. According to the OM result, region I of structure A has a deeper burnout footprint than regions II and III due to the asymmetrical connection of the cathodes. As a result, the contacts in region I are prone to make impurity doped into the silicon P+/NW junction, which causes the gradual increase in the leakage current. When I_{t2} occurs in structure A, the metals and the contacts are still not damaged to change resistance, but after the junction is uniformly and permanently broken,

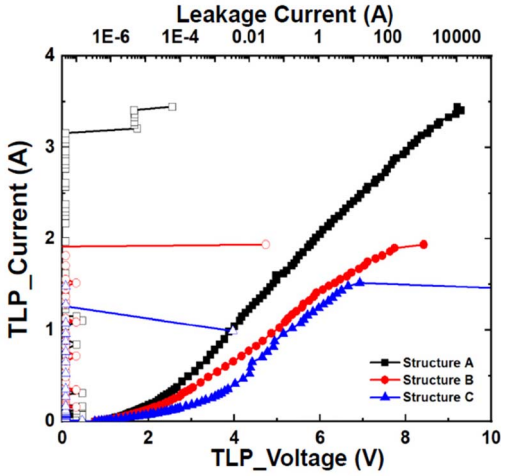

Fig. 11. TLP results of all the two-finger test structures with the finger width of 40 μm. The I_{t2} corresponds proportionally to the HBM results in Fig. 10.

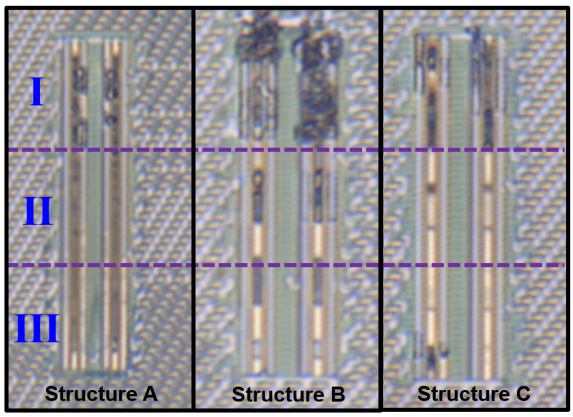

Fig. 12. OM photographs of the three test structures for FA. The left to the right structures A–C in the order. Each structure separates three parts of the failure spots to be further investigated by SEM in Fig. 13.

it makes the TLP current slightly snapback to the electrical short characteristic with large dc leakage current. On the other hand, the nonuniform current path totally enlarges the turn-ON resistance and causes earlier failure current in structures B and C. The I_{t2} occurs with the electrical open characteristic of TLP current, increasing the dc leakage current.

Fig. 13 shows the scanning electron microscopy (SEM) photographs to indicate the detailed burnout situation of three regions I, II, and III in Fig. 12. The failure spots evenly distributed in three regions of structure A are obviously observed in Fig. 13(a), (d), and (g), respectively, whereas it has no evident burnout spots both in structures B and C in Fig. 13(e), (h), and (f), respectively. The SEM results totally support the above-mentioned analysis.

IV. Optimized Design for ESD and RF Performance

A. Proposed Tapered Metal Layout

Although the discrete metals can reduce capacitance, the HBM level, instead, degrades significantly due to the totally nonuniform current path causing the unbalanced thermal

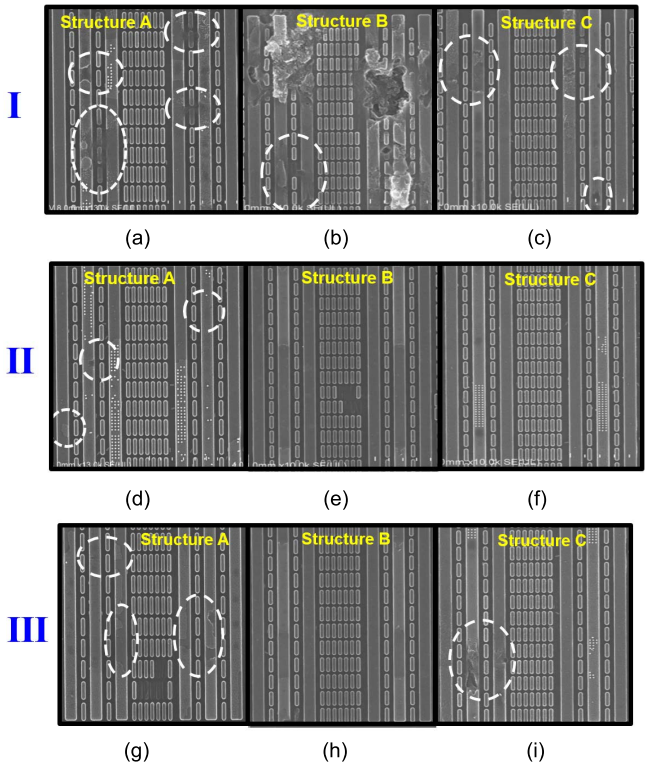

Fig. 13. SEM photographs. (a), (d), and (g) Structure A of regions I, II, and III in Fig. 12, respectively. (b), (e), and (h) Structure B of regions I, II, and III in Fig. 12, respectively. (c), (f), and (i) Structure C of regions I, II, and III in Fig. 12, respectively.

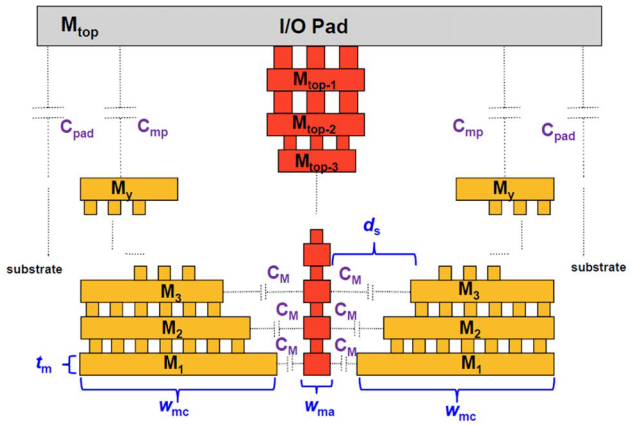

Fig. 14. Cross-sectional view of the tapered structure D with full metals for each metal layer. M_1 is fixed with the minimum spacing between the anodes and cathodes. From M_2 to M_y, it moves the cathodes away from the anodes increasing the coupling spacing d_s. Like Figs. 2, 4, 6–8, the anode connection is shown by red color, whereas the cathode connection is shown by yellow color.

distribution. Therefore, keeping the metals as the full style of structure A is a well-experienced statement from a prior study. We propose structure D to move the cathode away from the anode in order to increase the distance so that the capacitance can be reduced with the full metals.

The concept of the tapered layout is shown in Fig. 14. In our experiments, the tapered structure makes the cathodes shift 2× the distance away from the anodes for each layer from M_2 until M_4. M_5 and M_6 maintain the same distance as M_4 in consideration of the capacity of the ESD current.

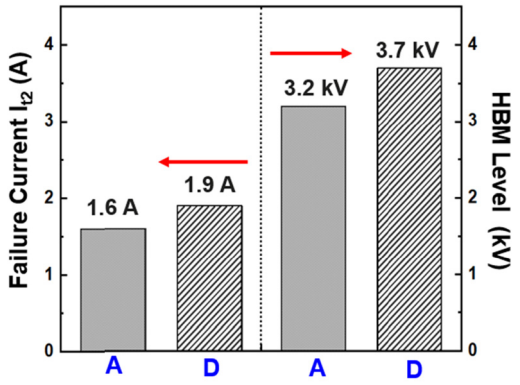

Fig. 15. HBM failure voltage level on the right side. Structure D improves 500-V higher level than the structure A. The failure current from TLP tester correlates with the HBM results on the left side and the TLP *I–V* curve is shown in Fig. 16.

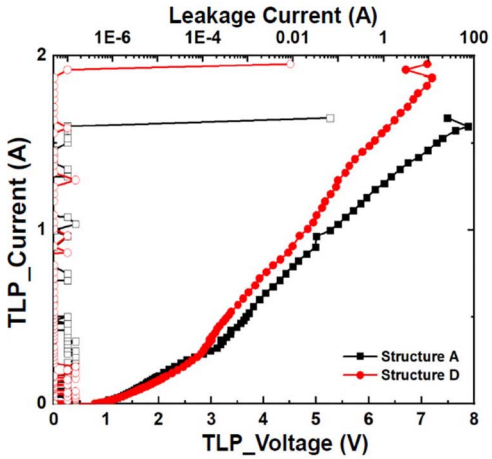

Fig. 16. TLP results of all the one-finger test structures with the finger width of 40 μm. The I_{t2} corresponds proportionally to the HBM results in Fig. 15.

The parameters are listed in Table III. The same measurements in terms of RF and ESD evaluation which we used for the discrete metals are repeated in the following parts.

B. ESD Measurement Results

For the HBM tests, the same HED-W5000M HBM tester is utilized. Note that the diode size here for structures A and D is the one-finger structure with a finger width of 40 μm. As shown in Fig. 15, structure D can enhance 500 V higher than the HBM level than structure A. In other words, under the same finger size, structure D can offer extra HBM immunity. On the other hand, the same TLP tester with 100-ns pulsewidth and 2-ns rising time is utilized to investigate the device behavior. As shown in Fig. 16, the TLP result between structures A and D is compared. The I_{t2} of structure A is almost the half order of the 2-finger device previously so that the result is consistent with the finger size. Moreover, structure D is enhanced 19% higher from 1.6 to 1.9 A because the metal width of bottom metal (M_1) is 3× wider than structure A to form the reliable tapered metal connection. Therefore, R_{ON} is also improved from 3.51 to 2.53 Ω.

Based on the analysis in discrete metals, we can also apply the scenarios in Fig. 16. Electrical short (i.e., lower impedance) in the TLP $I–V$ curve is observed after I_{t2} occurs in structure D, which indicates that the junction failure is not highly related to the contacts spike or burnout. Moreover, the layout of the tapered metals improves more uniform thermal distribution. As a result, the tapered structure has better ESD performance than the original full metal and significantly than the discrete metals.

TABLE III
BEOL PARAMETERS OF FULL AND TAPERED METALS

	Structure A (Fig. 6)	Structure D (Fig.14)
$M_{1\sim6}$ t_m (μm)	0.09	0.09
M_1 w_{ma} (μm)	0.5	0.5
M_1 w_{mc} (μm)	1	3
M_2 w_{mc} (μm)	1	2.5
M_3 w_{mc} (μm)	1	2
$M_{4\sim6}$ w_{mc} (μm)	1	1.5
M_1 d_s (μm)	0.5	0.5
M_2 d_s (μm)	0.5	1
M_3 d_s (μm)	0.5	1.5
$M_{4\sim6}$ d_s (μm)	0.5	2

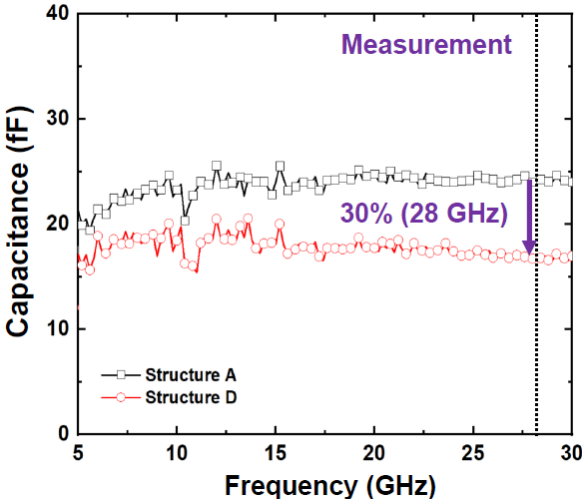

Fig. 17. RF measurement results. Structure D of the tapered layout has a less capacitance of 30% than the original structure A at 28 GHz.

C. Capacitance and RF BW Improvement

The capacitance result with frequency response until 30 GHz is shown in Fig. 17. The result indicates structure D improves 30% lower capacitance at 28 GHz than structure A in terms of the horizontal capacitance of C_M. It proves that increasing the distance d_s in (1) helps to decrease the capacitance under the same FEOL area. The BEOL layout area, nonetheless, is increased with the larger d_s and wider metal width of M_1. Fortunately, the whole devices are integrated with I/O pad so that the increment of the device area does not render the layout penalty on the ESD protection circuit.

Since we have already studied structure D has lower capacitance and higher HBM level in the device perspective, we want

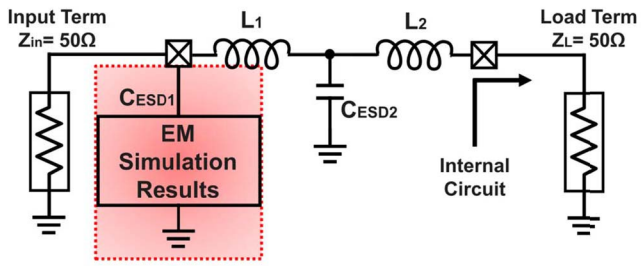

Fig. 18. Distributed network with the proposed low-C pad methods. The electromagnetic (EM) simulation results are put in the network to observe the BW of the network.

TABLE IV
DESIGNED PARAMETERS OF DISTRIBUTED NETWORK

	Proposed devices	
L_1 (pH)	200	
L_2 (pH)	80	
	Structure A	Structure D
C_{ESD1} (fF)	121	111
C_{ESD2} (fF)	112	102

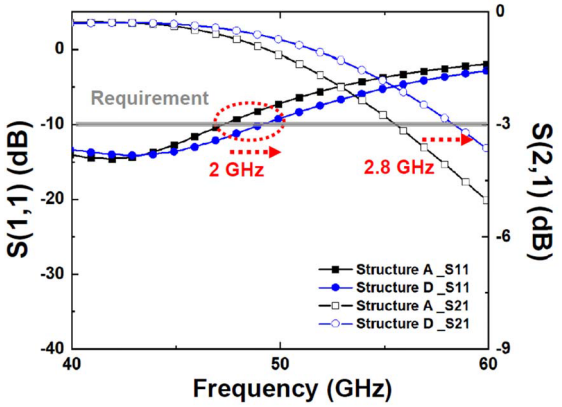

Fig. 19. Simulation results of return loss (S_{11}) for 50-Ω system matching of internal circuits and insertion loss (S_{21}) for signal loss from the I/O pad to signal input of internal circuits. S_{11} of the proposed structure D improves 2-GHz wider than the structure A. S_{21} of the proposed structure D improves 2.8-GHz wider than the structure A.

to verify the BW improvement of the distributed network in Fig. 1. The simulation setup is depicted in Fig. 18. The values of the lumped components listed in Table IV are designed to match the 50 Ω impedance of the internal circuit. The results are simulated by using ADS software as shown in Fig. 19. Simulated S_{11}, representing the return loss of the distributed network, is 2-GHz wider in one-finger devices, while the simulated S_{21}, representing the insertion loss, is 2.8-GHz wider. The requirements are set below -10 dB in S_{11} and above -3 dB in S_{21}, respectively. It is evident that structure D provides effective BW improvement and potentially makes the internal RF/high-speed circuit design more flexible.

The overall performance of the proposed device in this article can be evaluated from the figure of merit (FOM) in terms of capacitance (C_M), network BW, and current level failure (I_{t2}) and is expressed as

$$\mathbf{FOM} = \frac{\mathbf{I_{t2}} \times \mathbf{BW_{S11}} \times \mathbf{BW_{S21}}}{\mathbf{C_M}}. \quad (2)$$

TABLE V
COMPARISON TABLE OF ONE-FINGER STRUCTURES

		Structure A	Structure D
RF	#C_M (fF)	24	16.7
	#C_j (fF)	28.3	28.3
	@S_{11} (GHz)	47.1	49.1
	@S_{21} (GHz)	55.5	58.3
ESD	V_{t1} (V)	0.99	1
	R_{on} (Ω)	3.51	2.53
	I_{t2} (A)	1.6	1.9
	HBM (kV)	3.2	3.7
Layout Area	*A (μm^2)	136.6	292.8
FOM	(A*GHz/ fF)	174.27	325.68

capacitance is measured and extracted at 28-GHz. @ simulation data.
* consider 0.9x shrinkage in 28 nm process.

We discard the layout area in (2) in consideration of the same area of the I/O pad. Moreover, the capacitance of C_M is only considered in (2) due to the same junction capacitance. The FOM is utilized to show the overall BEOL enhancement under the same finger size. The numerical results are summarized in Table V with a comparison table in summary. FOM of structure D shows around 2× better than structure A.

V. CONCLUSION

The choice of technology influences the capacitance value due to the different physical 3-D sizes in each process. With the ESD devices integrated under the I/O pad in the distributed network, the BEOL capacitance in the advanced 28-nm CMOS technology starts to dominate the overall capacitance. The physical cross-sectional view and the model of the ESD protection diode offer a clear scope of capacitance contributions.

In order to retain the same layout area, discrete metals are proposed to decrease the capacitance but the HBM level was dramatically sacrificed. The FA revealed that the nonuniform current distribution leads to a higher turn-ON resistance and worse thermal effect so that the failure level degrades completely.

However, the proposed tapered metals enhanced the HBM level and provided less capacitance by increasing the space between the anode and the cathode. Furthermore, the BW of the distributed network can be upgraded to 2.8-GHz wider under the same FEOL layout size.

In conclusion, the tapered metal layout gains advantages of both lower capacitance and higher HBM immunity, and the technique is applicable to the ESD protection devices for RF and high-speed I/O design.

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