Energy Transformation Between the Inductor and the Power Transistor for the Unclamped Inductive Switching (UIS) Test

Karuna Nidhi, Jian-Hsing Lee, Shao-Chang Huang, and Ming-Dou Ker, *Fellow, IEEE*

***Abstract*—The fundamental model of energy transformation between the inductor and the power transistor for the unclamped inductive switching (UIS) test is inspected. Based on the experimental results, the energy stored in the inductor at the period of the channel turn-on can be dissipated by the power transistor after the channel is turned off. In this work, a new theoretical model to well describe the electrical and thermal behaviors of the power transistor during the unclamped inductive switching (UIS) test has been identified and analyzed with the experimental silicon results under different inductor values in 0.15 μm BCD process. The total UIS energy reduced due to series resistance of the inductor and the power transistor has been theoretically explained and well matches with the experimental measured results on silicon.**

***Index Terms*—Unclamped inductive switching (UIS), avalanche breakdown, power transistor, inductor, series resistance, second breakdown.**

I. Introduction

THE UNCLAMPED inductive switching (UIS) test is widely accepted and implemented in the power metal-oxide- semiconductor field-effect-transistor (MOSFET) family. It is very crucial for the power device reliability since it happen during uncertain and abnormal conditions. It has been a methodology to qualify the ruggedness and the robustness of the power transistors, as shown in Fig. 1 [1]–[8]. The methodology is based on the channel of the power transistor turns on to provide a low impedance current path to ramp up the current I_D of the inductor L, as the voltage V_G is applied to the gate. Then, the V_G and V_{DD} drop down to 0V to turn off the channel (T_2 in Fig. 1). Since the current of an inductor cannot be changed instantaneously, the power transistor is forced to bias at the avalanche breakdown region to keep the current flowing. This causes power transistor to operate at the high voltage and current I_D to fall with time. After the channel turns off, all energy stored in the inductor at the period of the channel turn-on (T_1 in Fig. 1) is transmitted into and dissipated by the power transistor. This is the conventional model to describe the energy transformation between the inductor and the power transistor for the UIS test [7]–[13]. The typically measured maximum current and voltage (just before failure) waveforms of large array device (LAD) 5-V NMOSFET for the UIS tests of W = 6000μm and W = 12000μm under L = 0.5 mH are shown in Fig. 2(a) and (b), respectively. If this conventional model was true, then the time in avalanche (T_2) should be longer than 37 μs and 66.4 μs in Figs. 2(a) and (b), respectively. Table I shows the calculation of T_2 based on the conventional UIS model ($T_2 = LI_o/V_o$) for the condition W = 6000μm and W = 12000μm under L = 0.5 mH. This deviation arises from the series resistances of the inductor and the power transistor. These series circuit resistances reduce the device avalanche stress. The lack of accuracy in the calculation of the UIS energy handling capability of the power FETs create misconception of design goal. Hence it leads to many unnecessary iterations to achieve the desired results and confirms the unpredicted anomalous behavior of the test device. It is important to note that the real applications involving the UIS must contain the series resistance from the used inductor and any other series elements. Hence in this paper, a new theoretical model and the previous equations used to model the UIS calculation is compared along with measured curves to overcome the inaccuracy in the UIS energy calculation.

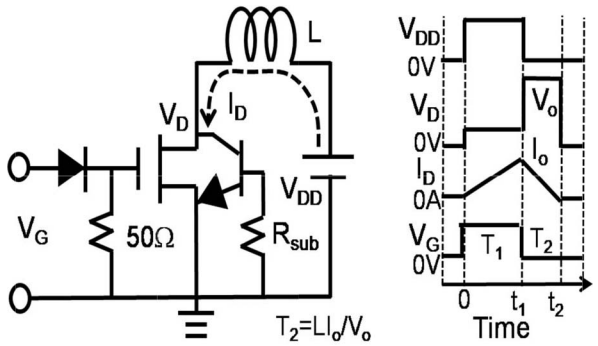

Fig. 1. Schematic diagram for UIS test and associated waveforms.

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Karuna Nidhi is with the Device Engineering Division, Vanguard International Semiconductor Corporation, Hsinchu 30010, Taiwan, and also with the International Graduate Program, College of Electrical Engineering and Computer Science, National Chiao Tung University, Hsinchu 30010, Taiwan (e-mail: karuna.munna@gmail.com).

Jian-Hsing Lee and Shao-Chang Huang are with the Device Engineering Division, Vanguard International Semiconductor Corporation, Hsinchu 30010, Taiwan (e-mail: ano.lee2009@gmail.com; ajakes2010@yahoo.com.tw).

Ming-Dou Ker is with the Institute of Electronics, National Chiao Tung University, Hsinchu 30010, Taiwan, and also with the Department of Electronics, I-Shou University, Kaohsiung 840, Taiwan (e-mail: mdker@ieee.org).

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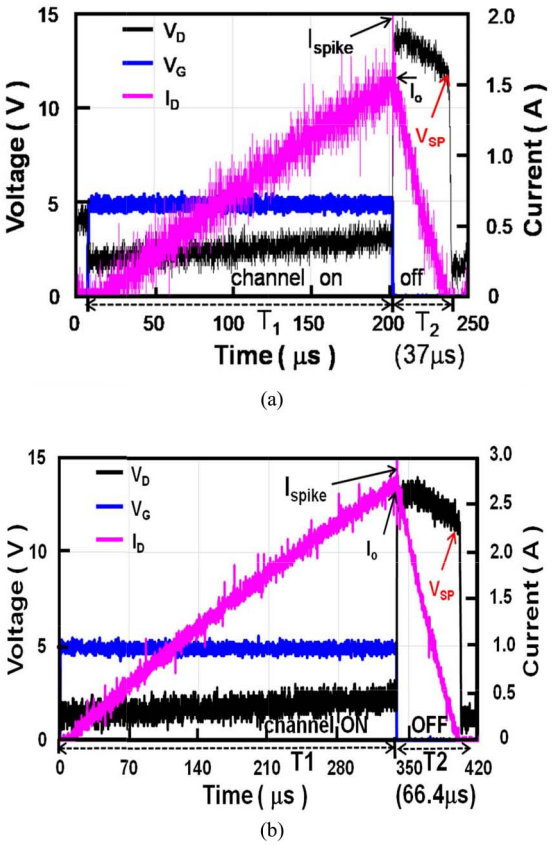


Fig. 2. The maximum measured current and voltage waveforms just before failure for the UIS test (a) W=6000μm and (b) W = 12000μm under L = 0.5mH.

II. UIS Energy Overview

The unclamped inductive switching has demonstrated to be one of the proficient parameter in the power electronics design since mid 80's. Even as latest devices from FETs, IGBTs, and super-junctions are prone to the UIS instabilities as several papers and application notes in literature have investigated and demonstrated for the maximum energy capability before fail, failure mechanism and the energy capability improvement methodology [1]–[5], [7]–[16]. Well over 500 literatures have been published either entirely or in part, with the subject of UIS mechanism. Recently, the increasing use of MOSFETs in automotive and switching applications makes the necessity to have the proper avalanche ruggedness under UIS at inductive operations. To access the robustness under pulsed conditions the maximum energy capability of the power devices must be evaluated before failure. The UIS occurs when FET is connected to a parasitic or lumped inductance and there is a change in current. An inductor is very much dependent upon the physical dimensions of the coil. As such, high values of inductance are avoided in circuit design when size constrains are in effect. The permeability component of the inductance is the permeability of the material that is encircled by the coil [17]. Inductors will always have resistance associated with the windings of the coil and whenever current flows through a resistance energy is lost in the form of heat due to Ohms Law, ($P = I^2R$) regardless of whether the current is alternating or constant.

As the inductor charged up, i.e., the energy is stored in the magnetic fields of the inductor, the current in the inductor cannot change instantaneously [17], [18]. During the storage phase of the inductor, $I_{L(STORAGE)}$ current charges through the inductor is

$$I_{L(STORAGE)} = \frac{V1}{R_T}\left(1 - e^{-\left(\frac{R_T}{L}\right)t}\right) \tag{1}$$

where V1 represents to the voltage supply and L is the inductor used, and R_T refers the total series resistance of the circuit.

While in releasing phase, the current discharges through the inductor is $I_{L(RELEASE)}$

$$I_{L(RELEASE)} = \frac{V1}{R_T}\left(e^{-\left(\frac{R_T}{L}\right)t}\right) \tag{2}$$

The inductor dissipates its stored energy into the FET during UIS test. The operating conditions are calculated rather than measured since the determination of the UIS capability using measured values for I_{DM} and T_2 seemed trivial and self-explanatory. The conventional method for the energy calculation as

$$E_{\max} = \frac{1}{2}LI_{DM}^2 \tag{3}$$

where E_{max} is the maximum energy capability, L is the inductor used, and I_{DM} is maximum current before failure.

To account for the real testing conditions, the energy handling capability of the UIS is classified based on the role of resistances. The UIS energy calculation is classified in two ways based on with and without taking resistances in account. Most of the conventional based methods follow the energy calculation without having resistances in account. The energy calculated by Eq. (3) is not equal to the calculated energy stored or dissipated by the inductor or the device. Calculations based on Eq. (3) do not take into account any resistance in the UIS circuit and Eq. (1) along with Eq. (2) are completely ignored. It is important to mention that the Eq. (3) is not valid for the circuit shown in Fig. 1, and it is only valid if the power supply is removed by switches S1 and S2 when turning the device off. Otherwise the dissipated energy will be significant higher.

During the UIS measurement, resistances play a role as energy consumers [18], [19]. To the best of authors' knowledge, only few articles have considered the resistors [11], [19]–[21]. As the unclamped inductive capability is an interactive function of other environmental stresses, it is necessary to include some calculation of other operating conditions as part of this analysis. The application note from Vishay Siliconix semiconductor and Fairchild semiconductor has mentioned the role of resistors during the calculation of the UIS energy in their data sheets [11], [20]. However, all the parameters are still not properly counted into the power for the energy derivations of the power transistors in any of these articles.

III. New Model for the UIS Test

The device layout used for the UIS test is shown in Fig. 3, which is a multi-fingered large array device with the channel

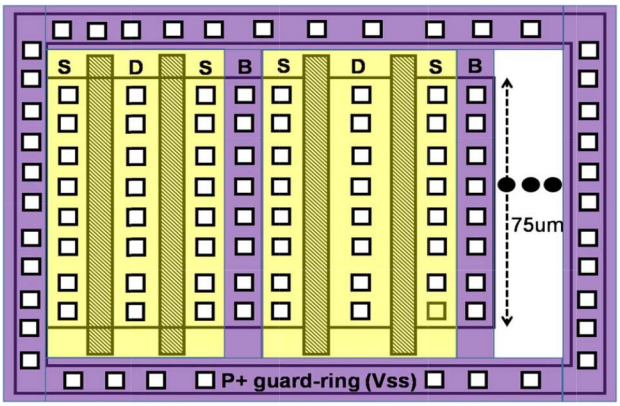
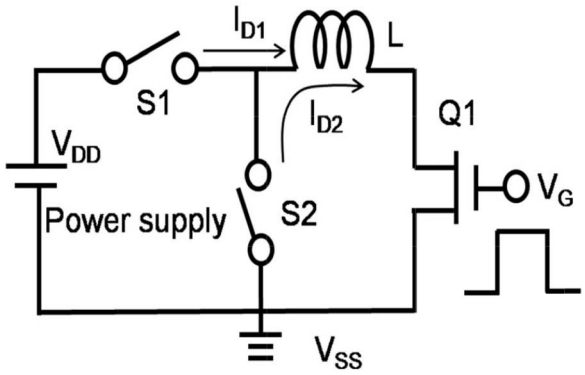


Fig. 3. Layout top-view of 5V-NMOSFETs.

(a)



(b)

Fig. 4. For UIS test (a) commercially used UIS tester ITC55100 and (b) simplified schematic diagram.

length of 0.6μm, unit finger width of 75μm. LAD structures with total width of 6000μm and 12000μm is considered to study in this paper. Except the P+ guard ring, each source of the device is butted with a P+ pick-up (S and B in Fig. 3) to equalize the substrate resistance (R_{sub}) of the parasitic n-p-n bipolar junction transistor (BJT).

The equipment used to evaluate the UIS test, a commercial UIS tester ITC55100 is shown in Fig. 4(a) and its simplified schematic diagram as shown in Fig. 4(b) [21]–[23]. In this paper, SOP-8 type package is used for the UIS measurement. The voltage and current waveforms of the 5-V NMOSFETs for L = 0.5mH under the UIS test have been shown in Fig. 2. At the onset of the test, the switch S1 closes, and the voltage V_G is

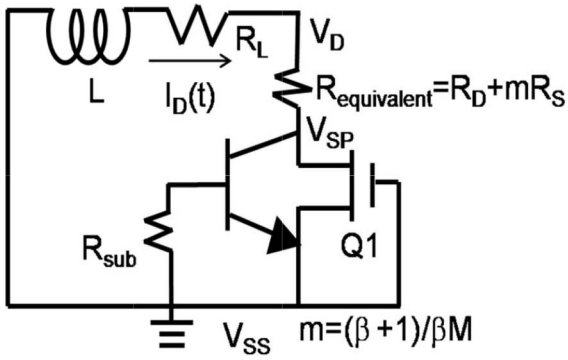


Fig. 5. The equivalent circuit of the device under the UIS test at the period when the channel turns off.

applied to the gate of the transistor Q1. So, the current starts to flow from the power supply V_{DD} to Q1 through the inductor L, resulting in the current I_{D1} increasing linearly with time (0 to 202μs in Fig. 2(a) and 0 to 337μs in Fig. 2(b)). As the current reaches the setting point (I_o), the switches S1 opens, S2 closes, and the channel of transistor turns off ($V_G = 0V$) [20]–[26]. Then, the inductor releases its stored energy to keep the current flowing, resulting in the current I_{D2} decreasing linearly with time (202μs to 239μs and 337μs to 403.4μs as shown in Fig. 2(a) and (b), respectively). Due to the switches, there is an arc occurred at the transient that the switch S1 turns off and switch S2 turns on to result in the current (I_{spike}) higher than the I_o.

The equivalent circuit and cross-sectional view of the 5-V NMOSFETs at the period, when the channel turns off, are shown in Fig. 5.

Based on the circuit shown in Figs. 6(a) and (b), the drain current I_D can be written as

$$L\frac{dI_D(t)}{dt} + R_T I_D(t) + V_{SP} = 0 \tag{4}$$

where $R_T = R_L + R_{equivalent}$, R_L is the series resistance of the inductor [11], [19], [20] depends on types of inductor is used for the testing, $R_{equivalent}$ is the equivalent series resistance of the drain and source can be calculated either by SPICE model [27], [28] or measured from IV curve, and V_{SP} is the summation of the voltages across the drain and the source junctions ($V_C + V_E$), which can be treated as a constant when the parasitic n-p-n BJT turns on [29], [30]. In the UIS measured waveforms, V_{SP} value is chosen at the end of discharging period, i.e., V_{SP} is always 10-20% larger than BV_{DSS}, (in Fig. 2(a) and 2(b)) when device avalanched near the rated capability. From Fig. 2, it can be found that the 5-V NMOSFETs are biased at the avalanche regime (>11V) when the channel turns off (T_2).

Assuming the channel turn-off transient (202μs in Fig. 2(a) and 337μs in Fig. 2(b)) as the time zero, the drain current (I_D) of 5V NMOSFETs is

$$I_D(t) = I_0 \exp\left(\frac{-R_T t}{L}\right) - \frac{V_{SP}}{R_T}\left(1 - \exp\left(\frac{-R_T t}{L}\right)\right) \tag{5}$$

where $I_o = I_D(0)$.

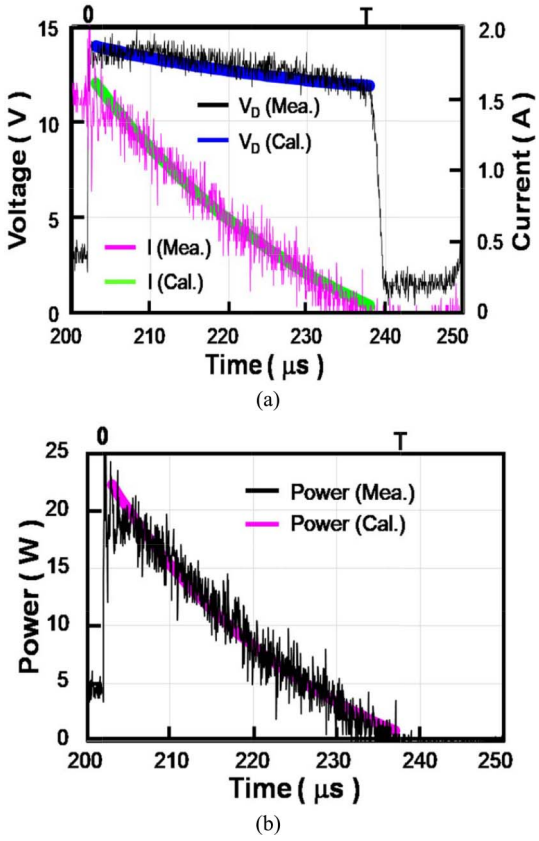


Fig. 6. Measured and calculated (a) voltage and current waveforms, (b) powers under W = 6000μm.

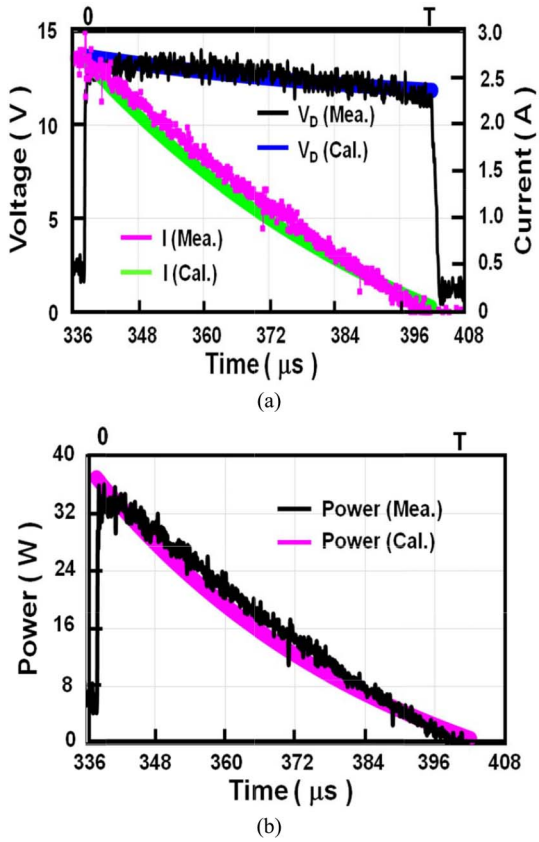


Fig. 7. Measured and calculated (a) voltage and current waveforms, (b) powers under W = 12000μm.

The drain voltage (V_D) of 5-V NMOSFETs is

$$V_D(t) = I_0 \exp\left(\frac{-R_T t}{L}\right) - \frac{V_{SP}}{R_T}\left(1 - \exp\left(\frac{-R_T t}{L}\right)\right) R_{equivalent} + V_{SP} \tag{6}$$

So, the power (P_D) can be written as

$$\begin{aligned} P_D(t) &= I_D(t)^2 R_{equivalent} + I_D(t) V_{SP} \\ &= \left[\left(I_0^2 + \frac{2V_{SP}I_0}{R_T} + \frac{V_{SP}^2}{R_T^2}\right)\exp\left(\frac{-2R_T t}{L}\right) \right. \\ &\quad \left. - \frac{2V_{SP}}{R_T}\left(I_0 + \frac{V_{SP}}{R_T}\right)\exp\left(\frac{-R_T t}{L}\right) + \frac{V_{SP}^2}{R_T^2}\right] R_{equivalent} \\ &\quad + \left[I_0 \exp\left(\frac{-R_T t}{L}\right) - \frac{V_{SP}}{R_T}\left(1 - \exp\left(\frac{-R_T t}{L}\right)\right)\right] V_{SP} \end{aligned} \tag{7}$$

Figs. 6(a) and 7(a) show the calculated voltage and current waveforms based on Eq. (5) and Eq. (6) with R_T of 15Ω and $R_{equivalent}$ of 1.33Ω, which can well match the measured result in Fig. 2(a) while $R_{equivalent}$ of 0.7Ω for W = 12000μm in Fig. 2(b). Hence, the calculated maximum power based on Eq. (7) also can well fit the measured power based the measured I-V curves in Fig. 2. These give the direct evidences to prove that the three equations can well depict the electrical and thermal behaviors of the 5-V NMOSFETs under the UIS test.

The energy stored on the inductor is released completely as the drain current I_D decreases to zero. Thus, the energy releasing time of the inductor (T) from Eq. (4) is

$$T = \frac{L}{R_T} Ln\left(1 + \frac{I_0 R_T}{V_{SP}}\right) \tag{8}$$

Integrating the generated powers, the energies dissipated by the 5-V NMOSFETs (E_D) is obtained as

$$\begin{aligned} E_D &= \int_0^T P(t)dt = \int_0^T I_D(t)^2 R_{equivalent} + I_D(t) V_{SP} dt \\ &= \left[\frac{L}{2R_T}\left(I_0^2 + \frac{2V_{SP}I_0}{R_T} + \frac{V_{SP}^2}{R_T^2}\right)\left[1 - \left(1 + \frac{I_0 R_T}{V_{SP}}\right)^{-2}\right] \right. \\ &\quad - \frac{2LV_{SP}}{R_T^2}\left(I_0 + \frac{V_{SP}}{R_T}\right)\left[1 - \left(1 + \frac{I_0 R_T}{V_{SP}}\right)^{-1}\right] \\ &\quad \left. + \frac{V_{SP}^2 L}{R_T^3} Ln\left(1 + \frac{I_0 R_T}{V_{SP}}\right)\right] R_{equivalent} \\ &\quad + \left[\frac{L}{R_T} I_0 \left[1 - \left(1 + \frac{I_0 R_T}{V_{SP}}\right)^{-1}\right] \right. \\ &\quad \left. - \frac{V_{SP} L}{R_T^2}\left(Ln\left(1 + \frac{I_0 R_T}{V_{SP}}\right) + \left(1 + \frac{I_0 R_T}{V_{SP}}\right)^{-1} - 1\right)\right] \\ &\quad \times V_{SP} \end{aligned} \tag{9}$$

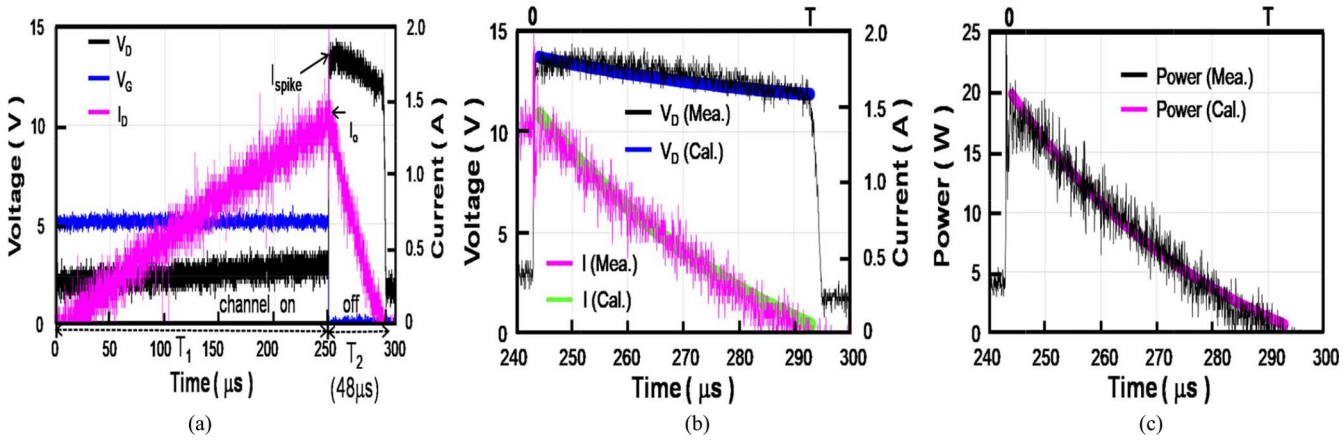


Fig. 8. The UIS Waveforms for L = 0.75mH under W = 6000μm, (a) measured current and voltage waveforms, comparison between measured and calculated (b) voltage and current waveforms, (b) powers.

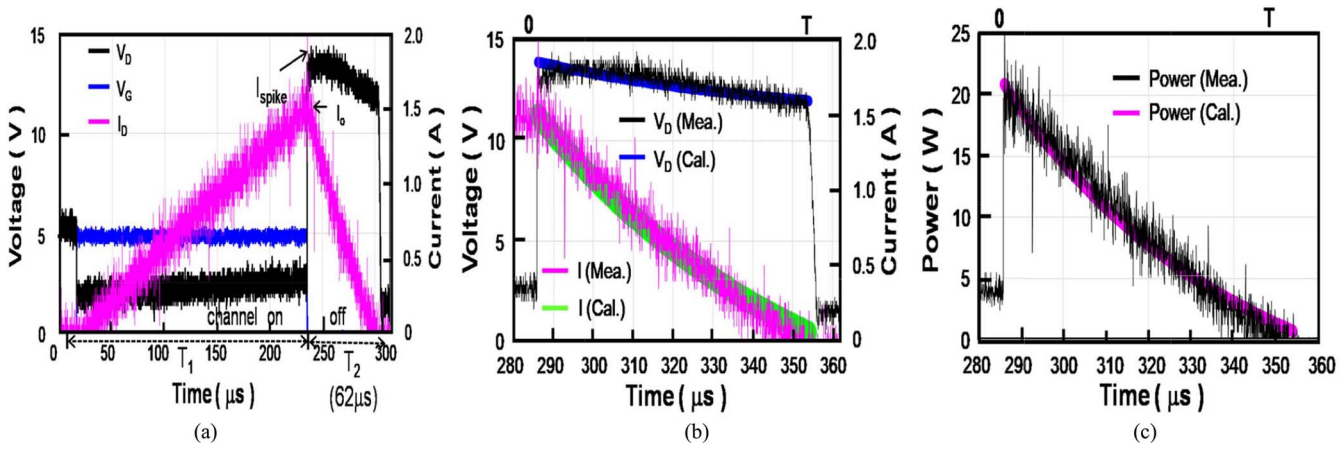


Fig. 9. The UIS Waveforms for L = 1.0mH under W = 6000μm, (a) measured current and voltage waveforms, comparison between measured and calculated (b) voltage and current waveforms, (b) powers.

Similarly, the energy generated by inductor (E_L) is calculated as

$$E_L = \int_0^T I_D(t)^2 R_L dt = \left[\frac{L}{2R_T}\left(I_0^2 + \frac{2V_{SP}I_0}{R_T} + \frac{V_{SP}^2}{R_T^2}\right)\left[1 - \left(1 + \frac{I_0 R_T}{V_{SP}}\right)^{-2}\right] - \frac{2LV_{SP}}{R_T^2}\left(I_0 + \frac{V_{SP}}{R_T}\right)\left[1 - \left(1 + \frac{I_0 R_T}{V_{SP}}\right)^{-1}\right] + \frac{V_{SP}^2 L}{R_T^3} Ln\left(1 + \frac{I_0 R_T}{V_{SP}}\right)\right] R_{equivalent} \quad (10)$$

From Table II, the dissipation energy (E_D) of the 5-V NMOSFETs based on Eq. (9) is very close to that evaluated by integrating the measured power in Fig. 6(b) and 7(b). This demonstrates that Eq. (9) is valid for calculating the dissipation energy of the 5-V NMOSFETs. It also can be seen that the energy ($LI^2/2$) stored on the inductor during the channel turn-on period (T_1 in Fig. 2) is equal to the summation of the energies dissipated by the 5-V NMOSFETs (E_D of Eq. (9)) and the series resistor of the inductor (E_L of Eq. (10)). It is verifying that the Eq. 3 ($LI^2/2$) is not all dissipated by the 5-V NMOSFETs. Moreover, the energy dissipated by the series resistance of the inductor is no less than that by the 5-V NMOSFETs and this effect cannot be neglected.

TABLE I
CALCULATION OF TIME IN AVALANCHE (T_2) BASED ON CONVENTIONAL UIS MODEL UNDER 0.5MH

(T_2=LI_o/V_o)	W=6000μm	W=12000μm
T_2	(0.5mH×1.6A/13V) =61.5μs	(0.5mH×2.7A/13V) =103.8μs

To approve the calculation from Eq. (9) and Eq. (10), the UIS test has been performed with two other inductor values (L = 0.75mH and 1mH) under W = 6000μm. The voltage and current waveforms, of the 5-V NMOSFETs for L = 0.75mH and L = 1mH under the UIS test have been shown in Figs. 8(a) and 9(a), respectively. It is clearly shown that an arc occurred at the transient that the switch S1 turns off and switch S2 turns on to that result in the current (I_{spike}) higher than the I_o.

The discharging time T_2 when channel turned off is 48μs and 62μs under 0.75mH and 1mH, respectively. Figs. 8(b) and 9(b) show the calculated voltage and current

TABLE II
STORED AND DISSIPATED ENERGIES IN THE INDUCTOR AND 5-V NMOSFETS UNDER L = 0.5MH

	$0.5LI^2$	Energy measured in Fig. 7 and 8	E_D (Eq. (9))	E_L (Eq. (10))
W= 6000μm	6.4E-4 Joule	3.31E-4 Joule	3.18E-4 Joule	3.24E-4 Joule
W= 12000μm	18.2E-4 Joule	10.2E-4 Joule	9.9E-4 Joule	10.1E-4 Joule

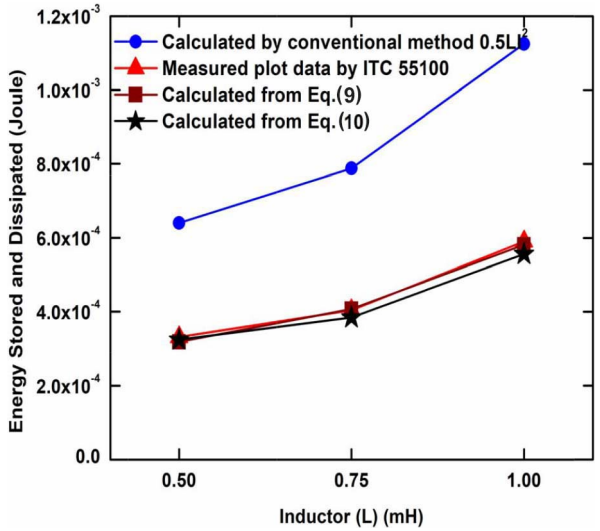


Fig. 10. Energy comparison between calculated by Eq. (3) and stored or dissipated energy in 5-V NMOSFETs.

waveforms based on Eq. (5) and Eq. (6) which are very well match the measured result in Figs. 8(a) and 9(a), respectively. The calculated power based on Eq. (7) also compared with the measured power based on the measured I-V curves in Figs. 8(a) and 9(a) as shown in Figs. 8(c) and 9(c), respectively. From Figs. 8 and 9, it can be concluded that Eqs. (5), (6), and (7) can fit perfectly to the measured data from the UIS tester.

Table III shows the stored energies and the dissipated energies under different inductor values (L = 0.5mH, 0.75mH, and 1.0mH). The comparison is shown between conventional calculation ($LI^2/2$), measured data from UIS tester, calculated from E_D (Eq. (9)), and calculated from E_L (Eq. (10)) for different inductor values. Fig. 10 shows the energy stored and dissipation comparison under different L values. The real calculation from measured data is almost half of the conventional calculated energy by Eq. (3). This much variations use to create misconception during design and hamper the design goal.

IV. CONCLUSION

For the power transistors, the series circuit resistance reduces the device avalanche stress during unclamped inductive switching (UIS) test at inductive operations. A theoretical model for the UIS has been demonstrated and practically verified with-in silicon experimental results that can well describe to the electrical and the thermal behaviors of the power transistor under the UIS test, as long as the series resistances of the inductor and the power transistor are counted. Otherwise, the dissipation energy of the power transistor during the UIS test will be overestimated.

TABLE III
COMPARISON BETWEEN THE STORED AND THE DISSIPATED ENERGIES AT DIFFERENT INDUCTORS (L = 0.5/0.75/1.0 MH) IN 5-V NMOSFETS

	L=0.5 mH	L=0.75 mH	L=1 mH
$0.5LI^2$	6.4E-4 Joule	7.88E-4 Joule	11.25E-4 Joule
Energy measured in Fig. 7(b)	3.31E-4 Joule	NA	NA
Energy measured in Fig. 8(c)	NA	4.04E-4 Joule	NA
Energy measured in Fig. 9(c)	NA	NA	5.93E-4 Joule
E_D (Eq. (9))	3.18E-4 Joule	4.07E-4 Joule	5.81E-4 Joule
E_L (Eq. (10))	3.24E-4 Joule	3.84E-4 Joule	5.56E-4 Joule

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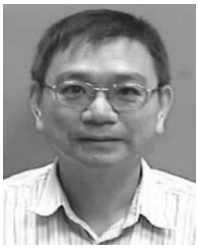
Karuna Nidhi received the B.E. degree in electrical and electronics engineering from Visvesvaraya Technological University, India, in 2010, the M.S. degree from Asia University, Taichung, Taiwan, in 2012, and the Ph.D. degree from National Chiao Tung University, Hsinchu, Taiwan, in 2019.

He is currently a Principal Engineer with Vanguard International Semiconductor Corporation, Hsinchu, Taiwan. His current research interests include device reliability and ESD protection design.

Jian-Hsing Lee joined Taiwan Semiconductor Manufacturing Corporation, Hsinchu, Taiwan, in 1989. He is currently the Director of the Device Engineering Division, Vanguard International Semiconductor Corporation, Hsinchu.

Dr. Lee was awarded as the TSMC Academician for contributions to ESD and latch-up in CMOS technologies.



Shao-Chang Huang received the B.S. and M.S. degrees in electrical engineering from National Cheng Kung University, Tainan, Taiwan, in 1994 and 1996, respectively, and the Ph.D. degree from the Institute of Electrical and Control Engineering, National Chiao Tung University, Hsinchu, Taiwan, in 2011.

From 1998 to 1999, he was engaged in thin-film-transistor devices with ERSO, ITRI, Taiwan. From 1999 to 2015, he worked on ESD/latch-up/IO circuit researches in UMC, HBA, TSMC, NOVATEK, eMemory, iMQ, and Fiti. In 2015 July, he joined Vanguard International Semiconductor Corporation, Hsinchu, where he is currently a Manager with the Large Array Device Department, Device Engineer Division.

Ming-Dou Ker (Fellow, IEEE) received the Ph.D. degree from the Institute of Electronics, National Chiao Tung University (NCTU), Hsinchu, Taiwan, in 1993.

He is currently a Distinguished Professor with the Institute of Electronics, NCTU, where he is the Director of the Biomedical Electronics Translational Research Center.

Dr. Ker is currently serving as an Editor for the IEEE TRANSACTIONS ON DEVICE AND MATERIALS RELIABILITY and an Associate Editor for the IEEE TRANSACTIONS ON BIOMEDICAL CIRCUITS AND SYSTEMS.