Design of Fin-Diode-Triggered Rotated Silicon-Controlled Rectifier for High-Speed Digital Application in 16-nm FinFET Process

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***Abstract*— The FinFET architecture has widely been used in the digital circuit application, due to the good short channel effect control and driving current boost. However, the worse thermal dispassion and smaller effective silicon volume would cause the significant impacts during the circuits under electrostatic discharge (ESD) event. Thus, the ESD protection device should be installed into the high-speed digital circuit to enhance the ESD robustness. To avoid the effect of circuit performance, the parasitic capacitance of ESD device must be as low as possible. In this article, two types of Fin-diode-triggered rotated silicon-controlled rectifier (SCR) with dual ESD current path have been proposed and verified in a 16-nm FinFET CMOS process. The proposed devices have better current-handling capability, sufficiently low parasitic, compact lay-out area, and low leakage current.**

***Index Terms*— Diode triggered, electrostatic discharge (ESD), FinFET architecture, silicon-controlled rectifier (SCR).**

I. Introduction

With the development of high-speed and low-power consumer products, CMOS field-effect transistors (FETs) are continuously shrinking. To achieve a good short channel effect control and driving current boost, the FinFET architecture has widely been used in the digital circuit application [1], [2], mostly for low-voltage applications (0.8–1.2 V) [3]. However, the electrostatic discharge (ESD) robustness is an important issue from the early FinFET process [4]. Due to the worse thermal dispassion and smaller effective silicon volume, the FinFET devices are weaker than the planar one under the ESD events. Thus, the ESD protection devices should be installed to protect the internal circuit against ESD stresses [5], [6]. On the other hand, the parasitic effects of ESD protection devices for high-speed digital circuit application should be minimized to ensure that the performance of the circuit would not be degraded.

The silicon-controlled rectifier (SCR) device is a common device for ESD protection in advanced FinFET technologies [7]–[9] due to the high ESD robustness within a small silicon area. By using the SCR device as an ESD protection device, the I–V characteristics of on-chip ESD protection SCR must be within the ESD protection window [10] to protect the internal circuits avoid latch-up issue [11]–[13].

In this article, a new SCR device is proposed and fabricated in a 16-nm FinFET CMOS process. The new proposed rotated SCR devices not only can release ESD current through the path which perpendicular to FINs but also minimize the ESD path.

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II. Device Structures

A. Prior Art Design

The SCR devices that include trigger circuit can provide better ESD robustness since SCR structures are known to suffer from high trigger voltage and slow turn-on speed [14]. Fig. 1 shows the Fin-SCR device (P+, NW, PW, and N+) [15] and the corresponding cross-sectional view of the prior art design, which includes one P+/N-well diode and one P-well/N+ diode. The first diode of Fin-SCR has P+ connected to the anode node and N+ connected to the P+ of the second diode with metal routing. The second diode of Fin-SCR has P+ connected to the N+ of the first diode and N+ connected to the cathode node with metal routing. To realize the shortest path of parasitic SCR, the P-well of the second diode has been surrounded by the N-well of the first diode due to the design rule. The distance of SCR path (P1) is about 1.26 μm. The Fin-SCR device is isolated from the common P-substrate by deep n-well (DNW).

In order to enhance the turn-on speed of Fin-SCR, the Fin-diode-triggered Fin-SCR (DTSCR) has been fabricated in this article and shown in Fig. 1(a). The anode node is connected to the P+ of D1, and the cathode node is connected to the N+ of D4. These two diodes are isolated from the common

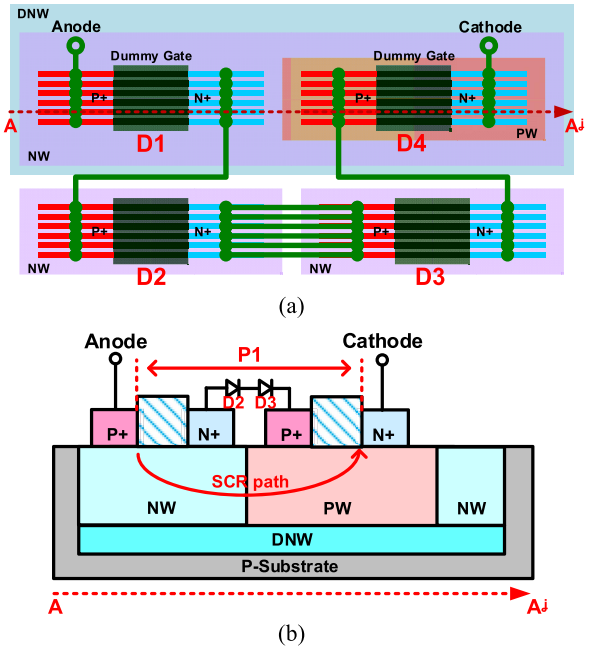

Fig. 1. Top view of (a) Fin-diode-triggered Fin-SCR (DTSCR) and (b) corresponding cross-sectional view of the prior art Fin-SCR device.

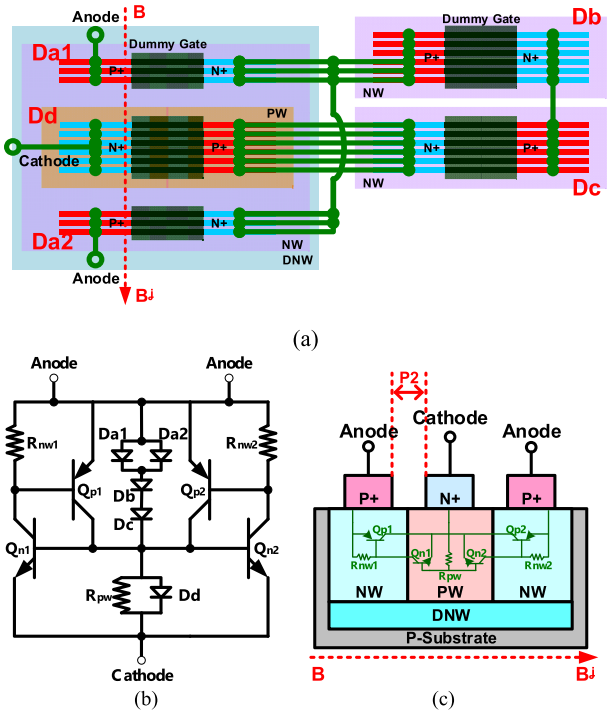

Fig. 2. (a) Top view of N-type Fin-diode-triggered rotated SCR. (b) Equivalent circuit of N-type DTRSCR. (c) Corresponding cross-sectional view of the N-type rotated SCR.

P-substrate by DNW. The other two diodes (D2 and D3) are chosen as P+/N-well diode due to the consideration of the layout area. During the ESD event, diode string can be turned on quickly and triggered the SCR path to release the ESD current. However, the Fin-SCR device has a large ON-state resistance (R_{ON}) under ESD stress due to the longer SCR path.

B. Proposed N-Type Fin-Diode-Triggered Rotated SCR

To minimize the ESD path, the current path of proposed rotated SCR devices is perpendicular to FINs. In order to enhance the turn-on speed, the proposed SCR devices are based on a diode string embedded SCR.

Fig. 2 shows the proposed N-type rotated SCR device (Da1, Da2, and Dd). In order to let the parasitic SCR path (P2) as short as possible, the first diode has been separated into two diodes, where the Fin numbers of each first diode are half than that second diode. These two parallel diodes are equivalent in size to the second diode, and both have P+ connected to the anode node and N+ connected to the P+ of the second diode. The second diode has P+ connected to the N+ of the first diode and N+ connected to the cathode node. The N-type rotated SCR device is also isolated from the common P-substrate by DNW. To ensure the shortest parasitic SCR path, the distances of the first diode and second diode are followed by the minimum value in the design rules.

Fig. 2(a) shows the proposed N-type Fin-diode-triggered rotated SCR (DTRSCR), which includes first parallel diodes (Da1 and Da2), Db, Dc, and Dd. The diodes of trigger circuit (Dc and Dd) are chosen as P+/N-well diode due to the consideration of the layout area. The equivalent circuit of N-type DTRSCR is shown in Fig. 2(b) with the parasitic BJTs and resistors, and the corresponding cross-sectional view of the N-type rotated SCR is also shown in Fig. 2(c). During ESD stress, the ESD current flows through Da1 (Da2), Db, and Dc, and the voltage of P-well parasitic resistance (Rpw) will increase. Due to the rising voltage, the NPN BJTs (Qn1 and Qn2) may turn on first, and then, they will help PNP BJTs (Qp1 and Qp2) to be turned on. The positive feedback of those parasitic BJTs in SCR [16] can provide a current path to release the ESD current. Furthermore, the proposed SCR can release the ESD current by two current paths [17], and it means that more ESD current can be discharged under the same layout area than the single path SCR device. Compared with prior art design, the distance of proposed N-type DTRSCR path (P2) is about 0.4 μm, which is 68% smaller than P1.

C. Proposed P-Type Fin-Diode-Triggered Rotated SCR

Fig. 3 shows the proposed P-type rotated SCR (De, Dh1, and Dh2), and the corresponding cross-sectional view of the P-type rotated SCR is also shown in Fig. 3(c). In order to let the parasitic SCR path (P3) as short as possible, the second diode, which has N+ connected to the cathode node, is separated into two diodes such as Dh1 and Dh2. These two diodes are connected in parallel, and the Fin numbers of each second diode are half than that the first diode. The distances of the first diode and second diode are followed by the minimum value in the design rules. In order to isolate the P-type rotated SCR device from the common P-substrate, the DNW layer has been used.

Fig. 3(a) shows the proposed P-type Fin-diode-triggered rotated SCR (DTRSCR), which includes De, Df, Dg, and fourth parallel diodes (Dh1 and Dh2). The diodes of trigger circuit (Df and Dg) are chosen as P+/N-well diode due to the consideration of layout area. To ensure the correct current path, the P-type DTRSCR device has also been isolated from

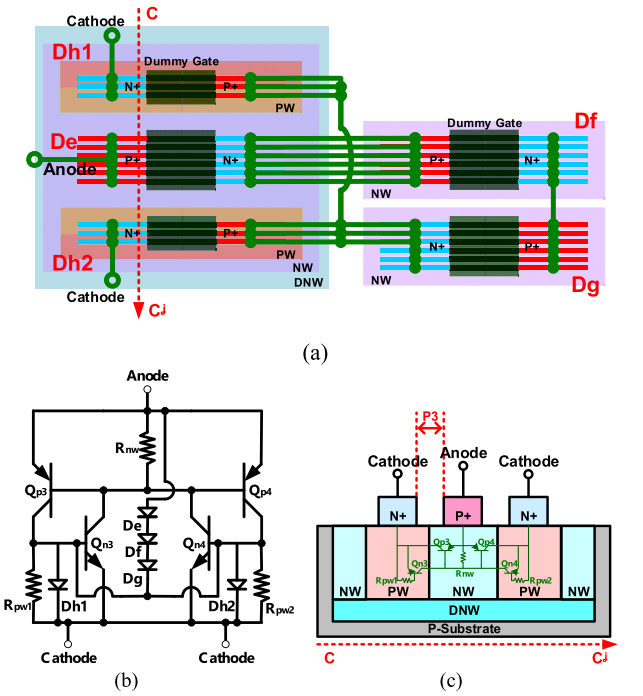

Fig. 3. (a) Top view of P-type Fin-diode-triggered rotated SCR. (b) Equivalent circuit of P-type DTRSCR. (c) Corresponding cross-sectional view of the P-type rotated SCR.

the common P-substrate by DNW. The equivalent circuit of P-type DTRSCR is shown in Fig. 3(b) with the parasitic BJTs and resistors. As the ESD current flows from anode to cathode through De, Df, Dg, and Dh1 (Dh2), this diodes' path can increase the voltage of P-well parasitic resistance (Rpw1 and Rpw2). Due to the rising voltage, the NPN BJTs (Qn3 and Qn4) and the PNP BJTs (Qp3 and Qp4) can be turned on in order by the positive feedback and then provide a current path to release the ESD current. According to the dual SCR current path, the proposed device can discharge more ESD current than that single path SCR device under the same layout area. Compared with prior art design, the distance of proposed N-type DTRSCR path (P3) is about 0.44 μm, which is 65% smaller than P1.

III. Experimental Results

The test devices of the prior art design, N-type DTRSCR, and P-type DTRSCR have been fabricated in a 16-nm FinFET CMOS process. Each test circuit is implemented with ground–signal–ground (G–S–G) RF test pattern for ON-wafer two-port S-parameter measurement.

A. Transmission Line Pulsing Measurement

To investigate the I–V characteristics of the test devices, a TLP generator [18] with a 10-ns rise time and a 100-ns pulse width is used. Fig. 4(a) shows the TLP-measured I–V characteristics of the proposed SCR devices and prior art DTSCR device with 20 fingers under a positive anode-to-cathode TLP stress. The TLP measurements are ON-wafer, which are measured without bonding wire. The SCR current paths of the proposed N-type DTRSCR, P-type DTRSCR,

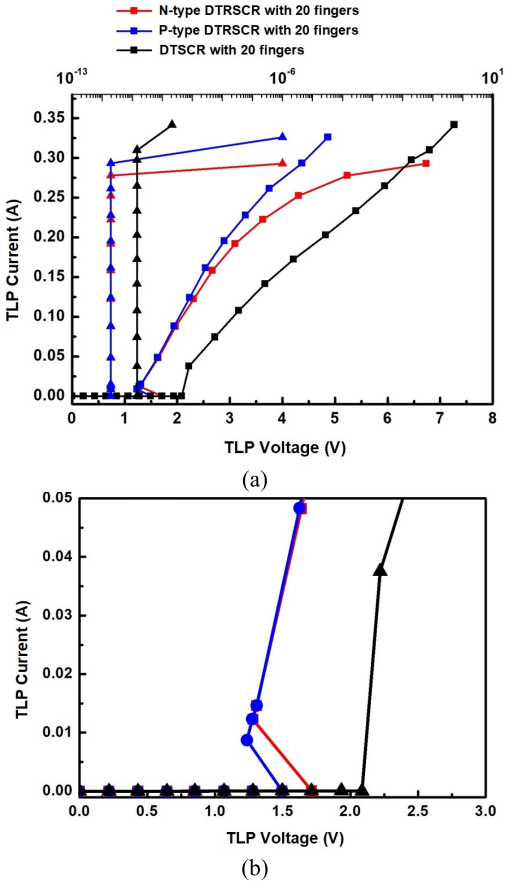

Fig. 4. (a) TLP-measured I–V curves of proposed devices and prior art DTSCR device with 20 fingers. (b) Zoomed-in view for investigating the trigger voltage (V_{t1}) and holding voltage (V_h).

and prior art DTSCR device with 20 fingers can be trigger on at 1.71, 1.50, and 2.09 V, respectively. The proposed N-type and P-type DTRSCR devices have snapback phenomenon at 1.28 and 1.24 V, respectively, but prior art DTSCR device has no obvious snapback phenomenon. According to the snapback phenomenon, the SCR path of the proposed SCR devices can surely be triggered under positive anode-to-cathode ESD stress. The second breakdown currents (I_{t2}) of the proposed N-type DTRSCR, P-type DTRSCR, and prior art DTSCR device with 20 fingers are 0.29, 0.33, and 0.34 A, respectively.

In order to investigate the turn-on speed of the proposed devices during the ESD stress, another very fast TLP (VF-TLP) system with a 200-ps rise time and a 5-ns pulse width is used. The VF-TLP measurements are ON-wafer, which are measured without bonding wire. Fig. 5(a) shows the comparison of VF-TLP I–V curves of proposed SCR devices and prior art DTSCR device. Compared to the DTSCR device, the proposed N-type and P-type DTRSCR devices both have the lower turn-on resistance. Fig. 5(b) shows the zoomed-in view of VF-TLP measured I–V curves. According to the measurement results, the proposed N-type and P-type DTRSCR devices have a lower trigger voltage as 1.76 and 1.75 V, respectively. The prior art DTSCR device has a higher trigger voltage as 2.80 V.

To investigate the clamping voltage of the proposed SCR devices and prior art DTSCR device, the VF-TLP measured

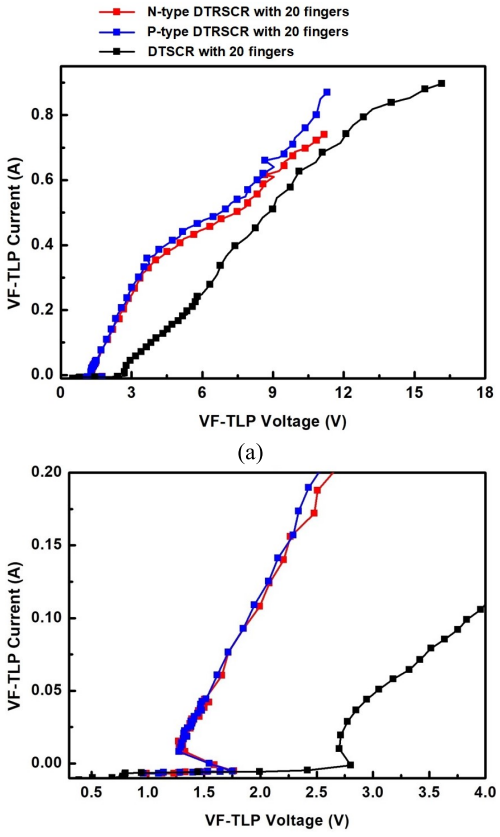

Fig. 5. (a) VF-TLP measured *I–V* curves of proposed devices and prior art DTSCR device with 20 fingers. (b) Zoomed-in view for investigating the trigger voltage (V_{t1}) and holding voltage (V_h).

voltage waveform under 0.6-A condition is shown in Fig. 6, and the voltage waveform is chosen under 0.6-A condition of VF-TLP current. The peak overshoot voltages of N-type DTRSCR, P-type DTRSCR, and DTSCR are 8.25, 7.65, and 9.24 V, respectively. As shown in Fig. 6, the clamping voltages of N-type DTRSCR and prior art DTSCR are similar, but P-type DTRSCR has lower clamp voltage.

B. Parasitic Capacitance

The parasitic effects of test devices are captured with the ON-wafer two-port S-parameter measurement from the anode port of P-type DTRSCR and the cathode port of N-type DTRSCR. In order to extract the exact parasitic capacitance of the stand-alone device at high frequency, the parasitic effects of the pads and the metal routing have been de-embedded [19], and the value of device capacitance can be calculated. Fig. 7 shows the extracted parasitic capacitance of the test devices from 2 to 13 GHz. According to Fig. 7, the DTSCR device has the lowest parasitic capacitance, and the proposed devices have a slightly larger parasitic capacitance. The test SCR devices would have a similar parasitic capacitance at a higher frequency. As frequency increases, the capacitance values of the proposed SCR devices are similar to those of the prior SCR device. It means that the proposed SCR devices would have lower capacitance value at high frequency, so the

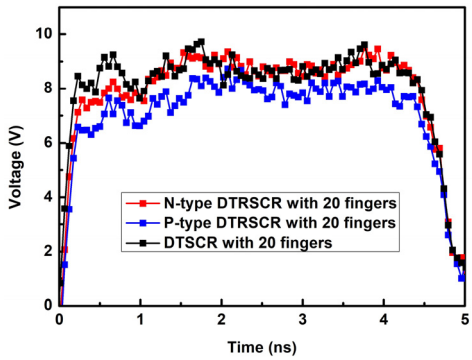

Fig. 6. VF-TLP measured voltage waveform of proposed devices and prior art DTSCR device with 20 fingers under 0.6-A condition.

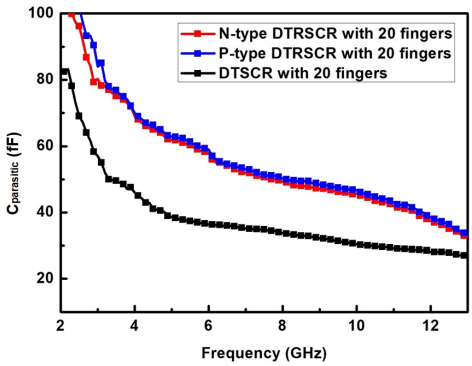

Fig. 7. Parasitic capacitance of the proposed devices and prior art DTSCR device with 20 fingers.

average capacitance value would not be too large and more suitable for the high-frequency application.

C. Leakage Current

Fig. 8(a) shows the leakage currents of all devices, which were measured from anode port to cathode port. Due to the FinFET architecture mostly been used in the low-voltage applications (0.8–1.2 V) for digital circuit, the leakage current at 0.8 and 1.2 V should be noticed. In this article, the layout parameters of P-type and N-type SCR are slightly different, such as the spacing of P-well and metal routing. Therefore, the distance between anode and cathode of P-type SCR is longer than that of N-type SCR, which might cause the difference of leakage current.

As devices under 0.8-V supply voltage, the leakage current of DTSCR, N-type DTRSCR, and P-type DTRSCR is 2, 1.9, and 1.9 pA at 25 °C, respectively. The leakage current of DTSCR, N-type DTRSCR, and P-type DTRSCR devices is 2.9 nA, 563.8 pA, and 145.2 pA at 80 °C, respectively. When the temperature rises to 125 °C, the leakage currents from DTSCR to P-type DTRSCR are 5.5, 16.1, and 3.2 nA, respectively. As the device at 1.2-V supply voltage, the leakage currents of all devices are around 20 pA at 25 °C. When the temperature rises to 80 °C, the leakage current of DTSCR, N-type DTRSCR, and P-type DTRSCR is 98.4 nA, 2.5 nA, and 437.5 pA, respectively. The leakage current of devices from DTSCR to P-type DTRSCR is 326.4, 358.9, and 181.7 nA at 125 °C, respectively. For the proposed N-type and

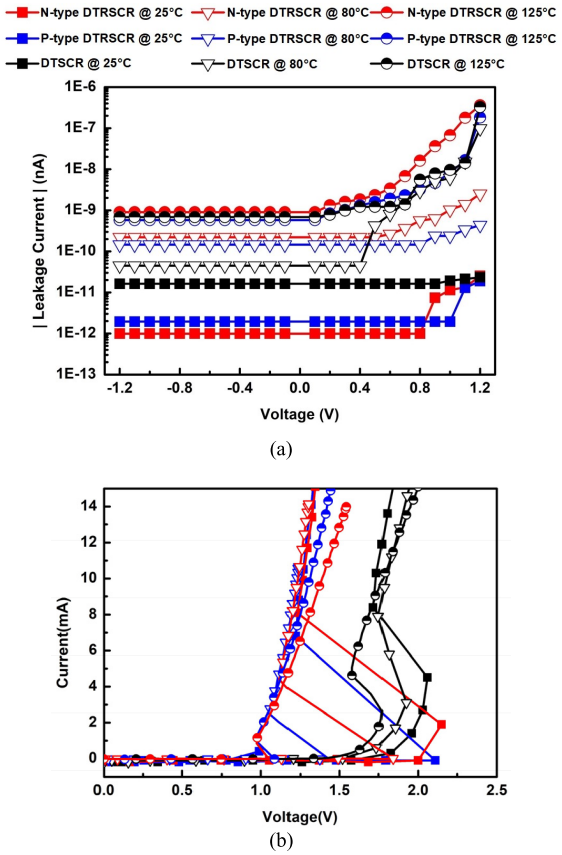

Fig. 8. (a) Measured leakage current and (b) dc *I–V* curve of DTSCR and proposed devices at 25 °C, 80 °C, and 125 °C.

P-type DTRSCR devices, the leakage currents are sufficiently low under 0.8- or 1.2-V operating condition.

D. DC I–V Curve

To investigate the holding voltage (V_h) of the devices, the dc I–V curves of devices have been measured by curve tracers. Fig. 8(b) shows the measured dc I–V curves of all devices, which were measured from the anode port to cathode port. According to Fig. 8(b), the V_h of DTSCR, N-type DTRSCR, and P-type DTRSCR is 1.74, 1.23, and 1.22 V at 25 °C, respectively. The leakage current of DTSCR, N-type DTRSCR, and P-type DTRSCR devices is 1.71, 1.16, and 1.11 V at 80 °C, respectively. When the temperature raised to 125 °C, the leakage currents from DTSCR to P-type DTRSCR are 1.50, 0.99, and 0.98 V, respectively. The lowest V_h of the proposed N-type and P-type DTRSCR devices is around 1 V, so the proposed SCR devices are suitable for the voltage which lowers than 1-V operating condition.

IV. Comparison and Discussion

A. Discussion of Measurement Results

An ESD protection device for a high-speed application must need a higher ESD level and lower parasitic effect. The current-handling ability of the protection device is usually expressed in terms of its second breakdown current (I_{t2}). However, the difference in I_{t2} values between the proposed devices and prior device in this article is not obvious. According to

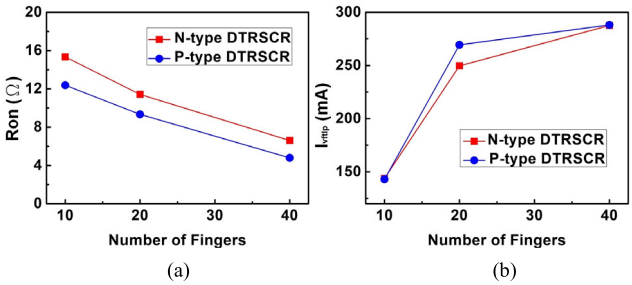

Fig. 9. (a) ON-state resistances of the proposed N-type and P-type DTRSCR devices with a different number of fingers. (b) VF-TLP measured current value at 3 V (I_{vftlp}) of proposed N-type and P-type DTRSCR devices with a different number of fingers.

this reason, the TLP measured current value at 3 V (I_{tlp}) and VF-TLP measured current value at 3 V (I_{vftlp}) have been used to compare the current-handling capability of the protection device in this article.

Due to the strict design rule of FinFET process, changing the number of fingers is a simpler way to find the difference between the size of devices, which can considerably influence the devices' current-handling capability and ON-state resistance R_{ON}. The increasing fingers' number is expected to increase the devices' current-handling capability and decrease R_{ON} because of the enlarged device size. Fig. 9(a) shows the ON-state resistances of the proposed N-type and P-type DTRSCR devices having different finger numbers and sure having lower R_{ON} when the finger numbers increase. Fig. 9(b) shows the VF-TLP measured current value at 3 V (I_{vftlp}) of proposed N-type and P-type DTRSCR devices having different finger numbers. Compared to Fig. 9(a), finger numbers of 10 and 40 have the lowest and highest I_{vftlp} and the largest and smallest R_{ON}, respectively. According to the above result, the ESD robustness can be enhanced by increasing the finger number of device, and the larger size of proposed SCR devices can provide higher ESD protection level. However, the I_{vftlp} of devices, which is not linearly increased with increasing finger number due to the maximum metal width allowed on each finger, is limited by design rule. Thus, the finger number of 20 is appropriate for SCR device. According to Fig. 5(a), the I_{t2} current of proposed devices is around 0.8 A. Therefore, four proposed SCRs in parallel can increase the I_{t2} current exceeded 2.5 A, and the layout area would be around 270 μm^2.

To avoid the latch-up issue under normal circuit operation, the holding voltage (V_h) should be higher than the supply voltage. According to the measurement result shown in Fig. 5, the V_h of proposed N-type and P-type DTRSCR devices is 1.23 and 1.22 V, respectively, and is higher than the supply voltage of the low-voltage applications (0.8–1.2 V) for digital circuit. Thus, the proposed SCR devices are free from the latch-up issue at 25 °C.

In FinFET technologies, the gate oxide breakdown voltage (BV_{ox}) is a critical parameter. The diode devices in FinFET process have the gate structure, so the bias on devices should be carefully designed under normal circuit operation. Fortunately, typical BV_{ox} in FinFET process is 3.5–5 V [20], and it means that the proposed SCR devices with ~2-V holding voltage are acceptable for low-voltage applications.

TABLE I
MEASURED RESULTS OF DEVICES

Name	DTSCR	N-type DTRSCR	P-type DTRSCR
V_{t1} (V)	2.09	1.71	1.50
I_{t2} (mA)	341.72	292.77	326.19
VF-I_{t2} (mA)	896.70	739.80	889.07
Ron (Ω)	17.73	11.42	9.33
$C_{parasitic}$ @ 10 GHz (fF)	30.40	45.62	46.65
Layout area (um^2)	98	44	58
I_{tlp} @ 3V (mA)	107.66	191.67	211.77
I_{vftlp} @ 3V (mA)	52.38	249.67	269.31
I_{tlp}/ ($C_{parasitic}$ *Layout area) ($uA/fF*um^2$)	36.1	95.5	78.3
I_{vftlp}/ ($C_{parasitic}$ *Layout area) ($uA/fF*um^2$)	17.6	124.4	99.5

Even though SCR has a low parasitic capacitance and high ESD robustness, the stand-alone SCR device cannot be switched instantly from OFF to ON. A transient voltage overshoot is observed if the applied ESD pulse has a sub-nanosecond rise time [21]. Before the SCR fully turns on, the voltage across its terminals is determined by the trigger circuit [22]. According to the above reason, the proposed DTRSCR devices, which employ the trigger circuit, can turn the SCR on quickly to provide good voltage clamping. According to the measurement results, the proposed DTRSCR devices have a good turn-on voltage of 1.71 and 1.50 V, respectively. Therefore, the proposed N-type and P-type DTRSCR devices can achieve better performance for FinFET high-speed low-voltage applications.

B. FOM Comparison

Table I shows the figures of merit (FOMs) comparison of devices. The *C*parasitic is the parasitic capacitance of the devices and has been selected at 10 GHz. For high-speed application, the higher current-handling capability and lower parasitic effect are needed, and the cost of the FinFET process is much more than that planar process, so the higher value of $I_{tlp}/(C_{parasitic} \times$ Layout area) and $I_{vftlp}/(C_{parasitic} \times$ Layout area) will be better. These two FOMs can more effectively reflect the ESD robustness of the SCR than I_{tlp}, I_{vftlp}, $C_{parasitic}$, and layout area alone. According to Table I, the test result of $I_{tlp}/(C_{parasitic} \times$ Layout area) for all devices from DTSCR to P-type DTRSCR is 36.1, 95.5, and 78.3 μA/fF·μm^2, respectively. The $I_{vftlp}/(C_{parasitic} \times$ Layout area) of DTSCR, N-type DTRSCR, and P-type DTRSCR is 17.6, 124.4, and 99.5 μA/fF·μm^2, respectively. According to the experimental results, the proposed devices both have better $I_{tlp}/(C_{parasitic} \times$ Layout area) and $I_{vftlp}/(C_{parasitic} \times$ Layout area) value, due to the fully turned on of SCR path.

TABLE II
COMPARISON OF CAPACITANCE AND ESD ROBUSTNESS BETWEEN SCR DEVICES

Name	$C_{parasitic}$ (fF)	I_{vftlp} @ 3 V (mA)	Width (um)	I_{vftlp}/ ($C_{parasitic}$ *Width) (uA/fF*um)
N-type DTRSCR	45.62	249.67	18	304.0
P-type DTRSCR	46.65	269.31	18	320.7
[8]	65	~1000	164	~93.8
[20]	~33	~100	80	~37.9
[23]	38.85	~400	~134	~76.8

Table II shows the comparison of capacitance, device width, and I_{vftlp} at 3 V among between SCR devices. In order to sustain a high level of ESD robustness, the large parasitic capacitance of the large-size device may cause large signal loss. The differences of parasitic capacitance value between proposed SCR devices and other devices are not too far, but the widths of proposed devices are much smaller than the other devices. According to the above reason, the proposed N-type and P-type DTRSCR have the highest $I_{vftlp}/(C_{parasitic} \times$ Width) value as 304 and 320.7 μA/fF·μm, respectively, and it means that the proposed devices can release more ESD current during the ESD event under same layout area.

V. CONCLUSION

The proposed rotated SCR devices have been successfully verified in a 16-nm FinFET CMOS process, where can release ESD current by the path perpendicular to FINs. The proposed N-type and P-type DTRSCR can be triggered on at 1.71 and 1.50 V, respectively. Comparing to the prior art DTSCR design, the FOMs of the proposed devices both have better current-handling capability under the same value of parasitic capacitance and also have low leakage current under low-voltage high-speed digital applications (0.8–1.2 V). Therefore, the proposed devices verified in this article will be a useful ESD protection solution for the high-speed digital applications in the FinFET CMOS technology.

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