Design of Stage-Selective Negative Voltage Generator to Improve On-Chip Power Conversion Efficiency for Neuron Stimulation

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***Abstract*— Dedicated to neuron stimulation circuits, a stage-selective negative voltage generator is proposed to enhance the overall power efficiency. Since the supplied voltage of the stimulus driver is subject to applications and treatments, an extensive output requirement of supply is demanded to achieve energy-efficient stimulation. The charge pump is implemented as a negative voltage generator for on-chip design. In a limited area, excess power loss is eliminated by reconfiguring the cascaded architecture and clocks. Digitally programmable voltage levels can be outputted by varying the number of stages dynamically. The function of stage selection is achieved by the proposed stage-selective scheme. With appreciate control, the stage-selective negative voltage generator can maintain higher power efficiency under different output voltage levels and loading conditions. The technique improves 40% power conversion ratio at most but only leads to an increment of 8% in area occupation. The measured output voltage covers from –0.3 V to –9.3 V within a maximum 5.5-mA output current, which is verified in a 0.25-μm BCD process.**

***Index Terms*— Stage-selective circuit, stage control, negative voltage generator, negative charge pump, energy-efficient.**

I. Introduction

AMONG all the DC-to-DC converters, switching capacitive converters (i.e. charge pump) are suitable for high-voltage generation in many applications, especially in neuron stimulation [1]–[8]. Microelectronics-based stimulators deliver voltage or current pulses as electrical stimulation treatment and treat neurological disorders as well [9]. For the purposes of biomedical stimulation circuits, providing a high voltage to drive a stimulator is the principal objective of a high-voltage generator. Hence, area cost and energy efficiency are the two major issues to be discussed [10]. Compared with traditional inductor-based or transformer-based converters, the charge pump favors the significantly on-chip considerations on area concerns. From the perspective of energy efficiency, it is strongly related to battery lifetime for a long period of usage. Without any off-chip components, the charge pump can effectively generate positive or negative high voltage from a lower voltage by different charge pump topologies. Therefore, it can support stimulators to deliver desired stimulus patterns. However, the organic impedance may be varied or the stimulus scale may be changed during therapeutic processes. It indicates that the required supply for stimulators is not always a fixed value [5]–[7]. In fact, it varies from several volts to tens of volts [8]. To make stimulators work more conservative, a charge pump with a wide output range is developed.

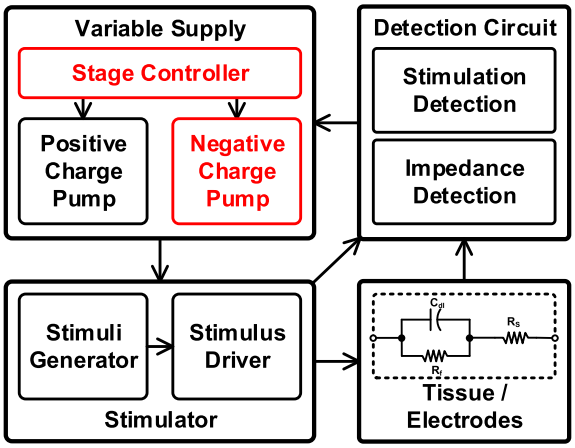

Fig. 1. A conceptual stimulation system for energy conservation includes the variable supply, the detecting circuit, and the stimulator. In this paper, a new proposal of the variable supply is composed of a stage controller and negative charge pump.

In a stimulation system, a variable supply system is an advanced integration to provide expected power dynamically and efficiently. A conceptual system is drawn in Fig. 1, containing a variable supply system, a detecting system, and stimulus drivers. In order to maximize the overall efficiency of implantable stimulators, adaptive power supply techniques are required to minimize the voltage drop across the stimuli generator. Some algorithms are imperative as criteria for dynamic reconfigurability. One of the detection circuits is accomplished by the electrode monitoring circuit (EMC) [6]. It can immediately measure the electrode output voltage and further tell the sufficiency of power supply by comparing the output voltage of electrodes and the high voltage generator. A stimulator buffer with a triode indicator [7] is used to

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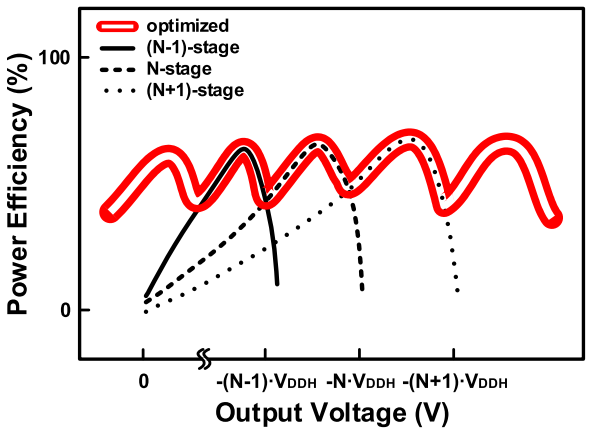


Fig. 2. An illustrated characteristic of the voltage generator (i.e. charge pump) with a fixed configuration. Black lines indicate the charge pump is implemented with an invariable architecture while the red line is an optimal performance against different output voltage.

monitor the operating region of the cascode current mirror. As long as the cascode current mirror is oppressed into the triode region, the indicator implies the inadequate power supply. Although several detection approaches are presented, an energy-efficient stimulation system may still be imperfect without the variable supply. Therefore, the charge pump with a variable output level is a decisive part to complete the entire conservative system.

One of the challenges of a variable supply system is to achieve the equilibrium of area and efficiency. More still, once the negative voltage is involved, reliability issues are critical and integrated considerations are problematic [11], [12]. Junction leakages and latch-up problems necessitate a careful solution. Besides, as if the configuration of a negative charge pump is established, the characteristic is determined as any black lines in Fig. 2. In a closed-loop system, only adjusting the reference voltage (V_{REF}) to vary the output voltage (V_{OUT}) and regulating V_{OUT} by feedback control may suffer efficiency-drop issues. In other words, the peak power efficiency occurs only at a certain voltage gain in each configuration. The excessive current loss gives rise to inferior efficacy [13]. Standing on this statement, several individual charge pump loops with different stages are integrated into a single chip. All the hills are collected as the red line shown in Fig. 2. Unfortunately, it would cost a large silicon area instead. Heretofore, efficiency maintenance and area conservation are conflicted in typical negative voltage generation.

In the sight of these reasons, a stage-selective negative voltage generator is proposed to balance the trade-offs of size and efficiency. The voltage generator is implemented with a switched-capacitor regulator in a 0.25-μm BCD process. Compare to the conventional charge pump, the key features in this work are stage selection, negative voltage operation, and efficiency maintenance. The experimental results show that the proposed stage-selective circuit for charge pump can extend the output range and improve power efficiency, though it cost few increments on the area. In this paper, the definitions of voltage generator and charge pump are equivalent. Clearly, a voltage generator is specific for its voltage conversion and the charge pump is particular about the switched capacitor operation. The paper is organized as follows: Section II reviews variable output techniques; Section III introduces the proposed circuit; Section IV presents simulated and measured results; Section V draws the conclusion.

II. Review of Variable Output Techniques

In the past, the charge pump is applied to vast integrated circuits with different requirements. For more progressive development, the charge pump is no longer being restricted by a constant voltage level. Some variable output techniques are presented to carry out more output requirements and conserve unnecessary current consumption. Previous variable output techniques are briefly introduced below for an energy-efficient system.

In the microelectromechanical system (MEMS), the variable actuation voltage is generated by the charge pump for electrostatic resonators biasing. Through external parameterized codes, the charge pump is implemented with the reconfigurable switched capacitor array [14] and even the tunable clock amplitude [15] to drive capacitive loads. In RF filters, the cascaded stages of the charge pump are gated by separated clock signals, so the output voltage can be tuned [16]. In typical flash memories, the charge pump contributes to high voltage generation whose output level depends on read, erase, and program operations. The variable output technique is achieved by adding several bypass switches [17]. It adopts a serial-parallel topology to draw a variable-conversion-ratio converter [18]. By adding several bypass switches, any reduction of the number of stages is taken place by a short circuit between the input and output terminals [19]. In [20], the charge pump combines different cell circuits so as to generate plural output voltages with superior efficacy. But for low-power RRAM realization, a main charge pump with a monitor charge pump [21] is able to adjust the number of stages and minimize current consumption. The presented stage control circuit determines the main pump configuration based on the clock comparison results. A variable charge pump is a tendency to export a larger output voltage range so far. There is no exception for neuron stimulation. With an invariable structure, the charge pump can increase or decrease output voltage with a tunable V_{REF} and in a closed-loop [7], [22]. The reconfigurable switched-capacitor network for neuron stimulation is addressed to convert an input voltage into half, double, or even triple [23], [24]. Another conventional charge pump with several paralleled bypass switches makes the structure and the output variable [25]. However, none of the state-of-the-art is applied to negative voltage operation. Most of them are hard to perform logic control in the negative voltage domain. Since the loading current varies from hundreds of nanoamps to several milliamps, a complicated topology may cause a severe parasitic effect on charge paths. Nevertheless, an additional charge pump that assists to track loading conditions would occupy redundant area cost. It does not benefit implantable biomedical applications and larger output current. Lastly, a novel charge pump intends to improve these problems and joins in negative voltage generation in this work.

III. Proposed Stage-Selective Negative Voltage Generator

A stage-selective negative voltage generator is proposed to enhance the overall power efficiency within a limited area. Typically, power losses can be classified as conduction loss, switching loss, redistribution loss and reversion loss [26]. A switched-capacitor converter performs better efficiency through proper optimization among a variety of power losses. For a wide output range, efficiency decay appears at low voltage gain cases. Power dissipates through charge conduction loss and switching loss is worsening due to more charge pump stages cascaded. Redistribution loss takes place at charge sharing between any two capacitors. The last reversion loss is about an undesirable short circuit path in the power stage of the negative charge pump. In this work, the main concept is to generate the desired output voltage with appropriate activated stages and eliminate excess power loss.

A. Proposed Stage-Selective Circuit

In a conventional configuration of the negative charge pump, charge pump cells are cascaded stage by stage and fixed. A proposed stage-selective circuit is added to make the configuration more flexible. In this work, there are two operational modes: pump mode and bypass mode. The "pump mode" is defined to increase the activated stage number of negative charge pump whereas the "bypass mode" is to decrease the activated stage number. In other words, the charge transfer path would be reconfigured from N to more than N stages in the pump mode, but it would be reconfigured from N to less than N stages in the bypass mode, where N represents the number of the activated charge pump cells.

As shown in Fig. 3(a), the operational mode is specified by the digital signals S_N and C_N through the corresponding controllers. In each stage, the stage-selective circuit consists of a stage controller, a negative level shifter (NLS_N), and a bypass switch (M_N). The external digital signal S_N is refined by the stage controller for time delay and then delivered as an internal control signal S_{NIN}. Besides, the bias VH_N is given by the stage controller as the power node of the NLS. Once the NLS received S_{NIN}, it would convert and extend the voltage domain from positive to negative at S_{NOUT} and SW_N. In an NLS, M_{P1} and M_{P2} are used to sense input voltage levels. The associated connection is annotated in Fig. 4. By comparing the pull-up current of PMOS (M_{P1} and M_{P2}) and the pull-down current of NMOS (M_{N1} and M_{N2}), the output signals SW_N of negative level shifters are requested to either fully conducted or completely cut off the bypass switches (M_N). When SW_N is connected to VH_N which is a positive potential (equal to V_{DDH}), M_N would be fully turned on. Charges transfer through the bypass switch (M_N). When SW_N is tied to VL_N which is a negative potential, M_N would be turned off. Moreover, a clock controller is commanded by the digital signal C_N. C_N controls whether the clock signal of the whole system is able to deliver into the charge pump cell or not. When the charge pump stage is bypassed by the S_N signal, the clock controller disconnects the clock to save some energy by C_N signal. To be brief, S_N determines the operating mode of the selected N^{th} stage along with C_N whether to pump up or bypass away VL_N.

B. Operative Mechanism

Because of the similar composition in each stage, the operation is introduced in Fig. 3(b) and Fig. 3(c). In order to pump up the voltage in Fig. 3(b), the stage control signal (S_N) would go low to turn off the bypass path. Then, the clock control signal (C_N) would go high to pass the clock signal into the core circuit. Thus, the output voltage at VL_N can be pumped to a more negative value with the system frequency. The charge path is diverted from the N^{th} bypass switch into the negative charge pump cell. In short, a low S_N and a high C_N declare that the selected N^{th} stage is operating in the pump mode. On the contrary, S_N would be pulled high when entering the bypass mode as shown in Fig. 3(c). A high S_N conducts the selected bypass switch and makes the excessive voltage at VL_N bypassed away. Meanwhile, C_N would be pulled low to shut off the corresponding clock controller, and further stop the clock toggling in the N^{th} four-phase clock generator. Hence, the core charge pump circuit is ceased and no longer deliver charges. The charge transfer path is substituted by the bypass switch. A higher value (i.e. less negative) at VL_N may be achieved with less energy loss due to the short circuit of M_N.

The closed-loop negative voltage generator with the stage-selective is presented in Fig. 5. Since the bypass switch is connected between the first input terminal (V_{IN}, 0 V) and the N^{th} output terminal (VL_N), there is an order to pump or bypass the charge pump stages from which direction. For pumping, the power stage which is nearer the output terminal has the priority to be activated (i.e. pump 1^{st}-, 2^{nd}-, 3^{rd}-, and 4^{th}-stage in order). But for bypassing, it begins from the one nearer the input terminal to disable the power stage (i.e. bypass 4^{th}-, 3^{rd}-, 2^{nd}-, and 1^{st}- stage in order). The arrangement makes the proposed scheme not only flexible but also reconfigurable.

A four-stage composition is adopted in Fig. 5. The negative charge pump cells are successively jointed. The proposed circuit is replicated and connected to the cells accordingly. Charges are sent from the input terminal (V_{IN}) and stored in the output capacitor (C_{O1}) at the output terminal (VL_1). In general, the input voltage at V_{IN} is 0 V as well as the ground. For example, the negative voltage generator is set to a four-stage configuration initially. Yet, the composition is expected to cut down by half for energy conservation. To prevent unknown conditions and residual charges, the fourth and the third power stages are bypassed in sequence. By conducting M_4 and turning off CLK_4, VL_4 would be released to the input voltage level (V_{IN}, 0 V). And then the similar progress is repeated in the third stage. A fully conducted M_3 gives the input 0 V to VL_3. Clock signals are no longer coupled into the charge pump cell thanks to an open CLK_3. VL_3 is discharged gradually as well as VL_1. Lastly, only the second and the first stages are available so that charges are delivered to VL_1 with a two-stage configuration of the negative voltage generator. The charge transfer path is changed from path A to path B and finally path C, as annotated in Fig. 5. Somehow a lower output voltage (more negative) is needed

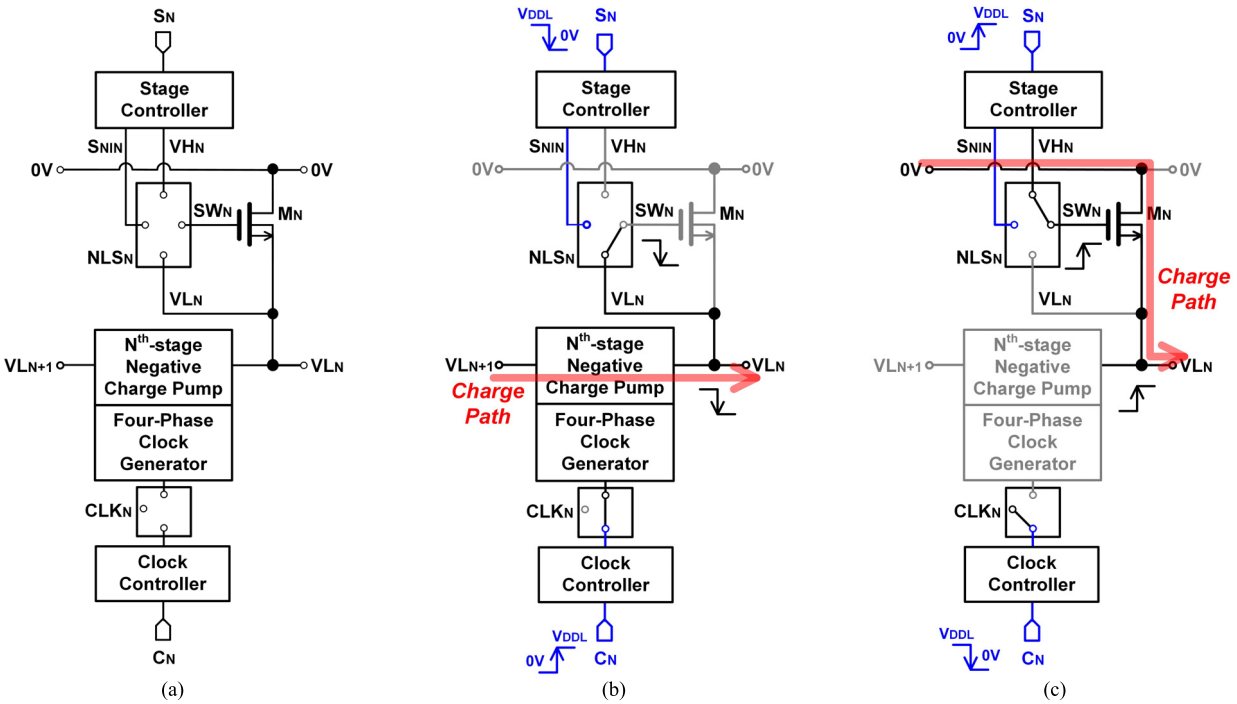


Fig. 3. (a) The unit structure of the proposed stage-selective circuit in the N^{th} stage. The operation of each selected stage with corresponding control signals. (b) In the pump mode, S_N is low but C_N is high; thus, the N^{th}-stage negative charge pump becomes the primary charge transfer path. (c) In the bypass mode, S_N turns high and C_N turns low so that charges directly pass through the N^{th}-stage bypass switch (M_N).

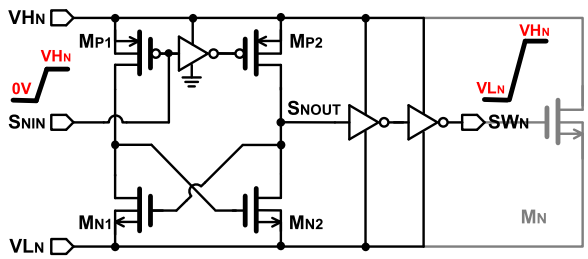


Fig. 4. The detailed circuit schematic of the negative level shifter (NLS).

at VL_1. Therefore, the negative voltage generator returns to the four-stage configuration by means of enabling the third and the fourth stages. To boost a more negative voltage, it is necessary to cut off the bypass path, which is created by M_3 and M_4. The entire closed-loop system would attempt to regulate VL_1 by toggling clock signals. In this event, CLK_3 and CLK_4 are short to transfer clocks into four-phase clock generators. A more negative output voltage is produced at VL_1 in the end. The charge transfer path is changed from path C to path B and finally path A, as annotated in Fig. 5.

When the loop is locked at a certain output level, more than one configuration might be able to achieve this scenario. If excessive power stages and clock generators are activated to meet the specification, too many charges would be redistributed. And further, more energy is dissipated. In contrast, the lack of activated stages and clock generators may induce overclocking, thereby the more switching loss getting worse. Thus, a competent configuration can perform better efficiency and stability with exact power stages and clocks. Depending on the conversion ratio, the power loss of the pumping stage can be optimized by the proposed circuit. The output voltage at VL_1 can provide the desired value with less power loss.

C. Circuit Implementation

In Fig. 5, the affiliated circuits comprise the voltage divider, the reference bias circuit, the error amplifier, the voltage control oscillator (VCO), positive level shifters, the four-phase clock generator, and the four-stage charge pump. For more details, a resistive digital-to-analog converter (RDAC) is a reference bias circuit in binary-weighted R-2R networks. The generated voltage (V_{REF}) of RDAC is controlled by five-bit signals $R_{[1:5]}$. According to the reference voltage (V_{REF}) and the resistive divider, the output of the charge pump loop would be locked at a target voltage level (V_{TG}). Whether the cascaded configuration or the output current is, the proposed stage - selective negative charge pump is seen as a self-regulated closed-loop unit with pulse frequency modulation (PFM) feedback control. It is notable that the error amplifier is designed with a wide bandwidth to trace the desired output target. Considered to a quick start-up and numerous output loading conditions, the oscillation frequency of the VCO should cover from several MHz to tens of MHz. In addition, a four-phase cross-couple structure is adopted as the core circuit of the negative charge pump cell [27]. The specific connection and the four-phase sequence of the charge pump cell are presented in Fig. 6. This topology is free from overstress issues because only $1\times V_{DDH}$ is delivered in each cascaded stage. For the reason that the power domain of the four-phase clock generator is V_{DDH}, the clock edges would only couple the toggling signals

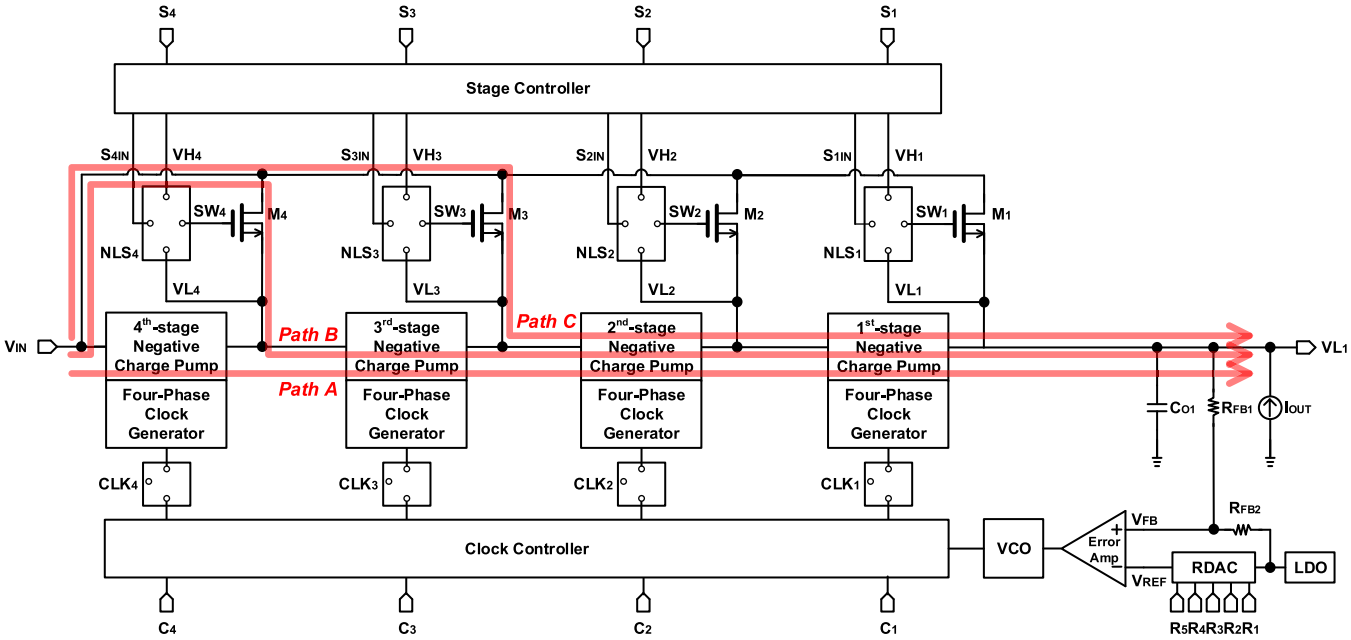


Fig. 5. The block diagram of the proposed stage-selective negative voltage generator.

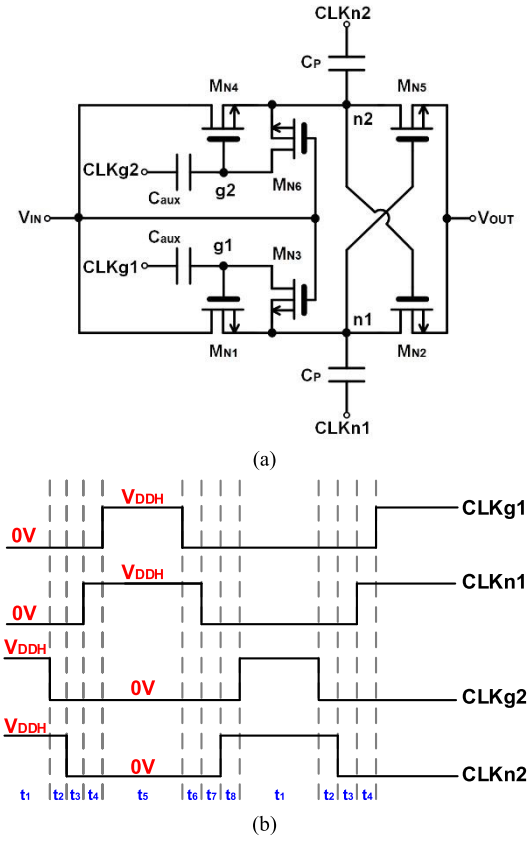


Fig. 6. (a) The circuit schematic and (b) the corresponding four-phase clocking waveforms of the negative charge pump cell.

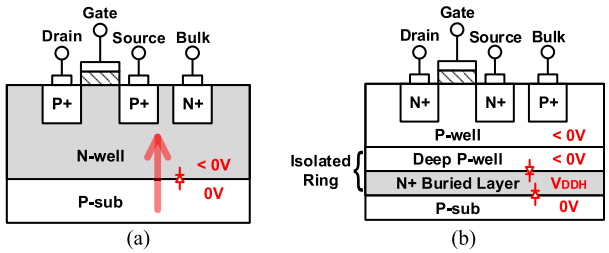


Fig. 7. The cross-section view of (a) PMOS forbidden to implement in the negative voltage domain and (b) NMOS with an isolated ring used in the negative charge pump cell.

with $1\times V_{DDH}$. Overstress concerns in charge pump cells are eliminated. The four-phase operation releases the return-back leakage and reversion loss. By virtue of the biomedical SoC integration, the global P-substrate is tied to 0 V as a ground.

For the sake of operation in the negative voltage, PMOS is forbidden to implement in all negative voltage domains, unless high voltage devices. Otherwise, PMOS could result in the forward parasitic diode in Fig.7 (a). All the switches are implemented in NMOS with isolation. The isolated ring is provided in the process with a deep P-well and a N+ buried layer (NBL) ring. The source and bulk terminals are jointed to avoid body effect. All NMOS are immersed in negative voltage, and the bias potential of P-well bulk ring and deep P-well ring is also negative. But the NBL is biased at V_{DDH} which is the highest voltage in the entire system. All the parasitic PN-junctions are reverse biased to prevent junction leakage. In Fig. 7(b), it annotates the practical bias conditions and the cross-section view of a switch in one charge pump cell.

IV. Verifications and Discussions

The proposed negative voltage generator with stage- selective circuits verifies the design on area and efficiency maintenance. Furthermore, configuration diversity is improved by additional bypass switches. This work has been fabricated in a

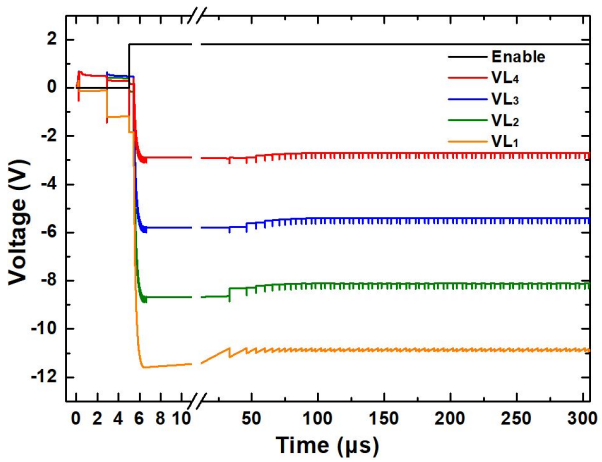


Fig. 8. The simulated results of the negative voltage generator to demonstrate its start-up and regulation.

TSMC 0.25-μm 2.5-V/5-V/12-V BCD process. In this process, the thick oxide in 12-V devices can tolerate the high voltage stress, yet the threshold voltage is high. Therefore, they are only adopted to NLS_N and M_N in the proposed stage-selective circuit. The maximum voltage difference in NLS_N and M_N is about 13 V in this work.

A. Simulation and Comparisons

For implantable biomedical applications, the impedance of electrodes and tissue varies with the size and position of the electrode. In neuron stimulation, the impedance value of the human brain is about 1 kΩ to 3 kΩ. The requisition of the power supply of stimulus drivers is widespread for either constant voltage or constant current stimulation. Thus, the stage- selective negative voltage generator is designed to output a wide voltage range within 5.5-mA output current. The output voltage (VL_1) is expected to regulate from –0.3 V to –9.3 V with the supplied voltages of 1.8 V (V_{DDL}) and 3 V (V_{DDH}). In this work, V_{DDL} is for analog circuits to minimize power. Yet V_{DDH} is for clock generators to couple the pumping capacitors. Aforementioned above, the analog type VCO gives around 100 MHz clocks to boost VL_1, so the quick start-up takes only 1 μs to reach the target voltage in Fig. 8. As long as the voltage is achieved, the clock frequency would slow down but still keep toggling to regulate by the PFM control.

Since the negative charge pump is implemented with four stages, the charge path can be reconfigured as zero-stage, one-stage, two-stage, three-stage, and four-stage in total. The zero-stage is for discharging and reset. Each configuration is born with its characteristic curves on power efficiency and output voltage. The simulated results under different loading conditions were explained in Fig. 9 (solid), including the minimum 0.5-mA and maximum 5.5-mA output current. The maximum voltage conversion is to couple $1\times V_{DDH}$ in each stage. When the voltage conversion ratio is between 60% and 80%, power losses are optimized to make the overall efficacy better. In other words, if the activated stages are appropriate for the output voltage levels, the power efficiency would be kept at a higher performance.

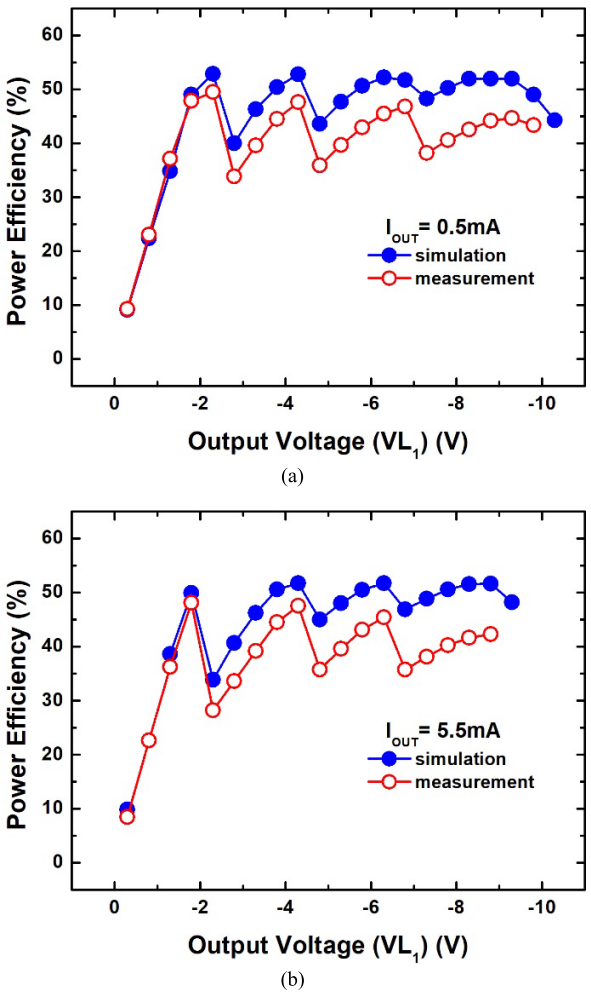


Fig. 9. The simulated and measured characteristics of the stage-selective negative voltage generator. (a) Under 0.5-mA output current (light load). (b) Under 5.5-mA output current (heavy load).

When the target level is loose, the major power loss is attributed to redistribution loss. Some of the delivered energy is dropped out so that the power efficiency is lower. However, when the target level is tight, the entire negative voltage generator is operated under a higher frequency. The power efficiency would drop dramatically as a result of the massive switching loss. Therefore, only a particular zone is preserved to achieve the expected efficiency without reconfigurable pumping schemes. Collecting the peak power efficiency of each configuration, the characteristic curves of this work are featured with the four successive hills. With stage selection, the simulated power efficiency is around 35% to 40% at valleys and roughly 50% at hilltops. As a result, the proposed negative voltage generator holds a better configuration and keeps a higher efficiency.

B. Silicon Verifications

The die microphotograph of the stage-selective negative voltage generator chip is shown in Fig. 10. Excluding I/O pads, the test chip occupies a silicon area of 2.25 mm^2. To further break down, 8% is occupied by the proposed stage-selection

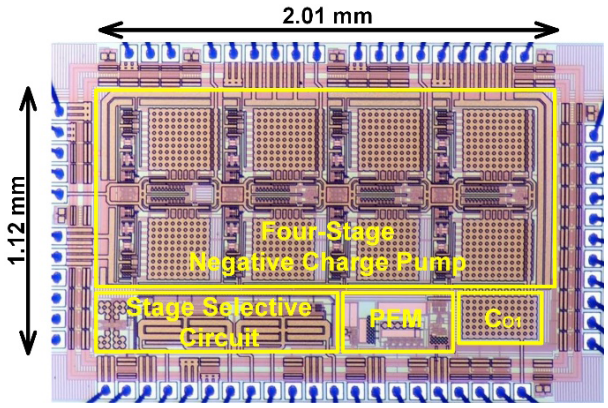
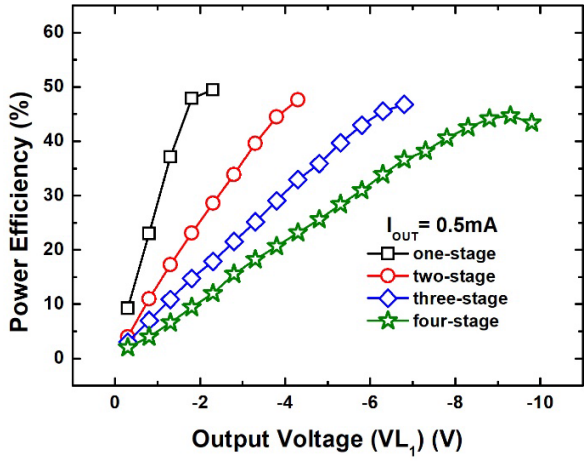
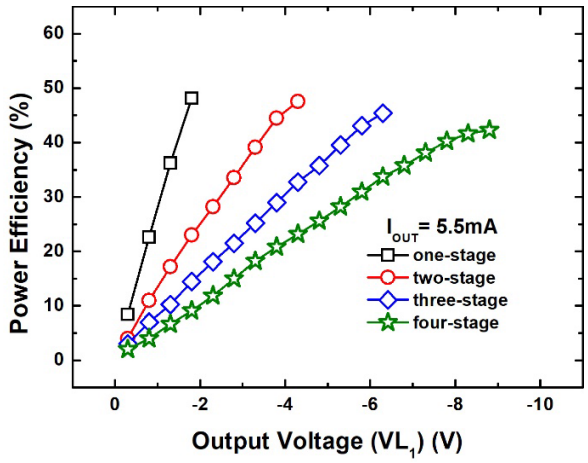


Fig. 10. Die microphotograph of the fabricated stage-selective negative voltage generator.



(a)



(b)

Fig. 11. The measured characteristics of the negative voltage generator with different cascaded configuration. (a) Under 0.5-mA output current (light load). (b) Under 5.5-mA output current (heavy load).

circuits, 87% is the power stages and all on-chip capacitors, and the rest 5% is the peripheral PFM circuits. For on-chip realization, all the capacitors are implemented with the metal-insulator-metal (MIM) capacitors. According to different purposes, capacitors are sorted into pumping capacitors (C_P), auxiliary capacitors (C_{aux}), and output capacitors (C_{OUT}). C_P is a fly capacitor of 100 pF so as to couple $1\times V_{DDH}$. C_{aux} which is sized to 2.5 pF only helps the main transistors for conduction. In addition, C_{OUT} at the output node (VL_1) is drawn with 125 pF to store charges and reduce output ripples.

As mentioned above, each configuration possesses its own characteristic curves on power efficiency and output voltage. The silicon measured results are presented in Fig. 11. When the configuration is fixed to certain stages, it can only vary output levels by adjusting V_{REF} and suffer low efficiency at less negative voltage cases. The major object is to combine those high efficiency parts in each configuration, and the four successive hills are gathered in Fig. 9 (hollow). The proposed circuit is verified to enhance the power conversion ratio around 40% to 55% with the assistant of the stage-selective circuit in measurements. Owing to the complex control sequence, digital codes are programmed into an external testing board and delivered to the internal test chip. Several control signals make the proposed negative voltage generator more flexible. The architecture is not fixed and the output is not constant, either. In this work, stage control signals ($S_{[1:4]}$) and clock control signals ($C_{[1:4]}$) are given to reconfigure the cascaded structure and clocks. In each configuration, reference control signals ($R_{[1:5]}$) further alter the regulated target voltage. Except the Enable signal is still manually controlled, other control signals come from digital control. As shown in Fig. 12(a), the fabricated chip is requested to alter VL_1 from –0.3 V to –9.3 V. The output impedance is 2 kΩ. In contrast, VL_1 in Fig. 12(b) is initially pumped to a negative high level and then stepped down. In a closed-loop system, the PFM feedback control technique is applied to regulate VL_1 at numerous levels. Under the optimized and activated stages, VL_1 is set with a resolution of –0.5 V. Whether it is operated in pump mode (Fig. 12(a)) or in bypass mode (Fig. 12(b)), the proposed circuit succeeds to expand the output voltage range and improves the low-efficiency issue. The variable technique is mainly for energy-efficient motivation, and the slight voltage shift avoids spikes from damages. Since VL_1 usually supports stimulators in biomedical SoC, increasing the supply of stimulators step by step performs a soft start-up. Decreasing the supply is to discharge and reset for thorough power-off. In Fig. 12 (c), the proposed stage-selective circuit is operated in order so that the configuration is transformed stage by stage. Under corresponding activated stages, VL_1 is locked at different objects. For instance, VL_1 is stabilized at –1.8 V with one stage validated, –3.3 V with two stages, –5.8 V with three stages, and –8.3 V with four stages. The measured results are recorded on waveforms. Moreover, it can also change the entire cascaded architecture arbitrarily. Despite the irregular transformation, the whole system is still able to settle on the target voltage. As depicted in Fig. 12(d), the configuration is varied out of order. Focusing on the transient state, VL_1 is able to regulate at a certain target voltage with the feedback control. The negative voltage generator is composed of a four-stage configuration, as a result, a stable –9.3-V output voltage is delivered under a 5.5-mA current loading, as demonstrated in Fig. 13(a). The internal nodes, including VL_2, VL_3, and VL_4, are also presented to explain the voltage

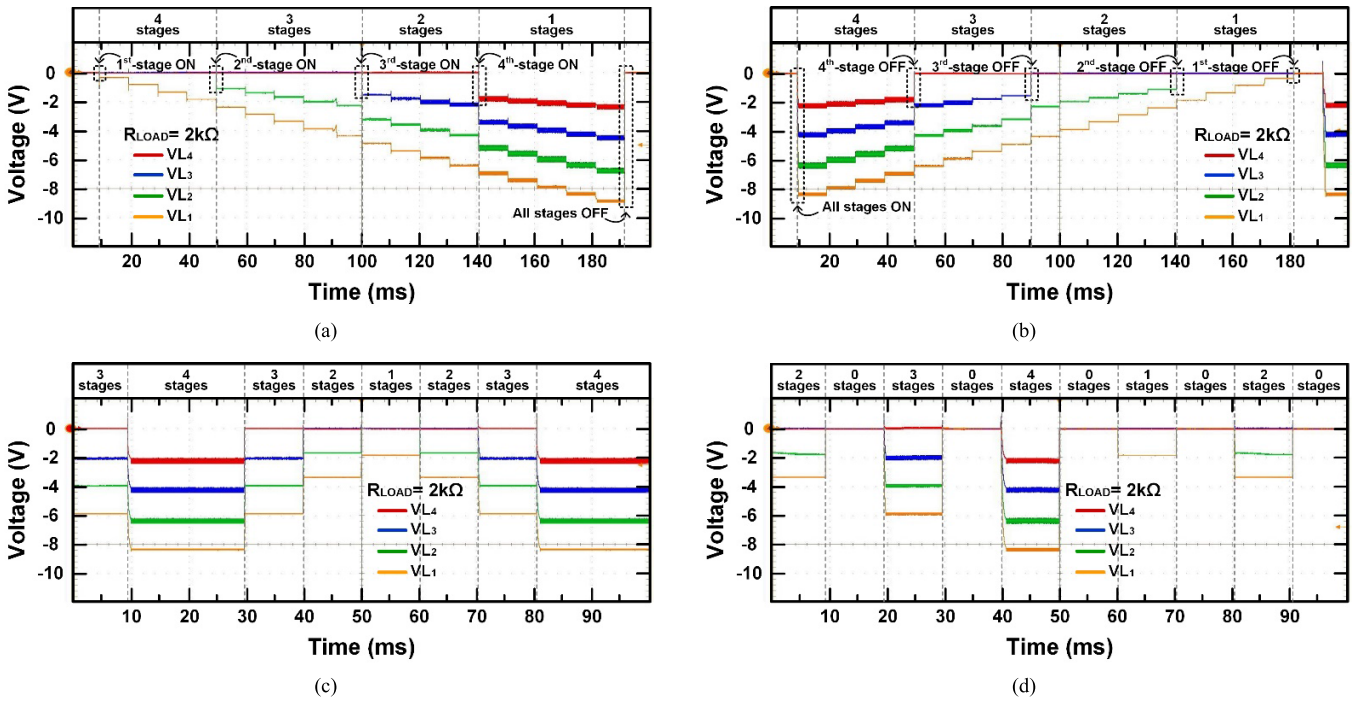


Fig. 12. The measured results of the stage-selective negative voltage generator operated (a) in the pump mode and (b) in the bypass mode. For special cases, the reference values and the activated stages of the stage-selective negative voltage generator are varied (c) in order and (d) out of order. All the measured events are verified with the output impedance of 2-kΩ (heavy load).

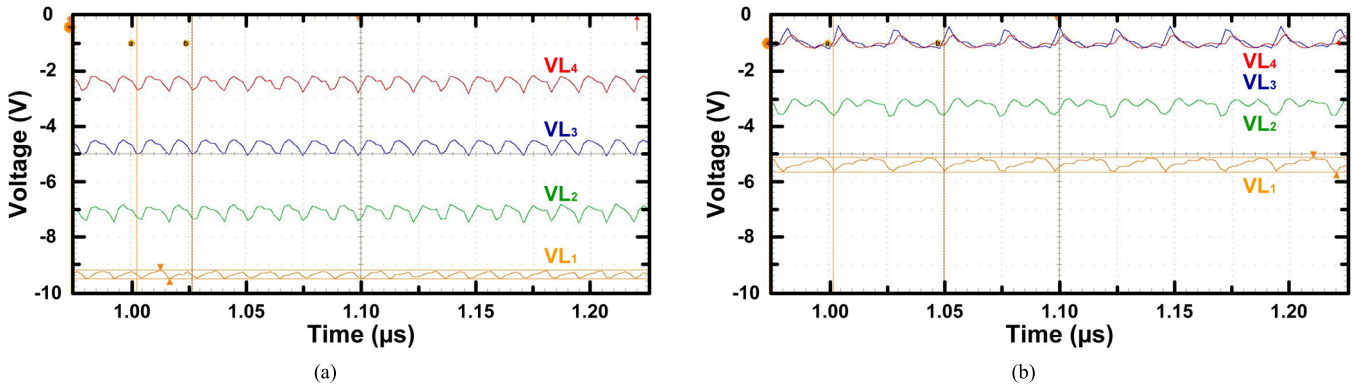


Fig. 13. (a) The measured results of the stage-selective negative voltage generator at –9.3-V output voltage and 5.5-mA loading current by a four-stage configuration. (b) The measured results of the stage-selective negative voltage generator at –4.3-V output voltage and 3.5-mA loading current by a two-stage configuration.

conversion ratio in each stage. In addition, it can also provide a –4.3-V output voltage and a 3.5-mA current loading with a two-stage configuration in Fig. 13(b). Since the third and the fourth stages are bypassed, VL_4 and VL_3 are short to the input terminal as well as 0 V. Under different loading conditions, the functions and performances are verified in silicon chips.

Based on these measured results, specifications of the fabricated stage-selective negative voltage generator are summarized in Table I and compared to other previous works. On the basis of negative voltage, this work takes advantage of a wide output voltage range and a large output current loading. With stage selection, an extensive voltage range and efficient power conversion have been accomplished and verified. The entire performance is flexible rather than fixed output or fixed charge transfer scheme. The new proposal of the variable output scheme can be realized in the negative voltage. From the perspective of a reconfigurable negative voltage generator, the overall power efficiency is optimized and enhanced. The proposed stage-selection circuit profits from making a proper voltage conversion for each power stage.

C. Discussion

Since input current is consumed consistent with activated pumping stages and clocks, it is important to dispose of redundant pumping blocks. In other words, it may easily suffer low-efficiency issues without stage selection when the activated stages and clocks are not fit for the output voltage levels. On the contrary, stage selection is able to maintain higher power efficiency under different output voltage levels. The greatest originality in this work is to realize the stage-selective circuit in the negative voltage domain. Since P-substrate is connected to 0 V for integration, the usage

TABLE I
PERFORMANCE COMPARISON WITH RELATED PRIOR WORKS

	Y.-C. Huang [12] (BioCAS '12)	I. Williams [23] (TBioCAS '13)	J. Gak [24] (LASCAS '13)	J.-H. Tsai [28] (JSSC '15)	A. Rashidi [29] (LSC '18)	Z. Luo [25] (TCAS I '19)	A. Ptal [22] (VLSID '20)	This work
Technology	0.18-µm CMOS	0.18-µm HV CMOS	0.6-µm HV CMOS	0.18-µm CMOS	0.18-µm CMOS	0.18-µm CMOS	0.18-µm BCD	0.25-µm BCD
Supplied Voltage	1.8 V	6 V	1.6~5.5 V	1 V	1.8 V	3.3 V	1.8 V	3 V
Output Voltage	–8.04 V	3~12 V (3 V/step)	0.5~16 V (0.5 V/step)	3~6 V	3.48 V –1.69 V* –3.38 V* –5.05 V*	3.3~12.6 V	7.5~24 V (1.2 V/step)	–0.3~–9.3 V (–0.5 V/step)
Output Current	–0.32 mA	N/A	N/A	0.24 mA	±0.1 mA	0.5~3.5 mA	0.1 mA	–0.5~–5.5 mA
Per Flying Capacitance	25 pF (on-chip)	150 pF (on-chip)	220 nF (off-chip)	N/A (on-chip)	23 pF (on-chip)	50 pF (on-chip)	N/A (on-chip)	100 pF (on-chip)
Area (I/O pads)	1.27 mm^2 (w/)	2.8 mm^2 (w/o)	1.7 mm^2 (w/o)	0.5 mm^2 (w/o)	0.5 mm^2 (w/)	2.87 mm^2 (w/)	0.32 mm^2 (w/o)	2.25 mm^2 (w/o)
Peak Efficiency	42.26%	~ 80%	73~79%	52%	POS:92.8% NEG:86.8% (simulated)	~ 70%	~ 49%	52%
Activated Stages	6× (fixed)	1× (variable)	1× and 2× (variable)	4× and 6× (variable)	3× (fixed)	3× (variable)	15× (fixed)	0× to 4× (variable)
Variable Output Technique	NO	SC network	SC network + Battery	Hybrid Topology	NO	Paralleled Bypass Switches	Adjusted V_{REF}	Grounded Bypass Switches

* The three negative voltages come from the internal and output nodes in a 3-stage negative charge pump.

of PMOS is limited. Not only the charge pump cell circuit is carefully designed with the isolated NMOS. But also the bypass switches are implemented by the high voltage NMOS. However, due to the high threshold, the less utility of high voltage devices on charge transfer path is better. Therefore, the grounded bypass switches are adopted to in this work. The most obvious efficiency difference occurs at –2.3-V output voltage. According to Fig. 11, the one-stage configuration is worthwhile to support output loading with 35% efficiency improvement against the four-stage configuration. Moreover, the proposed stage-selection circuit only takes only 8% augmentation on the area. It is obvious that the negative voltage generator with less activated amounts of stages has a higher efficacy during operation. A better performance is achieved by maintaining the voltage conversion ratio in each stage between 60% and 80%. However, it decays as the activated numbers of stages increase. An amendment on power loss is verified and noteworthy. In summary, VL_1 can regulate at –9.3 V under the 5.5-mA heaviest loading. The PFM feedback mechanism in coordination with stage selection push the effective output range to a widespread use.

V. CONCLUSION

For biomedical treatments, the output and the supplied voltages of stimulators vary from several volts to tens of volts. To provide a larger output range, size and efficiency are the limiting factors for the charge pump with a stationary architecture. A stage-selective negative voltage generator system has been proposed and realized by using the optimized serial stages to reduce excessive power consumption. The fabricated chip has been verified in a 0.25-μm BCD process. It generates a plurality of output voltage levels from –0.3 V to –9.3 V while the output loading current covers from 0.5 mA to 5.5 mA. It is an energy-efficient power source so that the power conversion efficiency is held at 50% roughly. With the addition of the stage-selective circuit, a compact area is achieved due to the distinct reconfiguration. Since the cascaded configuration is flexible and programmable, the entire architecture can be arbitrarily controlled by the parameterized digital codes.

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