Using Schottky Barrier Diode to Improve Latch-Up Immunity for CMOS ICs Operating With Negative Voltage Sources

Rong-Kun Chang and Ming-Dou Ker, *Fellow, IEEE*

***Abstract*— For some applications, the CMOS ICs need to be supplied with positive and negative voltage sources for the desired circuit operations. To supply the negative voltage source for circuit operations in the silicon chip with the common p-type substrate grounded, the isolation rings configured with n-well (NW) and deep n-well (DNW) layers must be used to isolate the circuits of nMOS devices operating with negative voltage from the common P-substrate. Such NW/DNW isolation rings in the circuit layouts are often connected to ground (GND = 0V) for the circuit operations with negative voltage source. But, a parasitic p-n-p-n path from I/O pMOS to this grounded NW/DNW isolation ring may cause the circuits at high risk to latch-up. In this letter, a novel method to improve latch-up immunity against such parasitic p-n-p-n path by using a Schottky junction is reported.**

***Index Terms*— Latch-up, silicon-controlled rectifier (SCR), Schottky junction, Schottky barrier diode (SBD), negative voltage supply, deep n-well (DNW).**

I. Introduction

THE implantable biomedical devices with neuro-modulation function via electrical stimulation are widely used to treat neuro disorders. The stimulation methods can be divided into the voltage mode and the current mode, as well as the electrode configuration for neuro-stimulation includes the mono-polar and the bi-polar styles. Typically, the mono-polar configuration required two high voltage power supplies ($\pm V_{CC}$) to realize the biphasic stimulation [1].

According to the requirement of high reliability for the implantable biomedical devices, on-chip ESD protection circuits must be equipped into the CMOS ICs to avoid the malfunctions caused by ESD stresses [2]. For the high operation voltage, the high-voltage-tolerant ESD protection circuits for the positive voltage supply pin [3] and the negative voltage supply pin [4] had been developed, respectively. In [4], the stacked-nMOS (STnMOS) was used to build the ESD protection circuit for negative power pin, which was isolated from the common P-substrate by the n-well (NW) and deep n-well (DNW) biased at ground (GND = 0V). To supply the negative voltage source ($-V_{CC}$) for stimulator circuit operations, the isolation rings configured with n-well (NW) and deep n-well (DNW) layers were used to isolate the circuits of nMOS devices operating with negative voltage from the common P-substrate. Such NW/DNW isolation rings in stimulator circuits, those providing negative stimulation currents/voltages under power supply between GND and $-V_{CC}$, are often connected to the relatively high potential bias of GND (0V). However, some non-typical latch-up paths may occur to cause unrecoverable failures [5], such as the parasitic silicon-controlled rectifier (SCR) structure between I/O pMOS and the grounded NW/DNW ring in the neuro-simulation circuits supplied with negative voltage sources. Due to the low holding voltage (V_h) of such parasitic SCR structure with DNW layer, the CMOS ICs to provide mono-polar bi-phasic stimulation may suffer high risk of latch-up issues.

The Schottky barrier diode (SBD) [6] is a kind of single-pole and multiple carrier device which works through the metal semiconductor contact barrier. According to the characteristic of the SBD device shown in Fig. 1, the Schottky barrier junction is suitable for embedding into the parasitic p-n-p-n path to increase its holding voltage (V_h) against the latch-up issue. The Schottky barrier junction was ever reported to enhance the latch-up immunity of power ICs fabricated in a high-voltage BCD technology [7], [8].

In this work, the latch-up path between PMOS and grounded NW/DNW was studied and investigated in silicon chip with different test structures. In order to investigate the characteristic of latch-up path, the dc curve tracer (Tek370B) is used to verify the holding voltage (V_h) of each latch-up test structure. The embedded Schottky barrier junction can effectively increase the V_h of the parasitic SCR structure to highly improve its latch-up immunity.

II. Test Structures

The Type-A test structure of the latch-up path between V_{DD}-biased PMOS and grounded NW/DNW is shown in Fig. 2(a) with its cross-sectional view. In the test structure, the poly

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The authors are with the Institute of Electronics, National Chiao Tung University at Guangfu, Hsinchu 300, Taiwan (e-mail: mdker@ieee.org).

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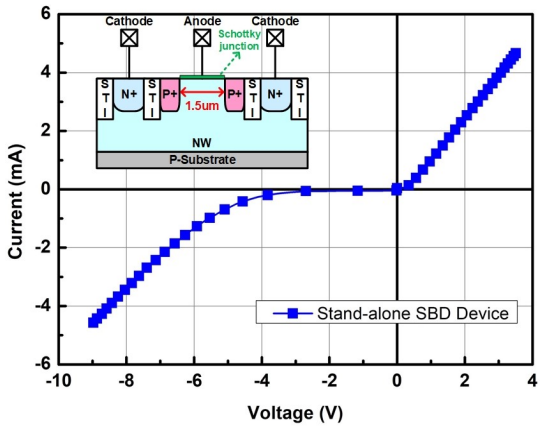

Fig. 1. The measured dc *I-V* characteristic of the stand-alone SBD device, which was fabricated in a 0.18-μm 1.8-V/3.3-V CMOS process.

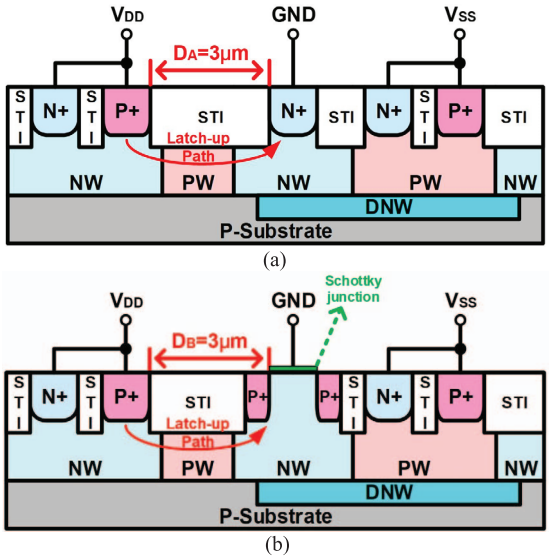

Fig. 2. The cross-sectional views of (a) Type-A, and (b) the proposed Type-B, test structures for the pMOS-to-grounded NW/DNW latch-up path.

gates of pMOS and nMOS were removed, only the P+ and N+ diffusions are left to represent the source and bulk terminals where connected to V_{DD} or V_{SS}, respectively. Among, the N+ and P+ diffusions which connected to V_{SS} of negative voltage supply are isolated from the common P-substrate by NW and DNW biased at GND (0V). The anode-to-cathode spacing of the parasitic latch-up path from V_{DD} to GND (D_A) is drawn as 3 μm in the Type-A test structure.

To increase the holding voltage (V_h) of the parasitic SCR structure, the Type-B test structure with embedded Schottky junction was proposed in this work, as the cross-sectional view shown in Fig. 2(b). Different from Type-A test structure, the isolation NW/DNW ring of Type-B test structure is connected to GND pad by the Schottky junction. This Schottky junction is one of standard devices provided by foundry in a 0.18-μm 1.8-V/3.3-V CMOS process, and neither additional process step nor additional mask layer is needed. In addition, the distance of anode-to-cathode spacing ($D_B = 3\mu$m) is kept the same as that in the Type-A test structure. The P+

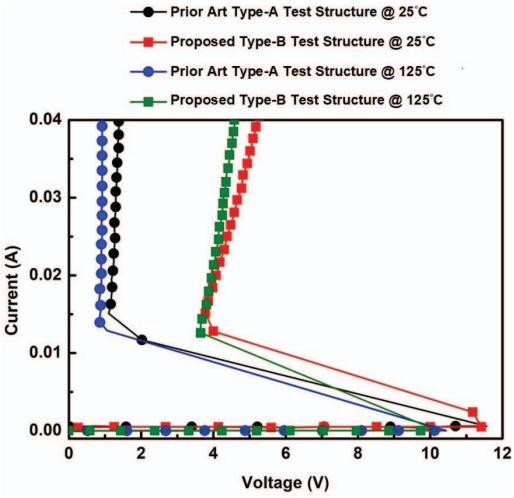

Fig. 3. The measured dc *I-V* characteristics of the parasitic latch-up paths in Type-A and Type-B test structures from V_{DD} to GND at 25 °C and 125 °C, respectively.

diffusion beside the Schottky junction in Fig. 2(b) is the guard ring structure of the SBD device, which is used to reduce its leakage current and to enhance breakdown voltage [9]. The doping concentration of the guard ring structure in the SBD device is the same as that of an ordinary P+ implant.

III. Experimental Results

A. DC I-V Characteristics

The test structures have been fabricated in a 0.18-μm 1.8-V/3.3-V CMOS process. The dc *I-V* characteristics of the test structures are measured (from V_{DD} node to GND node with the anode-to-cathode spacing of 3μm) by a curve tracer (Tek370B) at room temperature of 25 °C, and the results are shown in Fig. 3. The measured results of all test structures showed the obvious snapback phenomenon to clamp the voltage down. By comparing the measurement results between Type-A and Type-B test structures, the holding voltage (V_h) of the parasitic latch-up path has been increased from 1.10 V to 3.94 V by the embedded Schottky junction. Since the V_h of the Type-B test structure can be greater than V_{DD} (3.3 V), the latch-up occurrence can be avoided by the embedded Schottky junction. When the temperature rises to 125°C, the V_h values of Type-A and Type-B test structures are 0.86 V and 3.65 V, respectively. Since the V_h value of the Type-B test structure is still higher than V_{DD}(3.3 V), the risk of latch-up occurrence can also be avoided under a high-temperature situation. To further increase the V_h value, it can be achieved by extending the anode-to-cathode spacing (D_B) of the structure.

B. Latch-Up Test

To examine the latch-up immunity, the test method with positive and negative current tests (I-tests) had been already defined in the Joint Electron Device Engineering Council (JEDEC) standards. The measurement setup of JEDEC latch-up current trigger test is shown in Fig. 4(a). The P+ diffusion inside the n-well of the device under test (DUT) is connected to V_{DD} of 3.3 V to simulate a

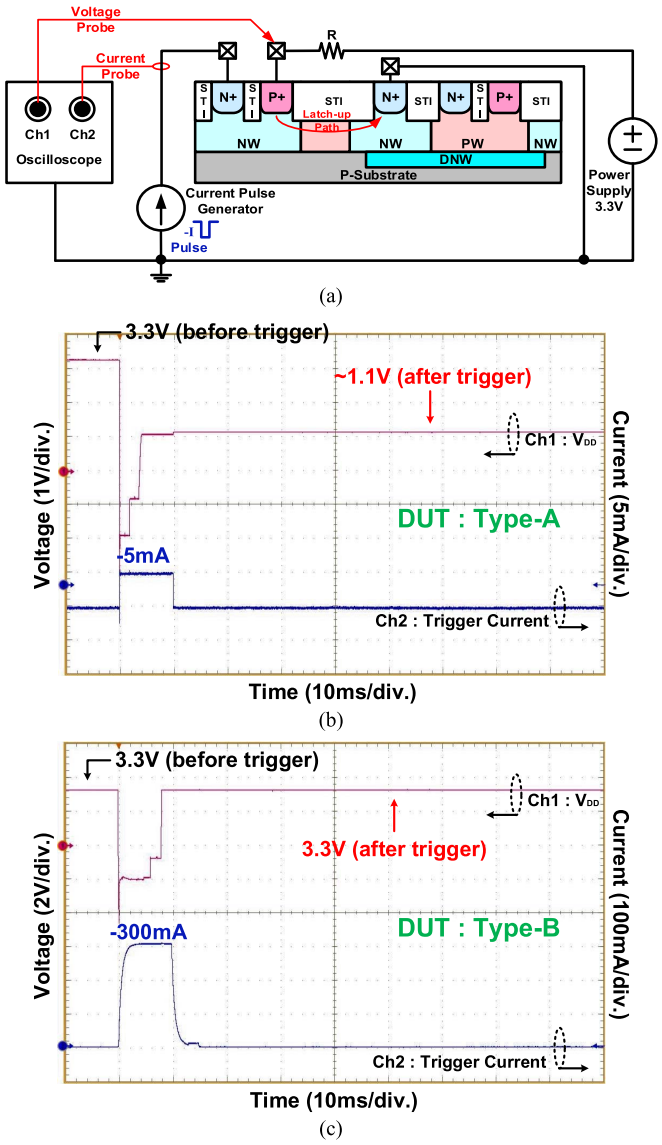

Fig. 4. (a) Latch-up measurement on the test structure with the negative current pulse applied to the N+ pickup of pMOS. Measured waveforms of (b) Type-A, and (c) Type-B, test structures under the I-test negative currents of −5-mA and −300-mA, respectively.

pMOS source, and the NW/DNW isolation ring is connected to ground (0V). A negative current pulse is applied to the N+ diffusion in the NW to generate the trigger current into the p-substrate. The current and voltage waveforms on the DUT are monitored simultaneously by the oscilloscope. After the I-test transient triggering, if the DUT was driven into a latch-up state, the voltage level at V_{DD} node will be clamped down. Thus, the latch-up event can be judged by monitoring the voltage waveform on the V_{DD} pin, when a negative trigger current with a pulse width of 10 ms is injected to the N+ in n-well.

Figs. 4(b) and 4(c) show the measured waveforms on the Type-A and Type-B test structures under latch-up negative I-test current of −5 mA and −300 mA, respectively. The parasitic latch-up path of the Type-A test structure was triggered on by the trigger current of −5 mA, as the voltage at V_{DD} is clamped down to ∼1.1 V. On the other hand, the V_{DD} voltage on the Type-B test structure is still kept at 3.3 V after the latch-up I-test of −300 mA, as shown in Fig. 4(c). From the experimental results, the Schottky junction can significantly improve latch-up immunity of the Type-B structure by increasing the holding voltage of the parasitic p-n-p-n path, but without increasing its anode-to-cathode spacing in layout.

IV. Conclusion

The latch-up issue between pMOS and the grounded NW/DNW isolation ring has been investigated in a 0.18-μm 1.8-V/3.3-V CMOS process. By using the Schottky junction to connect the NW/DNW isolation ring, the holding voltage of the parasitic p-n-p-n path can be increased greater than V_{DD}, and the latch-up immunity can be significantly improved. The Schottky junction can be directly embedded in the NW/DNW isolation ring without increasing the anode-to-cathode spacing of the parasitic p-n-p-n path in layout. The realization of Schottky junction is fully process-compatible to standard CMOS process with the fabrication supported by foundry. The Schottky junction embedded in the DNW structure is a good solution for latch-up prevention in CMOS ICs with negative voltage supply.

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