Stacking-MOS Protection Design for Interface Circuits Against Cross-Domain CDM ESD Stresses

Cheng-Yun Hsueh and Ming-Dou Ker, *Fellow, IEEE*

***Abstract*— Electrostatic discharge (ESD) is still a challenging reliability issue for integrated circuits (ICs) in advanced CMOS technology. With the development of ICs toward system-on-chip (SoC) applications, it has been common to integrate multiple separated power domains into a single chip for power management or noise isolation considerations. Besides, the fabricated transistors with thinner gate oxide for high-speed operation cause the ICs more sensitive to charged-device model (CDM) ESD events, especially under cross-domain stresses. The traditional cross-domain CDM ESD protection would result in some restrictions on circuit applications or cause some performance degradation. Thus, a new protection design with stacking footer/header metal-oxide-semiconductor (MOS) structure against cross-domain CDM ESD stresses was proposed in this work and verified in 0.18-μm CMOS technology. The proposed design got higher ESD robustness under CDM and HBM (human body model) ESD tests. Moreover, the CDM robustness of different stacking-MOS protection designs was also investigated in detail.**

***Index Terms*— Charged-device model (CDM), cross-domain ESD protection, electrostatic discharge (ESD) protection, multiple power domains, stacking metal-oxide-semiconductor (MOS) structure.**

I. Introduction

WHILE the CMOS technologies scaled-down, the charged-device model electrostatic discharge (CDM ESD) issue has become more critical because of the thinner gate oxide in larger chip size. With the continuous development of integrated circuits (ICs) in the direction of system-on-chip (SoC) applications, multiple independent power domains in an IC are requested by different circuit blocks, such as mixed-voltage, mixed-signal, and power management applications [1]. The supply voltage of core circuits was often reduced to save power consumption, while others may still require the separated power domains for circuit performance and noise isolation, especially for analog/RF circuits with higher noise sensitivity and SNR requirements.

Unfortunately, the interface circuits between the separated power domains are very sensitive to ESD events. Some efforts had been developed to avoid ESD damages at the cross-domain interface circuits [1]–[10]. During ESD stress across separated power domains, the whole-chip ESD protection can be established with the assistance of power-rail ESD clamp circuits and bidirectional diodes to conduct ESD currents away from the interface circuits between different domains. However, closer to the actual situation, the bidirectional diodes were only connected between the separated VSS power lines. Apart from this, some additional local ESD clamps were placed nearby the interface circuits to further reduce overstress voltages during ESD stresses [1]–[10]. Although some solutions were ever made, the cross-domain ESD stress is still a challenging issue in recent years.

With concerns of CDM ESD protection, the cross-domain interface is the most vulnerable situation. The CDM charges are mostly accumulated in the common p-substrate when the IC is initially floating, which would be discharged through the VDD/VSS metal buses from the internal circuit blocks during CDM ESD events to cause gate-oxide damages at the interface circuits between the separated power domains. To further prevent this kind of CDM damage, a new protection design with stacking footer/header metal-oxide-semiconductor (MOS) structure against cross-domain CDM ESD stresses was proposed and verified in this work.

II. Internal ESD Threats Under Cross-Power-Domain ESD Stresses

Fig. 1 illustrates an ESD protection scheme of an IC product with multiple separated power domains. Generally, whole-chip ESD protection consists of an I/O ESD protection circuit for each domain, power-rail ESD clamp circuits between VDD and VSS rails, and bidirectional diodes between VSS rails of different domains.

The input ESD protection is used against pad-to-VDD and pad-to-VSS ESD stresses at the input pad, and it consists of gate-grounded NMOS (M_{ni}), gate-VDD PMOS (M_{pi}), and

Manuscript received December 11, 2020; revised January 28, 2021 and February 17, 2021; accepted February 18, 2021. Date of publication March 8, 2021; date of current version March 24, 2021. This work was supported in part by the Center for Neuromodulation Medical Electronics Systems from The Featured Areas Research Center Program within the framework of the Higher Education Sprout Project by the Ministry of Education (MOE), Taiwan and in part by the Ministry of Science and Technology (MOST), Taiwan, under Contract 109-2221-E-009-100-MY3 and Contract 110-2622-8-009-017-TP1. The review of this article was arranged by Editor C. Duvvury. *(Corresponding author: Ming-Dou Ker.)*

The authors are with the Institute of Electronics, National Chiao Tung University, Hsinchu 300, Taiwan (e-mail: mdker@ieee.org).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TED.2021.3061325.

Digital Object Identifier 10.1109/TED.2021.3061325

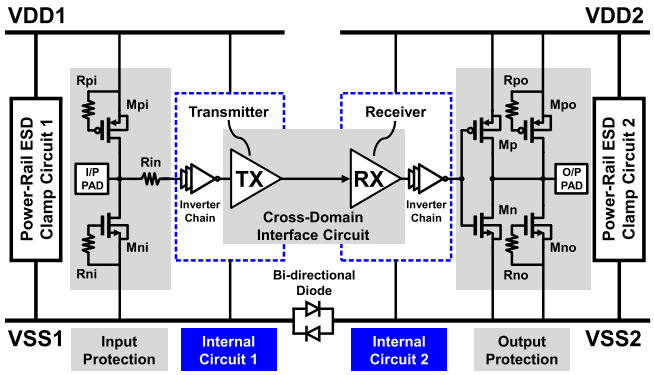


Fig. 1. Simplified circuit diagram of an IC with separated power domains.

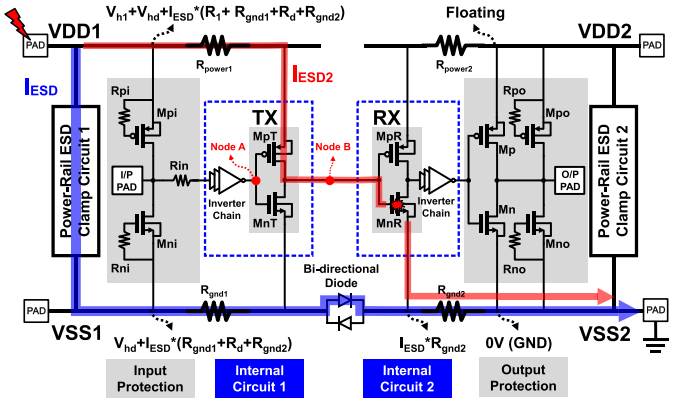


Fig. 2. Simplified circuit diagram of an IC with separated power domains under a cross-domain ESD event and the failure mode.

R_{in}. The output protection is used for pad-to-VDD and pad-to-VSS ESD protection at the output pad, and the driving strength of the output buffer is determined according to the external load, signal operation frequency, and distortion tolerance. Also, by connecting different finger numbers of M_p and M_n to get the appropriate driving current and achieve signal specifications, the other fingers are connected as M_{no} and M_{po}. The power-rail ESD clamp circuit, which consists of an *RC*-based ESD transient detection circuit and a substrate-triggered field-oxide device (STFOD) [11], is the main ESD device. Both internal circuits 1 and 2 are set as digital circuit blocks between separate power domains. To ensure the driving capability, the inverter chains, as a tapered buffer, were inserted between I/O ESD protection and the interface circuit. A pair of inverters are set as the transmitter (TX) and the receiver (RX) to represent the interface circuit that transfers signals from the circuit in VDD1/VSS1 domain to VDD2/VSS2 domain.

However, the interface circuits are often damaged under cross-domain ESD stresses even with full-chip ESD protection [1]–[10]. In fact, in a fast transient ESD event, the ESD current may find another unexpected path across the domain-crossing circuits before the power-rail ESD clamp bypass the ESD current to the VSS rail. As shown in Fig. 2, when the ESD zaps across different power domains, for example, positive ESD stress applied on VDD1 and grounded VSS2, and the ESD current could be discharged from VDD1 to VSS1 by power-rail ESD clamp circuit 1 in VDD1/VSS1 domain, and then from VSS1 to VSS2 through the bidirectional diode to the VSS2. $V_{\text{h1}}/V_{\text{hd}}$, and R_1/R_d are the holding voltage and the turn-on resistance of power-rail ESD clamp circuit 1/bidirectional diode, respectively. The parasitic resistances of power and ground buses, which are labeled as R_{power} and R_{gnd}, are essential in long discharge paths and normally depend on the complexity of the circuit layout. The actual resistances must be extracted from the physical layout and substituted into circuit models for simulation or analysis in circuit-level design.

In tradition, the purpose of the power-rail ESD clamp circuit in each domain is to dissipate the ESD current to the VSS rail during a cross-domain ESD event. But, the long current dissipation path I_{ESD1} may induce a large voltage drop between separate power domains. Since the voltage of node A is initially floating, the voltage of node B can be raised to near VDD1 by unexpected path I_{ESD2} through the ON-state transmitter's PMOS transistor (M_{pT}) to charge parasitic capacitance in the receiver side, and the largest voltage drop will be across the gate oxide of the receiver's NMOS transistor (M_{nR}).

CDM events can be applied to the same explanation since the charges are stored in the common *p*-substrate and connected to the VSS rail. However, the surrounding ESD protection circuit is unable to turn on efficiently because of extremely short rise time and duration time. Significantly, under CDM stress with peak currents reaching 5 A or more for large packages, the core transistors of the interface circuit will suffer from voltage overstress and become more critical in advanced process technology.

Even if there are many failure analysis (FA) procedures, such ESD failures across the domain-crossing circuits are usually difficult to examine and modify [1]. Therefore, many EDA tools with related simulation algorithms are currently being developed, such as the CDMi and PERC, to assist IC designers in simulating and analyzing the failure point of cross-domain circuits around the whole chip, and then insert necessary local protection to the corresponding location. However, this kind of simulation methodology still requires lots of experimental databases to achieve higher accuracy. Therefore, improving the ESD robustness of the cross-domain interface circuit is the most straightforward solution.

III. CDM ESD Protection Designs for Cross-Power-Domain Interface Circuits

A. Traditional CDM ESD Protection Design

To prevent this kind of cross-domain CDM damage, the typical second ESD protection design [2] is shown in Fig. 3. The protection design network consists of a series resistor, a pair of gate-ground NMOS (M_{nESD}), and gate-VDD PMOS (M_{pESD}). In general, M_{nESD} and M_{pESD} are added between the signal line and the VSS/VDD rail, respectively. Both transistors are turned off during normal operation since |vgs| is not high enough to invert the conduction channel. When the ESD event occurs, the collector-base junction of the parasitic NPN/PNP BJT becomes reverse biased to the critical electric field and then induces punchthrough breakdown or even avalanche breakdown. As the current flows from the base to the ground

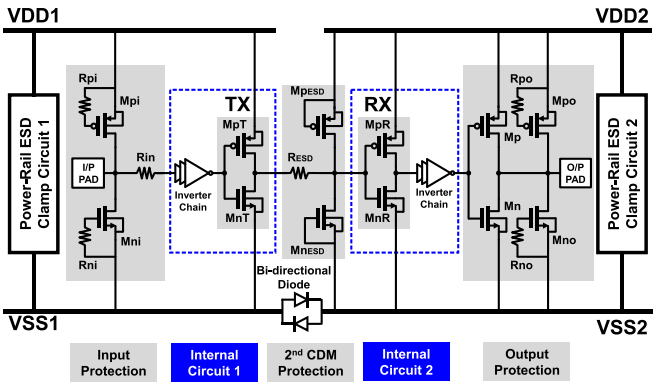


Fig. 3. Simplified circuit diagram to show the second ESD protection design for an IC with separated power domains against a cross-domain CDM ESD event.

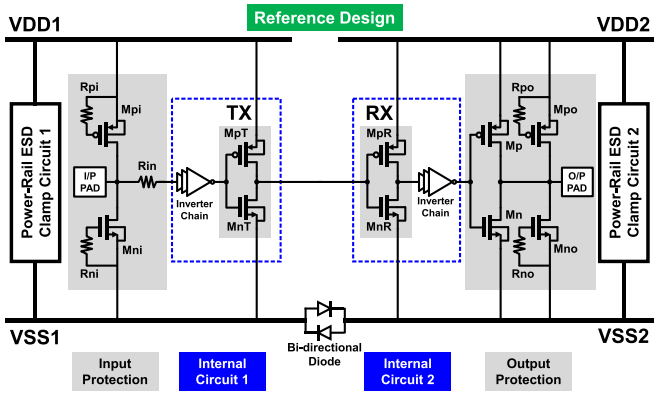


Fig. 4. Cross-domain circuit was fabricated under a 0.18-μm 1.8-V CMOS process, set as the reference design.

through the parasitic resistor, a potential difference will be established across the base–emitter junction, turning on the parasitic NPN BJT and dissipating ESD current.

Unfortunately, the traditional design has some drawbacks. The implementation of R_{esd}, $M_{nESD,}$ and M_{pESD} will occupy additional areas and contribute propagation delay time to the signal transmission. Furthermore, high voltage to low voltage (HV-to-LV) interfaces and power-down mode applications are not available because of the mistriggering of the parasitic diode under normal circuit operation.

B. New Proposed CDM ESD Protection Designs

To build a multidomain IC, a cross-domain circuit, set as the reference design, as shown in Fig. 4, is implemented under a 0.18-μm 1.8-V CMOS process. This circuit includes power-rail ESD clamp circuits, I/O ESD protection circuits for each domain, bidirectional diodes between the separated VSS, and two inverters as the interface circuit. The parameters of all the transistors are listed in Table I. Both the transmitter and receiver modules use the inverter cell, provided by the 0.18-μm standard cell library, with a specific driving capability. Choosing a larger size inverter on the TX side can promote unexpected discharge paths across the interface circuit and the smallest size inverter on the RX side as a worst case. And the gate potential rises more rapidly since its minimal parasitic capacitance.

Based on area cost and circuit performance considerations, the structure of the cross-domain interface circuit should be modified and optimized, and achieve higher cross-domain CDM ESD robustness. Figs. 5–7 show the new proposed Type-A, Type-B, and Type-C designs by modifying the interconnection of the receiver module with stacking MOS structure to have the same function as the reference design under normal operation, thus enhancing the equivalent impedance of the interface circuit under ESD event and suppressing the generation of unexpected discharge paths.

Fig. 5 illustrates a schematic from the previous work [9]–[10]; a receiver module consists of stacking header PMOS M_{pR2} and footer NMOS M_{nR2} directly connected to VSS2 and VDD2, respectively. Both are coupled with an inverter constituted of a PMOS transistor M_{pR1} and an NMOS transistor M_{nR1}. The gates of M_{pR1} and M_{nR1} are tied together which are connected to the signal line, while the drains of M_{pR1} and M_{nR1} are tied together for providing an output signal to the next stage circuit, the inverter chain. In the digital circuit, a combinational logic in

TABLE I
DEVICE PARAMETERS OF THE INTERNAL CIRCUIT

Subcircuit	Device Parameter	Reference Design	Type-A to Type-C
Transmitter (TX)	MOS W/L (μm/μm)	M_{nT}=6/0.18 M_{pT}=8.22/0.18	M_{nT}=6/0.18 M_{pT}=8.22/0.18
Receiver (RX)	MOS W/L (μm/μm)	M_{pR}=0.685/0.18 M_{nR}=0.5/0.18	M_{nH}=M_{nL}=1/0.18 M_{pH}=M_{pL}=1.37/0.18 M_{nR1}=M_{nR2}=0.5/0.18 M_{pR1}=M_{pR2}=0.685/0.18
Input Protection	Resistor (Ω)	R_{in}=200 R_{pi}= R_{ni}=1k	R_{in}=200 R_{pi}= R_{ni}=1k
	MOS W/L (μm/μm)	M_{pi}=360/0.25 M_{ni}=360/0.5	M_{pi}=360/0.25 M_{ni}=360/0.5
Output Protection	Resistor (Ω)	R_{po}= Rno=1k	R_{po}= R_{no}=1k
	MOS W/L (μm/μm)	M_{p}=150/0.25 M_{n}=75/0.5 M_{po}=210/0.25 M_{no}=285/0.5	M_{p}=150/0.25 M_{n}=75/0.5 M_{po}=210/0.25 M_{no}=285/0.5
RC-Based Power-Rail ESD Clamp Circuit	Resistor (Ω)	R_{ESD}~95k	R_{ESD}~95k
	Capacitor (F)	C_{ESD}~2p	C_{ESD}~2p
	MOS W/L (μm/μm)	M_{pESD}=60/0.25 M_{nESD}=24/0.25	M_{pESD}=60/0.25 M_{nESD}=24/0.25
	STFOD Perimeter (μm)	STFOD=188	STFOD=188

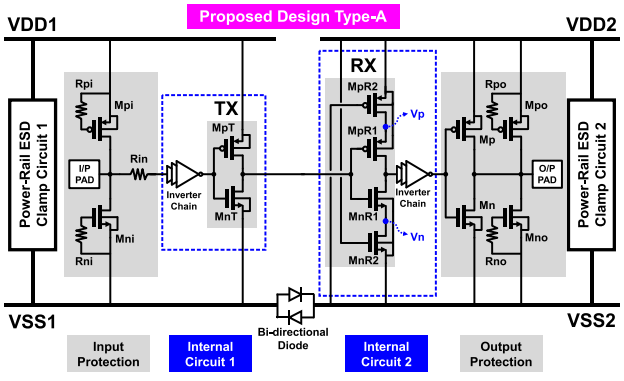


Fig. 5. Cross-domain circuits with a receiver module consist of stacking header PMOS and footer NMOS are proposed as Type-A design.

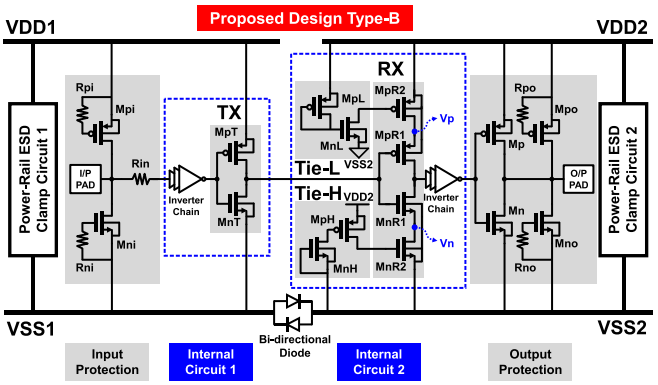


Fig. 6. Cross-domain circuits with a receiver module consist of stacking header PMOS and footer NMOS are proposed as Type-B design.

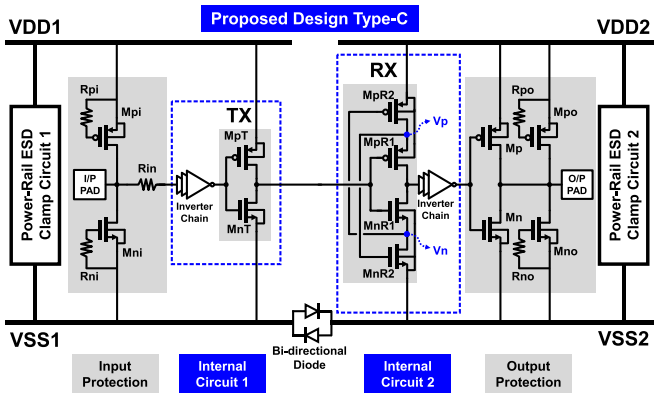


Fig. 7. Cross-domain circuits with a receiver module consist of stacking header PMOS and footer NMOS are proposed as Type-C design.

the form of stacking transistors needs sizing to achieve the same driving capability. However, during signal transmission, a potential difference between the source and body of M_{nR1} and M_{pR1} causes the body effect and degrades the switching speed.

The gate to the source overlapped junction must be protected first because of the lowest breakdown voltage [12]. When a cross-domain ESD event occurs as mentioned above, the large potential difference will cross between the gate of M_{nR1} and the source of M_{nR2}. The internal node V_n forms a floating node, and the total parasitic capacitance on the V_n forms a voltage divider. By modulating the sizes of M_{nR1} and M_{nR2}, the voltage coupled to the V_n node can be dynamically adjusted, which could alleviate the overvoltage of M_{nR1}. The PMOS side also adopts the same symmetrical structure as NMOS. Under the corresponding cross-domain ESD stress condition, a voltage divider is formed at the floating node V_p to relieve the overvoltage of M_{pR1}.

The most common failure mechanism in CDM ESD events is gate oxide breakdown. Since the metal bus is prone to accumulate CDM charges, tie circuits have become one of the solutions [13] but occupied more area. Fig. 6 illustrates a receiver module consists of stacking structures with a standard tie-low/high circuit. Tie circuits are used to avoid direct gate connection to the VDD/VSS bus, thereby protecting the cell from damage. In this case, $M_{\mathrm{nH}}/M_{\mathrm{pL}}$ acts as a diode-connected startup circuit, and then $M_{\mathrm{pH}}/M_{\mathrm{nL}}$ pull logic high/low as output to bias $M_{\mathrm{nR2}}/M_{\mathrm{pR2}}$ in fully ON-state, respectively.

Fig. 7 illustrates a receiver module consists of stacking structures connected to interstage node V_n and V_p, which form a symmetrical latch structure. The latch structure could eliminate the requirement for additional tie circuits. However, the latch structure needs to be carefully designed and used. Note that high-speed signals are rapidly switching during interface circuit communication, and noise interference, which may couple to V_n, V_p nodes, may occur, and then cause M_{nR2} and M_{pR2} to escape from the original logic state. If a high level of logic output is lower than VDD/2, the malfunction will happen in the poststages. And the frequency at this time is defined as the maximum frequency (f_{max}), which could be evaluated as a performance limit in terms of speed. In this experiment, the size of transistors in the latch structure has been well designed to ensure stable output for high-speed signals.

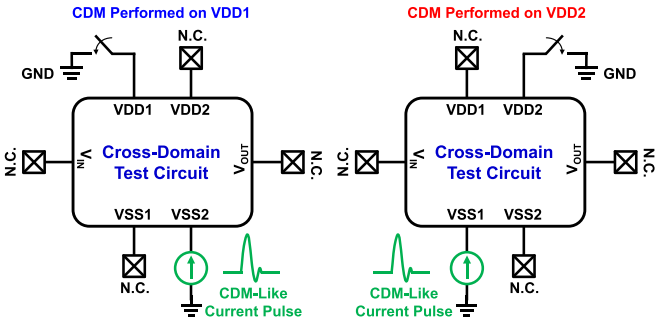


Fig. 8. CDM-like simulations have been performed on the VDD1/VDD2 from each power domain to simulate the cross-domain CDM events.

For the Type-B and Type-C designs, a voltage divider with the floating nodes V_p and V_n was formed to couple the instantaneous rising voltage during cross-domain ESD stress, thus increase the equivalent breakdown voltage of the receiver module. Furthermore, the gate connection of the stacking MOS via tie circuits prevents the CDM charges on the metal wire from breaking down the interface gate-oxide and ensures a better CDM ESD robustness under different conditions.

C. Predictive Cross-Domain Voltage Under CDM Simulation

In this subsection, the referring CDM simulation method [14]–[16] is simplified as a CDM-like current pulse injected from common p-substrate and grounded VDD pin to qualitatively analyze the cross-domain circuit. The simulation setup used for simplified CDM simulations is shown in Fig. 8. Note that, due to the absence of the HSPICE-model of ESD devices, the STFOD is replaced with a vertical NPN BJT, and the bidirectional diodes are replaced with an antiparallel P+/N-well diode for simulation.

The influence of different designs on CDM cross-domain voltage is discussed as well. Moreover, this approach can also analyze the CDM failure by applying the measured CDM current peak to the circuit to determine the failure location and find out the victim. CDM-like waveform simulations have been performed on the VDD1/VDD2 from each power domain

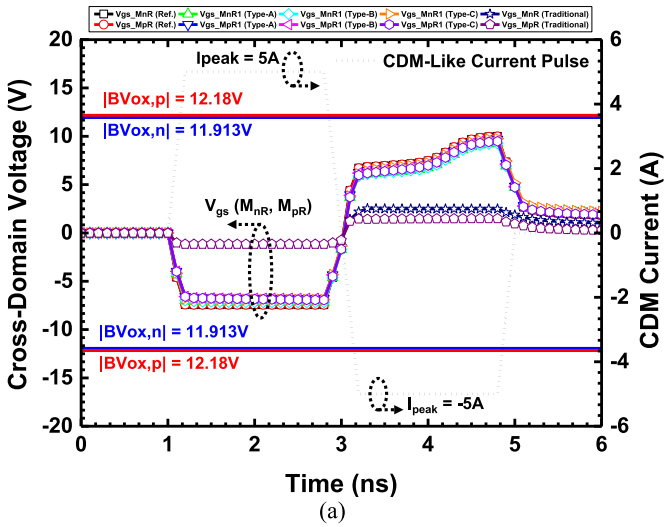


Fig. 9. Simulated cross-domain voltage waveforms, while positive and negative CDM was performed on the (a) VDD1 and (b) VDD2.

to monitor the cross-domain voltage, especially the receiver module. The CDM current peak is selected both positive and negative 5 A with 200-ps rise time to meet the small capacitance module in JEDEC standard [17] (see Fig. 9).

The simulated cross-domain voltage waveforms in Fig. 9(a) show that, while positive CDM was performed on the VDD1, the peak voltages V_{gs_MnR}/V_{gs_MnR1} across the receiver NMOS gate-oxide are lower than the measured gate-oxide breakdown voltage $|BV_{ox,n}|$, and the receiver PMOS has the same trend. Furthermore, while negative CDM was performed on the VDD1, all peak voltages across the gate-oxide of the receiver module are close to $|BV_{ox,n}|$ and $|BV_{ox,p}|$. By observing the transient overvoltage of cross-domain circuits, it could be confirmed that the receiver NMOS is more vulnerable under negative CDM conditions.

In addition, the simulated cross-domain voltage waveforms in Fig. 9(b) show that, while positive CDM was performed on the VDD2, V_{gs_MpR}/V_{gs_MpR1} are very close to $|BV_{ox,p}|$, but V_{gs_MnR}/V_{gs_MnR1} is lower than $|BV_{ox,n}|$. In contrast, while negative CDM was performed on the VDD2, a trend similar to positive period could be observed. The most of

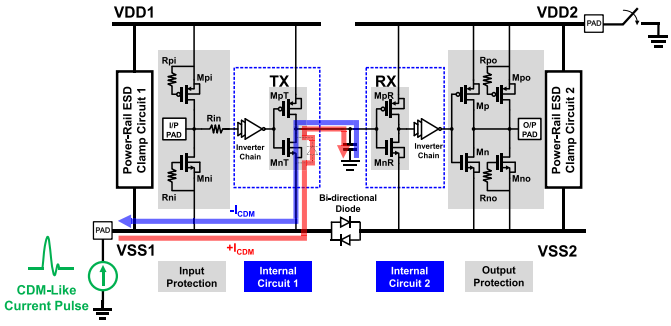


Fig. 10. Schematic illustration of parasitic current paths under CDM-like simulation was performed on VDD2 (grounded VDD2).

V_{gs_MpR}/V_{gs_MpR1} are much higher than $|BV_{ox,p}|$. As a result, the receiver PMOS is more vulnerable under negative CDM conditions. Thus, the VDD2 (−) stress could be predicted as the worst case for all designs. The victim devices were M_{pR} or M_{pR1}, where the FA in Section IV-D seems to support that as well. Although the stacking-MOS designs were adopted, the difference was slightly between the reference proposed Type-A, Type-B, and Type-C designs. The main reason for the poor performance of VDD2(-) is the invalidation of the stacking-MOS protection design. The header PMOS M_{pR2} will be turned on during the negative period, a perfect voltage divider cannot be formed at all.

Note that, compared with the reference design, the proposed Type-A, Type-B, and Type-C designs have a slight voltage-divided effect, thus relieve transient overstress during both positive and negative CDM stress periods. The traditional design (local clamp + series R) is introduced as a prior art but not implemented in the CDM test chip for measurement. Fortunately, the ESD performance could also be obtained through the predictive CDM-like simulation. The traditional design presents a good performance to overcome the transient overvoltage issues. However, the local clamp will conduct part of the CDM current and may burn out M_{nESD} or M_{PESD} before the gate-oxide breakdown of M_{nR}. Therefore, the actual CDM robustness cannot be guaranteed from existing results.

Overall, the transient overstresses of RX-PMOS (M_{pR}) are more critical than RX-NMOS (M_{nR}), while negative CDM is performed on the VDD2, because parasitic current paths of TX-NMOS (M_{nR}) were generated during the transient periods of rapid discharge. These paths can transport the positive or negative CDM charge, thereby raise or drop the local potential of the floating capacitor on the signal line, as shown in Fig. 10. In the end, the large potential drop across the interface circuit will destroy the gate-oxide of M_{pR} first with a lower CDM level.

D. Performance-Area Comparison

The functional simulation setup of cross-domain interface circuits is shown in Fig. 11, probing the rise time, fall time, and internal propagation delay time of RX. Moreover, the comparison between Types A, B, C, and the traditional design in terms of die area impact and performance impact has been provided and summarized in Table II. The newly proposed design can indeed obtain area advantages, especially

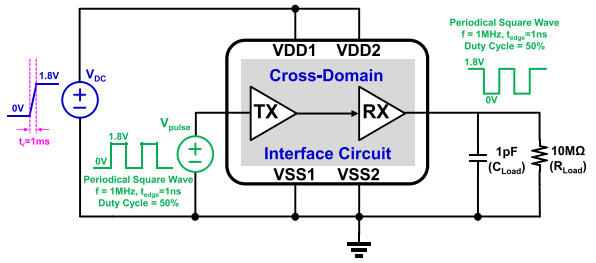


Fig. 11. Functional simulation setup of cross-domain interface circuits.

TABLE II
PERFORMANCE-AREA COMPARISON OF CROSS-DOMAIN CIRCUITS

Designs	Reference	Type-A	Type-B	Type-C	Traditional (Local Clamp + R) M_{nESD} = 10μ/0.18μ M_{pESD} = 10μ/0.18μ R = 200Ω
Cell Area [μm²]	6.59	9.58	22.17	9.86	49.08
Rise-Time (t_r) [ns]	0.105	0.107	0.107	0.107	0.144
Fall-Time (t_f) [ns]	0.109	0.112	0.112	0.112	0.142
Delay-Time (t_{DLH}) [ns]	5.451	10.44	10.44	10.44	5.474
Delay-Time (t_{DHL}) [ns]	3.117	4.91	4.91	4.91	3.209

A and C, but the speed will be limited by the stacking-MOS structure, which can be traded off by optimizing the size of the transistor. Although the traditional design occupies more area, the difference in terms of speed is relatively small.

IV. Experimental Results and Failure Analysis

The reference design and the new proposed designs with different structures and interconnections of the receiver module embedded in the domain-crossing circuit have been fabricated in a 0.18-μm 1.8-V CMOS process. The zoomed-in illustration of layout top view and optical microscope (OM) micrograph of CDM test chip is shown in Fig. 12. The aforementioned cross-domain test circuits with Type A, B, and C designs are on the same die/IC and assembled in the side-braze 48 pins ceramic package for CDM ESD test. For each test circuit, the input–output protection was embedded in the I/O pad, and the power-rail ESD clamp circuit was embedded in the VDD pad. In this experiment, the I/O pads and VDD pads were abutted together, and ground rails (VSS) of the same power domain were connected to a common ground to save the layout area. Until ESD tests were finished, the failure criterion depends on electrical verification and functional verification to judge the specific I/O pin of the device under test (DUT) is passed or failed. By the verification results, comparisons of the ESD robustness under different architectures are provided as follows.

A. Electrical Verification

Since the ESD discharge mechanism of CDM and HBM is quite different, causing internal damage is quite complicated. The electrical verification will be through the I–V characteristic of all combinations between any two VDD/VSS pins. Preliminarily observe the leakage of various paths, and trace the components that may be damaged in the interface circuit, which is helpful for FA, subsequently.

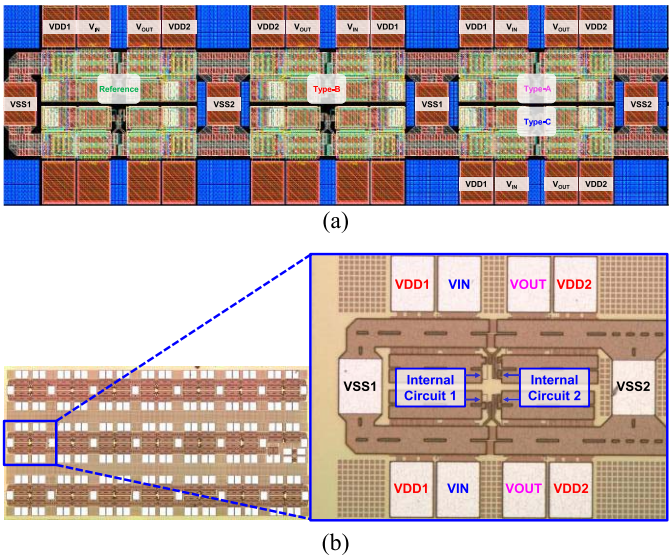


Fig. 12. Zoomed-in illustration of (a) layout top view and (b) OM micrograph of CDM test chip.

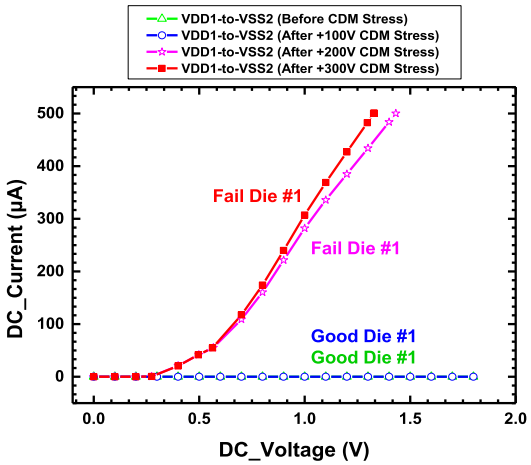


Fig. 13. Traced dc I–V characteristics from VDD1 to VDD2 of the reference design before and after ESD stress.

For electrical verification, the failure criterion is defined as the leakage current under 1.8-V bias increases over ten times of magnitude from its original leakage current, or the I–V characteristics shifting more than 30% from its initial curve after each ESD stress level. For example, the traced dc I–V characteristics of the reference design before and after ESD stress are shown in Fig. 13. Each of the dc I–V curves was measured by B2902A Precision Source/Measure Unit (PSMU), respectively. After the positive CDM 200- and 300-V stress, the dc I–V characteristics between VDD1 and VDD2 shifted obviously, and the leakage current increased significantly by more than ten times under 1.8-V bias.

B. Functional Verification

With an odd number of inverter stages, the circuit is used to invert the input signal. To confirm the circuit function, the proposed designs was verified by observing the output signal integrity. B2902A PSMU is used to force the VDD1 and

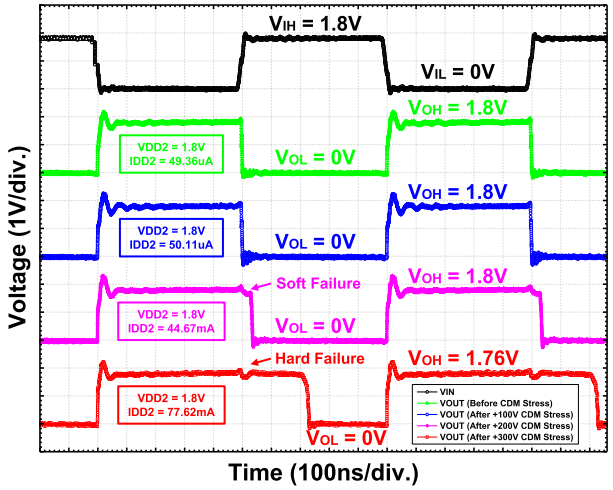


Fig. 14. Measured voltage waveforms of the reference design cross-domain circuit before and after CDM ESD stresses.

VDD2 at 1.8 V, while the VSS1 and VSS2 are both grounded. 33210A Waveform/Function Generator is connected to the input pad, generating a 1-MHz periodic square waveform as the clock signal. The input and the output waveform are captured by the MDO3054 Mixed Domain Oscilloscope. For example, the measurement results of the reference design before and after CDM ESD stress are shown in Fig. 14, respectively. Since the interface circuits are vulnerable under cross-domain ESD stresses, the measured waveforms show distortions and degradations after ESD damage.

C. CDM and HBM Robustness

The cross-domain CDM ESD test is done by pointing the pogo pin on VDD1 (as VDD1-to-VSS2 stress) or VDD2 (as VDD2-to-VSS1 stress). Both positive and negative polarity stress are done for two discharge directions, are shown in Fig. 15(a) and (b), respectively. The CDM ESD test step voltage is 100 V, and the failure criterion is defined as one of the electrical or function verification results out of specifications.

The CDM test was performed on the fabricated silicon chip with different protection designs (Type A ∼ C), which assembled in a Side-Braze 48 pins package. The discharge current was measured by a high bandwidth digital oscilloscope. The measured CDM discharge current waveforms and peak currents for different CDM measurements from +/−100 to +/−500 V are shown in Fig. 16. Due to the different test-key locations and the charge distribution inside the whole chip, the peak current and rise time of each pin under test (PUT) would be slightly different.

All measured results of the proposed design after CDM ESD stress are listed in Table III. As expected, the reference design as a baseline shows the worst CDM ESD robustness, about 100-V CDM level under three conditions. Conversely, the Type-A design shows better CDM performance, despite local VDD/VSS is directly connected to the gate. Similarly, the Type-B and Type-C designs adopt tie circuits that can maintain better CDM ESD robustness under different conditions.

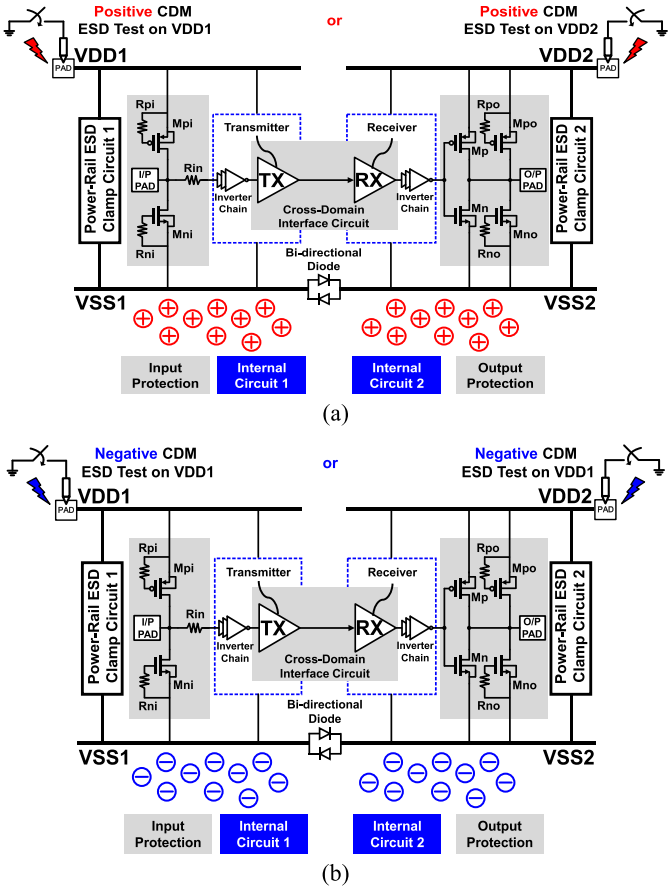


Fig. 15. Schematic diagrams of (a) positive CDM ESD stress, and (b) negative CDM ESD stress, for cross-domain CDM ESD test.

TABLE III
CDM ROBUSTNESS FOR DIFFERENT DISCHARGE PINS AND THE FIELD PLATE CHARGED POLARITY

Designs	Reference	Type-A	Type-B	Type-C
VDD1 (+)	100V	>500V	400V	>500V
VDD1 (-)	200V	400V	400V	400V
VDD2 (+)	100V	>500V	400V	300V
VDD2 (-)	100V	200V	200V	300V

When compared with Type-B and C, Type-A performs better for the VDD2 (+) stress. Since the stacking footer PMOS (M_{pR2}) in design Type-B or Type-C was turned off as high impedance while the potential of VSS2 was high enough. So that, a perfect voltage divider was formed on the floating node V_p, and the CDM-like simulation results seem to support that. According to this reason, the gate of M_{pR2} was directly connected to VSS2 in Type-A design, but Type-B and Type-C designs were not. As known, this may cause different impedance characteristics of OFF-state M_{pR2}. Hence, Type-A design will gain better high impedance characteristic of OFF-state M_{pR2} from interconnections, thereby obtaining better CDM robustness under VDD2 (+) stress.

Note that the VDD2 (−) stress condition is the worst case with the lowest withstand voltage among all designs, because the discharge path of power-rail ESD clamp circuit 2 was not designed well for fast transient ESD events (VF-TLP or CDM). Hence, the ESD path with nonuniform conduction will induce snapback breakdown and high R_{on} of STFOD. Eventually, the VDD2 potential will be raised up to force the receiver PMOS gate-oxide breakdown earlier.

As a result, the simulation results in Fig. 9 only support us to predict that RX-NMOS (M_{nR} or M_{nR1})/RX-PMOS (M_{pR} or M_{pR1}) is the victim, while negative CDM is performed on the VDD1/VDD2. But the difference was slightly between the proposed Type A, B, and C. However, in the experimental results, Type-C has been shown to perform better for VDD2(−) stress. The root cause is the different interconnections from VSS2 to the gate of M_{pR2}. It could be explained as M_{pR2} would be unequally turned on via different paths for each design. During VDD2 (−) stress, the turned-on M_{pR2} would cause V_p raised to near VDD2 potential. For Type-C design, the gate of M_{pR2} is connected to VSS2 through the M_{nR2}, smaller than M_{nL}, and the latch structure also needs enough regeneration time to stably turned M_{pR2} on.

The disconnect between CDM-like simulation and experimental results could be explained by two reasons: First, due to the absence of the HSPICE-model of ESD devices, the actual current flow during CDM events may not be represented and modeled correctly. And the existing devices, used to replace ESD devices, may have some impacts on predictive capabilities. Second, the simulation setup seems to be too simple, and most parasitic effects are ignored in the existing pre-layout simulation. Thus, the parasitic junction capacitances of internal node V_n/V_p have not been accurately estimated, resulting in the internal node V_n/V_p not being maintained at a perfect floating state during the CDM-like simulation.

However, the new proposed designs have a higher CDM robustness, which means that under different directional stress combinations, stacking structures of the receiver module can reduce cross-domain transient overvoltage.

Finally, the cross-domain HBM ESD test is also done by applying a positive HBM pulse at VDD1 (or VDD2) with grounded VSS2 (or VSS1). All measured results are listed in Table IV. Consider the situation when the I/O ESD protection design does not completely dissipate the HBM ESD energy. As a result, the proposed designs have better robustness compared with the reference design under the VDD1-to-VSS2 condition. Furthermore, the behavior different from CDM under the VDD2-to-VSS1 condition since the longer rise and duration time of HBM improves the transient overvoltage issue. Likewise, the stacking MOS architecture is suitable for the I/O ESD protection to increase the breakdown voltage.

D. Failure Analysis (FA) and Discussion

The InfraRed Optical Beam Induced Resistance Change (IR-OBIRCH) is used as the electrical FA tool in this experiment to locate the failure point. By scanning and heating through the surface of voltage-applied IC with an IR-laser, the position with impedance variation different from other regions has a higher probability to be considered as the abnormal failure point. Note that the green hot spot indicates that the impedance increases, and the leakage decreases; otherwise, the red hot spot indicates that the impedance decreases, and the leakage increases.

As shown in Fig. 17(a) and (b), the reference/Type-B designs with 1.8-V bias on each power domain, the failure points were detected and located at the receiver module after the −300/−500-V CDM test on VDD1. Dc voltage and current are marked, revealed that the Type-B design has the same failure point but slight damage under higher CDM stress.

According to the IR-OBIRCH failure spot locations mentioned above, the physical FA procedures such as de-layer and Scanning Electron Microscope (SEM) will be further performed on CDM test chip. By inspecting the contact anomalies and poly profile by Passive Voltage Contrast (PVC) SEM and High Acceleration Voltage (HKV) SEM, respectively,

TABLE IV
HBM ROBUSTNESS FOR DIFFERENT DISCHARGE PINS

Designs	Reference	Type-A	Type-B	Type-C
VDD1 to VSS2	0.9 kV	1.5 kV	1.75 kV	1.5 kV
VDD2 to VSS1	1.75 kV	1.75 kV	2 kV	1.75 kV

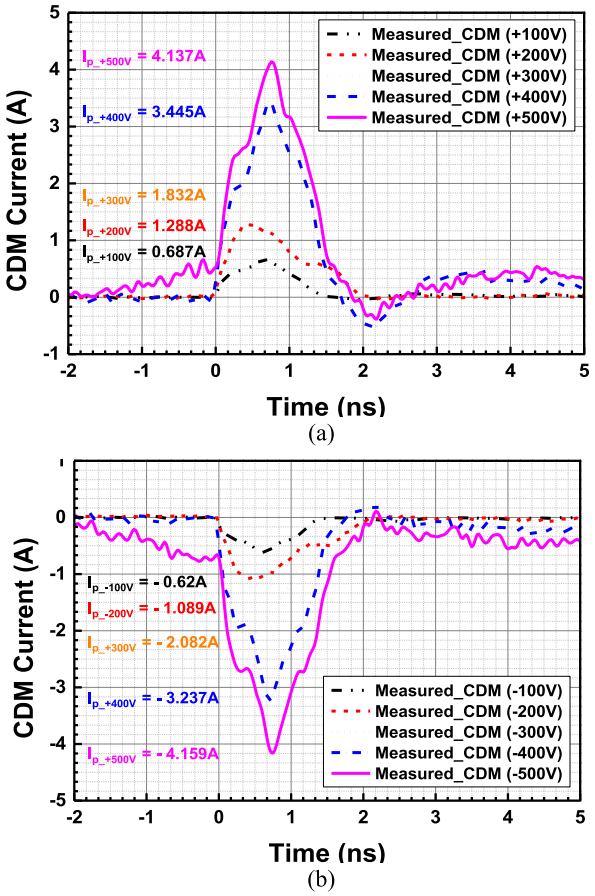
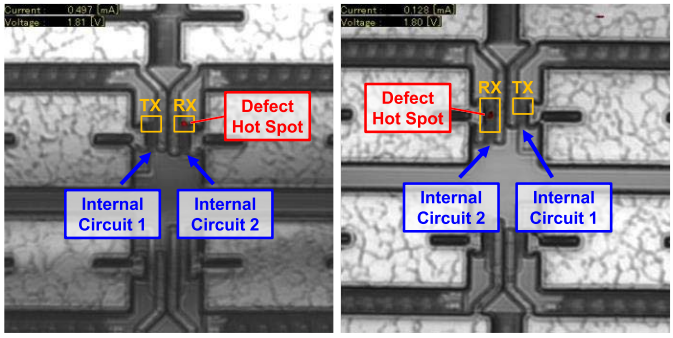


Fig. 16. Measured CDM discharge current waveforms and peak values for CDM stresses from (a) +100 to +500 V and (b) −100 to −500 V, respectively, where the silicon chip was assembled in a Side-Braze 48 pins package.



(a) (b)

Fig. 17. IR-OBIRCH failure spots of (a) reference design and (b) Type-B design, after −300/−500-V CDM test on VDD1, respectively.

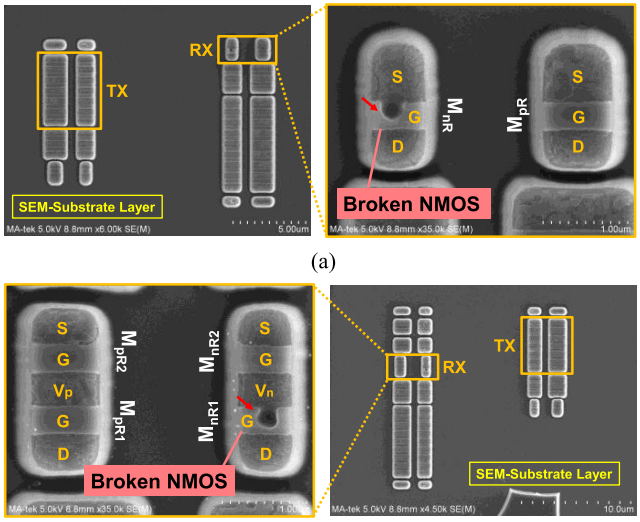


Fig. 18. De-layer SEM anomalies of (a) reference design after −300-V CDM test on VDD1, and (b) Type-B design after −500-V CDM test on VDD1.

the defect can be analyzed because of gate-oxide breakdown. In our hands, the failure samples have been implemented by the de-layer procedure and got similar results for each design after VDD1(−) or VDD2 (−) stress condition. In Fig. 18, the reference/Type-B design passed VDD1(−) 200/400 V CDM qualification but failed at VDD1(−) 300/500 V revealed a gate oxide defect in RX-NMOS. In Fig. 19, the Type-A/Type-C design passed VDD2(−) 200/300-V CDM qualification but failed at VDD2 (−) 300 /400 V revealed a gate oxide defect in RX-PMOS.

Significantly, for the reference design, the gate oxide of RX-NMOS (M_{nR}) in the VDD2/VSS2 domain is damaged by large transient overvoltage due to CDM, but no damage was observed on RX-PMOS (M_{pR}) [see Fig. 18(a)]. Equally, Type-B design has the same phenomenon as mentioned above; only the gate oxide of RX-NMOS (M_{nR1}) is damaged [see Fig. 18(b)]. In contrast, for Type-A design, the gate oxide of RX-PMOS (M_{pR1}) in the VDD2/VSS2 domain is damaged due to CDM, but no damage was observed on RX-NMOS (M_{nR1}) [see Fig. 19(a)]. Equally, for the Type-C design, only the gate oxide of RX-PMOS (M_{pR1}) is damaged [see Fig. 19(b)].

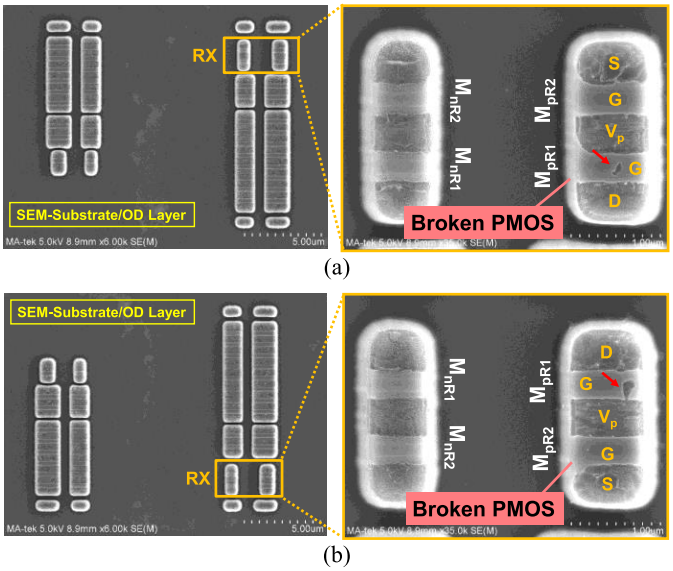


Fig. 19. De-layer SEM anomalies of (a) Type-A design after −300-V CDM test on VDD2, and (b) Type-C design after −400-V CDM test on VDD2.

V. Conclusion

ESD threats on the cross-domain interface circuits between the separated power domains are studied in this work. Some new ESD protection designs of different receiver modules with stacking MOS transistor structures have been proposed and successfully verified in 0.18-μm 1.8-V CMOS technology. The CDM-like simulation was adopted to predict the failure point and to explain the observed failure mechanism. The difference between HBM and CDM is discussed and revealed that the Type-C design is a better solution for practical applications. Finally, the IR-OBIRCH and the de-layer SEM results showed the gate-oxide damage in each design, verifying the failure mechanism of the interface circuit under cross-domain CDM stresses. The proposed designs can be used in IC products with separated power domains to enhance the robustness against cross-domain CDM events.

Acknowledgment

The authors would like to thank Taiwan Semiconductor Research Institute (TSRI) with the support of EDA Tools for test chip design and chip fabrication via TSMC. The authors also thank the Editor and Reviewers for their valuable suggestions to improve this work for publication.

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