Schottky-Embedded Silicon-Controlled Rectifier With High Holding Voltage Realized in a 0.18-μm Low-Voltage CMOS Process

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***Abstract*— The silicon-controlled rectifier (SCR) has been reported to protect CMOS integrated circuits (ICs), due to high ESD robustness within a small silicon area. However, the holding voltage (V_h) of the SCR device was too low to suffer the latch-up issue. Thus, the V_h value of the SCR device must be improved to be greater than the circuit operating voltage for safe applications. In this work, the Schottky-embedded modified lateral SCR (SMLSCR) with high holding voltage for ESD protection was proposed and verified in a 0.18-μm 1.8-V/3.3-V CMOS process. By using the Schottky barrier junction, the V_h value of the SCR device can be improved by the reverse-bias Schottky barrier diode (SBD) that is embedded into the SCR device structure. Among those experimental results on the SMLSCR devices with split layout parameters in the silicon test chip, the SMLSCR device without P^+ guard ring has the best second breakdown current (I_{t2}) of 3.1 A and a high V_h value of 9.7 V.**

***Index Terms*— Electrostatic discharge (ESD), latch-up, Schottky barrier diode (SBD), Schottky-embedded modified lateral silicon-controlled rectifier (SMLSCR), silicon controlled rectifier (SCR).**

I. Introduction

THE Schottky barrier diode (SBD) [1] is a kind of low turn-on voltage device, which can be switched under high-speed mode. Because the SBD device is a single-pole and multiple carrier device working through the metal semiconductor contact barrier [2], the forward voltage drop of the SBD device is lower than that of the normal p-n junction diode. In addition, the reverse recovery time of SBD device is much smaller than that of the normal p-n junction diode. Therefore, the SBD devices are suitable for the applications of high-frequency circuits, rectifier circuits, and power protection circuits [3]–[5].

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With the progress of process improvement, the shrinking of gate oxide causes worse electrostatic discharge (ESD) robustness in the CMOS devices [6]. Thus, the CMOS integrated circuits (ICs) must be equipped with on-chip ESD protection devices to avoid the overstress from the ESD events. The silicon-controlled rectifier (SCR), with high ESD robustness within a small silicon area, had been studied for ESD protection in some CMOS processes [7]–[10]. However, the very low holding voltage (V_h) of SCR devices would lead to potential latch-up risk [11]–[13] when the IC's are operating under normal circuit applications.

In this work, a new Schottky-embedded modified lateral SCR (SMLSCR) is proposed and verified in a 0.18-μm 1.8-V/3.3-V CMOS process. With the embedded Schottky barrier junction, the holding voltage of the proposed SMLSCR can be significantly increased for high-voltage circuit applications.

II. Device Structures

A. Prior-Art MLSCR

The modified lateral SCR (MLSCR) was earlier reported for on-chip ESD protection application in CMOS technology [14]. Fig. 1 shows the layout top view and the corresponding cross-sectional view of the MLSCR device, which can effectively reduce the turn-on voltage (V_{t1}) of the SCR device by inserting the heavily doped N^+ or P^+ regions across the boundary of n-well and p-well. In Fig. 1, the SCR path includes P^+, n-well, p-well, and N^+ from anode port to cathode port, and the inserted heavily doping region has been selected with N^+ diffusion between the boundary of n-well and p-well. The distance ($D1$) from anode to cathode of the SCR path inside the MLSCR is drawn with 4.6 μm in a given 0.18-μm 1.8-V/3.3-V CMOS process as a baseline for comparison.

Fig. 2 shows the TLP-measured I–V characteristic of the fabricated MLSCR device with 100-μm device width under positive anode-to-cathode TLP stress. The turn-on voltage (V_{t1}), holding voltage (V_h), and the second breakdown current (I_{t2}) of this MLSCR device are 11.6 V, 2.8 V, and 7.5 A, respectively. Although the MLSCR can reach a very high level of I_{t2} current for good ESD robustness, yet the holding voltage of MLSCR was still too low for the applications in some neuro-stimulation biomedical chips those are often operated with higher voltage levels. Thus, the holding voltage

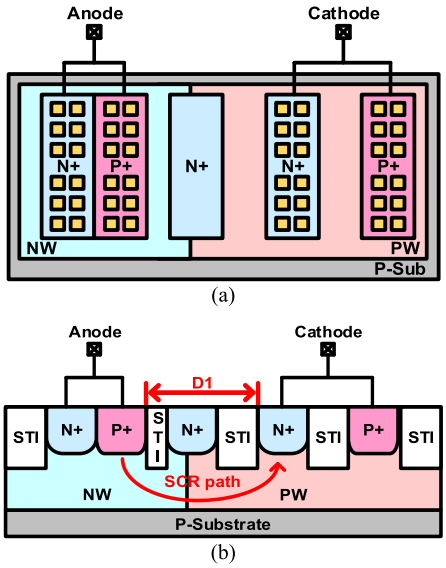

Fig. 1. (a) Layout top view and (b) corresponding cross-sectional view, of the MLSCR [14].

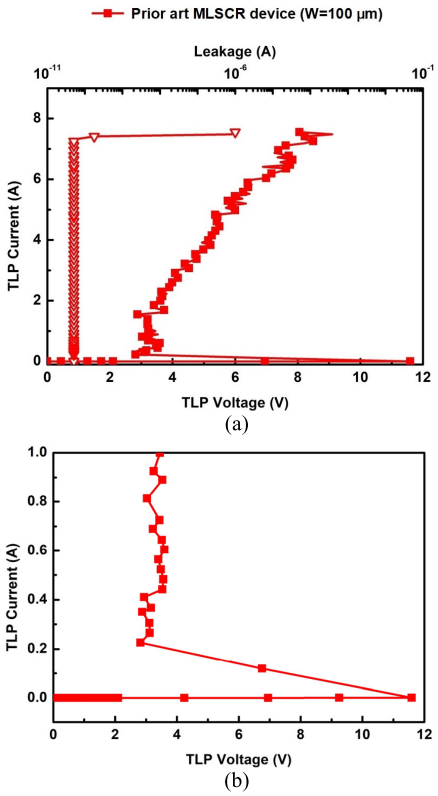

Fig. 2. (a) TLP-measured *I*–*V* characteristic of the MLSCR device under positive anode-to-cathode TLP stress. (b) Zoomed-in view for investigating the trigger voltage (V_{t1}) and holding voltage (V_h) of the MLSCR.

of MLSCR must be further increased for safe applications in high-voltage circuits [15].

B. Proposed Schottky-Embedded Modified Lateral SCR

The SBDs were ever studied in some ESD protection designs [16], [17]. In this work, to enhance the holding voltage of MLSCR, the reverse bias of the Schottky barrier junction is used to increase the V_h of the SCR device [18].

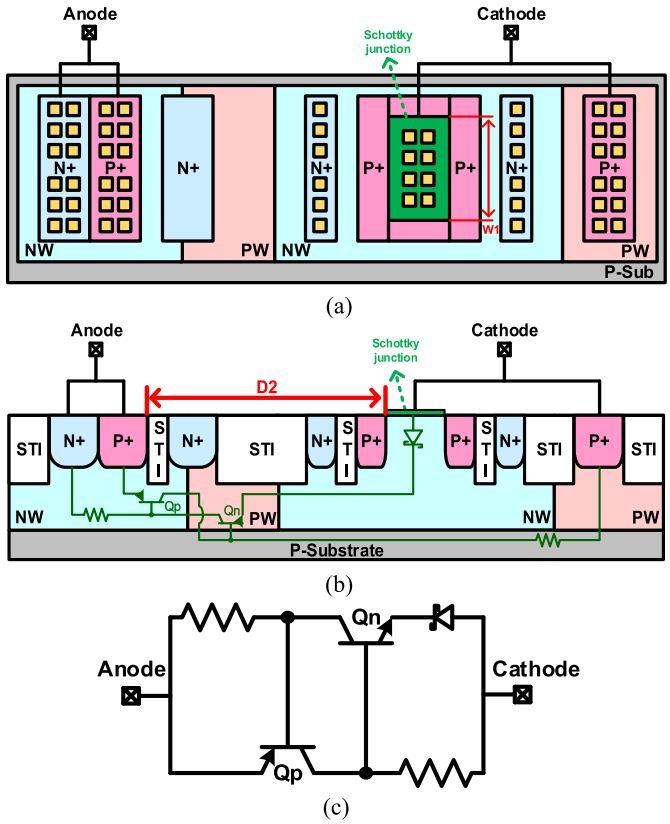

Fig. 3. (a) Layout top view, (b) corresponding cross-sectional view, and (c) equivalent circuit of the proposed type-A SMLSCR.

Fig. 3 shows the schematic layout top view and the corresponding cross-sectional view of the proposed type-A SMLSCR. The SCR path includes P^+, n-well, p-well, and n-well from anode port to cathode port, and a Schottky junction has been inserted between the cathode port and the second n-well region to enhance the total holding voltage. The inserted heavily doping region between the boundary of n-well and p-well has been selected as N^+ diffusion to reduce the turn-on voltage of the SCR device. The narrow floating N^+ regions around the Schottky junction in the second N-well are the original cathode port of the Schottky diode, and these N^+ regions cannot be removed due to the request of design rules from foundry. The Schottky junction that connected to the cathode port was surrounded by the P^+ guard ring, and the maximum value of Schottky junction width ($W1$) is 16 μm, as specified by design rules. In the test chip, a single finger width of the SMLSCR device layout is drawn as 50 μm, so the cathode port of SMLSCR is consisted of three segments of SDB devices. The distance of the SCR path ($D2$) from anode to cathode in the SMLSCR is kept as the same as that (4.6 μm) of MLSCR for performance comparison.

To investigate the influence of some layout parameters on the SMLSCR devices, three types of SMLSCR devices have been split and fabricated in this work, as the list shown in Table I. The total widths of type-A to type-C SMLSCR devices are 100 μm, and the width of each finger is 50 μm. The Schottky junction width ($W1$) of type-A, B, C SMLSCR devices is 16 μm, so the number of Schottky

TABLE I
PARAMETERS OF PROPOSED SCR DEVICES

Name	Type of Proposed SCR Device		
	A	B	C
Total Width (μm)	100	100	100
Number of Fingers	2	2	2
Schottky Area Width (μm)	16	16	16
Schottky Area Number per Finger	3	3	3
With or Without P+ Guard Ring	Yes	No	Yes
P+ Guard Ring Width (μm)	0.22	N/A	0.5

area in each finger is 3. The Schottky junction area of type-A and type-C SMLSCR devices is surrounded by P^+ guard ring. To investigate the relationship between device ESD level and the P^+ guard ring that surrounding the Schottky junction, the difference among the type-A, type-B, type-C SMLSCR devices in layout is the width of P^+ guard ring. The width of P^+ guard ring in type-A and type-C SMLSCR devices are 0.22 and 0.5 μm, respectively. Different to the type-A and type-C SMLSCR, the Schottky junction area of type-B SMLSCR device is not surrounded by P^+ guard ring (i.e., without P^+ guard ring) for performance study. The layout parameters of all proposed SMLSCR devices are listed in Table I.

III. EXPERIMENTAL RESULTS

The proposed type-A to type-C SMLSCR devices in this work have been fabricated in a 0.18-μm 1.8-V/3.3-V CMOS process.

A. Transmission Line Pulsing Measurement

To investigate the I-V characteristics of the test devices, a transmission line pulsing (TLP) generator [19] with a pulsewidth of 100 ns and rising time of 10 ns is used to measure the second breakdown current (I_{t2}) and holding voltage (V_h) of the proposed type-A to type-C SMLSCR devices. Fig. 4 shows the TLP-measured I–V characteristics of the proposed SMLSCR devices under positive anode-to-cathode TLP stress. The SCR current paths of the proposed type-A to type-C SMLSCR devices can be triggered at 15.4, 13.9, and 15.8 V, respectively. Both of the proposed devices have a snapback phenomenon, and the holding voltage (V_h) of these SMLSCR devices from type-A to type-C are 10.7, 9.7, and 12 V, respectively. According to the snapback phenomenon, the SCR path of proposed SMLSCR devices sure can be triggered under positive anode-to-cathode ESD stress. The second breakdown currents (I_{t2}) of the proposed type-A to type-C SMLSCR devices are 2.1, 3.1, and 1.5 A, respectively.

To investigate the turn-on speed of the proposed devices during the ESD stress, a very fast TLP (VF-TLP) system with a 200-ps rise time and a 5-ns pulsewidth is used. The VF-TLP measurements in this work are on-wafer, which are measured without bonding wire. Fig. 5 shows the VF-TLP I–V curves

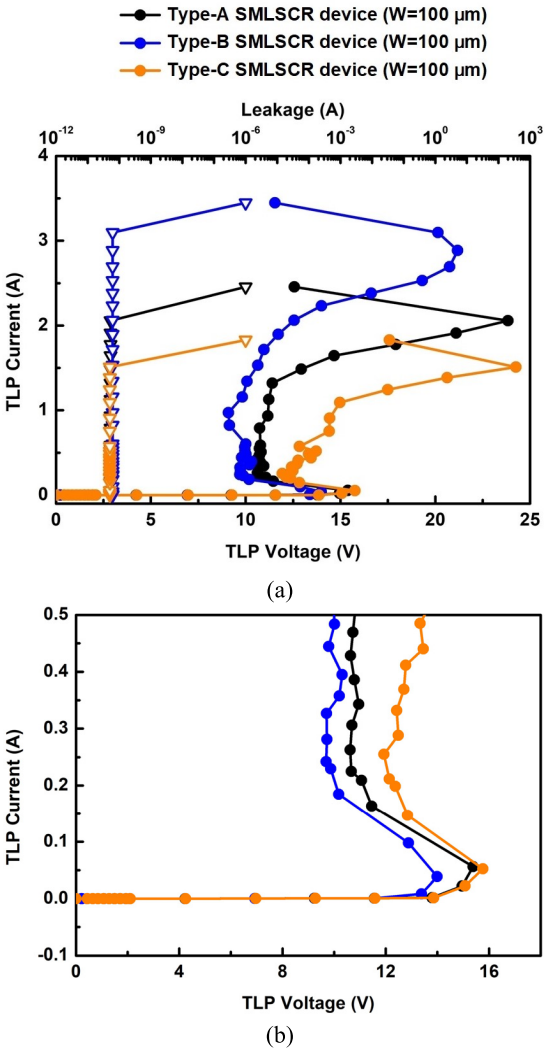

Fig. 4. (a) TLP-measured I–V characteristics of the proposed type-A to type-C SMLSCR devices with two fingers under positive anode-to-cathode TLP stress. (b) Zoomed-in view for investigating the trigger voltage (V_{t1}) and holding voltage (V_h).

comparison among the proposed SMLSCR devices and the prior art MLSCR device. According to the measurement results, the trigger voltages of proposed type-A to type-C SMLSCR devices and MLSCR devices are 13.6, 12, 14, and 10 V, respectively.

To investigate the clamping voltage of the proposed SMLSCR devices and prior art MLSCR device, the VF-TLP measured voltage waveform under 3-A condition is shown in Fig. 6, where the voltage waveform is chosen under 3-A condition of VF-TLP current. The peak overshoot voltages of type-A to type-C SMLSCR and MLSCR devices are 29.3, 28.2, 30, and 20 V, respectively. The clamping voltages of type-A to type-C SMLSCR devices are similar, but the type-B SMLSCR device has a little lower clamp voltage as shown in Fig. 6.

B. Leakage Current

Fig. 7 shows the leakage currents of all proposed devices, which were measured from anode port to cathode port. As devices at the temperature of 25 °C, the leakage current of

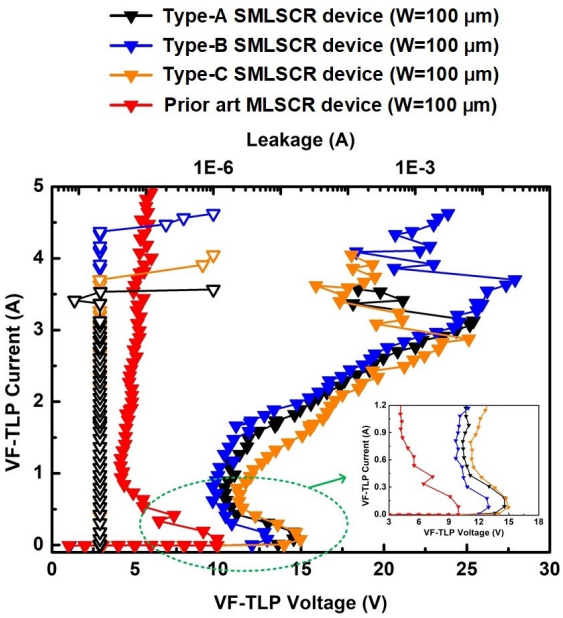

Fig. 5. VF-TLP measured *I–V* curves of proposed devices and prior art MLSCR device with two fingers under positive anode-to-cathode VF-TLP stress.

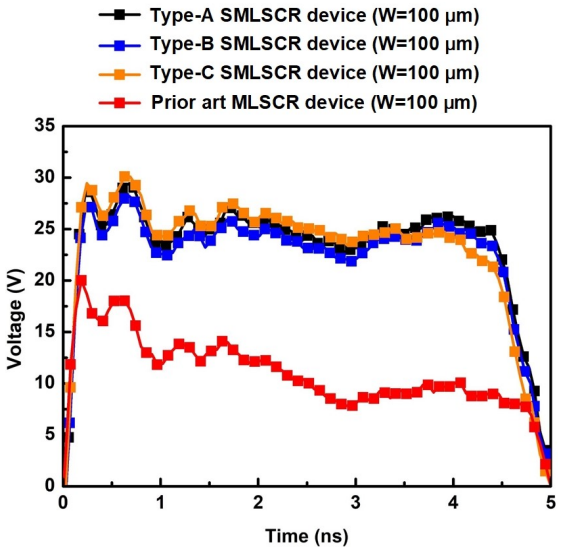

Fig. 6. VF-TLP measured voltage waveforms among proposed devices and prior art MLSCR device with two fingers under 3-A condition.

proposed SMLSCR devices from type-A to type-C are 0.7, 1.3, and 0.9 nA under 9-V supply voltage. When the temperature rises to 125 °C, the leakage currents under 9-V supply voltage from type-A to type-C SMLSCR are 0.68, 0.73, and 0.71 μA, respectively. For the proposed SMLSCR devices, the leakage currents are sufficiently low under 9-V operating condition, and there is no considerable difference between all proposed SMLSCR devices at high temperatures.

C. DC I–V Curve

To investigate the holding voltage (V_h) of the proposed devices, the dc I–V curves of type-A to type-C SMLSCR devices have been measured by curve tracers. Fig. 8 shows the measured dc I–V curves of all devices from anode port

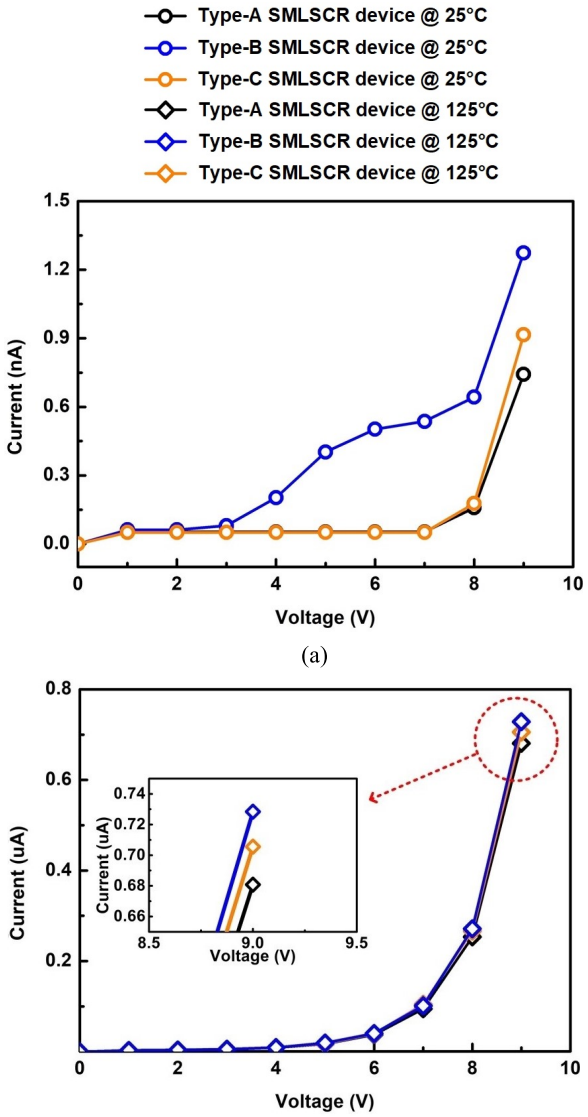

Fig. 7. Measured leakage currents of proposed type-A to type-C SMLSCR devices at (a) 25 °C and (b) 125 °C.

to cathode port at 25 °C and 125 °C. According to Fig. 8, the V_h values of type-A to type-C SMLSCR devices are 11.2, 10.1, and 11.7 V at 25 °C, respectively. Compared with the measured results from TLP, the V_h values measured by curve tracers do not have an obvious difference. When the temperature rises to 125 °C, the V_h values from type-A to type-C SMLSCR devices are 9.6, 8.7, and 9.8 V, respectively. According to the abovementioned results, the relationship of V_h values between type-A to type-C SMLSCR devices can remain at the same level.

D. Failure Analysis

To further observe the certain failure locations, the scanning electron microscope (SEM) experiment was used. Fig. 9 shows the SEM photograph of the proposed type-B SMLSCR device after 4.5-kV HBM ESD test. The ESD current flowing through the silicon chip caused the serious nonrecoverable burned-out failure, which is obviously located at the path from the P^+ implant region to the Schottky junction area. According to

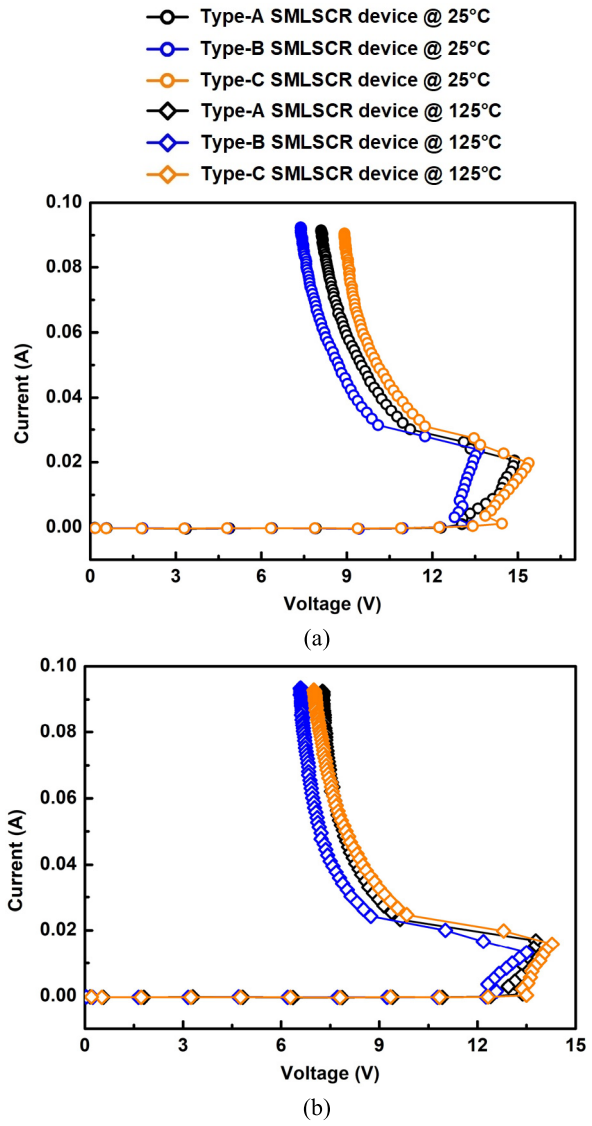

Fig. 8. Measured dc *I–V* curves of proposed type-A to type-C SMLSCR devices at (a) 25 °C and (b) 125 °C.

the result, the proposed devices do discharge the ESD current from anode to cathode through the SCR path.

IV. Comparison and Discussion

A. Discussion of Measurement Results

The SCR device is widely known as a low holding voltage (V_h) ESD protection device, so many studies are devoted to improving V_h of the SCR device. Moreover, lots of circuit applications are often operated with higher voltage levels, such as implanted biomedical devices. Among them, the supply voltage of ±9 V has been used in the circuits of implanted biomedical devices, such as a charge pump system and stimulator circuit [20]–[22]. Therefore, the SCR devices under 9-V VDD-to-GND or I/O-to-GND applications will be explored in this work.

Compared with the MLSCR device, the holding voltage (V_h) of the proposed SMLSCR devices has been enhanced by the Schottky junction. In Section II-A, the holding voltage (V_h) of prior art MLSCR device is only 2.8 V, and this V_h can be enhanced to 10.7 V by using the Schottky junction

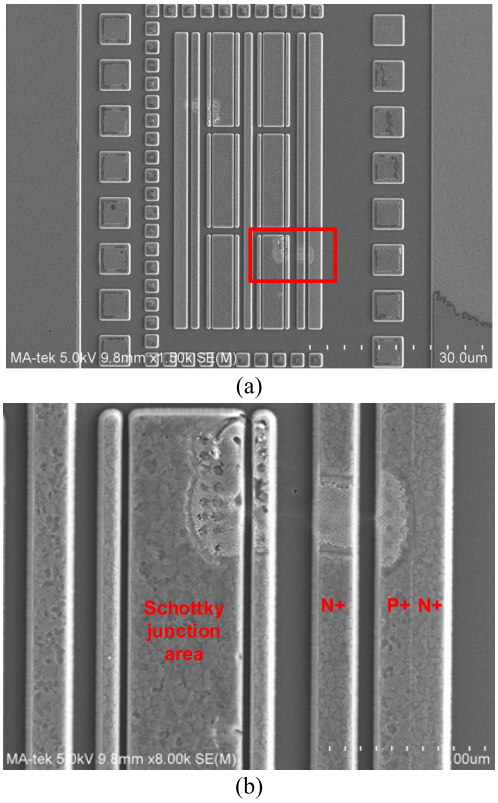

Fig. 9. (a) SEM photograph of proposed type-B SMLSCR device and (b) zoomed-in view after 4.5-kV HBM ESD test.

at the cathode port like proposed type-A SMLSCR. However, the turn-on voltage (V_{t1}) of the proposed type-A SMLSCR has been raised from 11.6 to 15.4 V at the same time, but the V_{t1} can also be reduced by using the trigger circuit [23].

In Section III-A, the holding voltage (V_h), turn-on voltage (V_{t1}), and second breakdown current (I_{t2}) have been measured by the TLP system. Type-A and type-C SMLSCR devices have higher V_{t1} due to the presence of the P^+ guard ring. Without the P^+ guard ring, the V_{t1} can be reduced like type-B SMLSCR device as 13.9 V. To avoid the latch-up risk under normal circuit operation, the holding voltage (V_h) should be higher than the supply voltage. By changing the width of the P^+ guard ring from 0.22 to 0.5 μm, the V_h of type-A and type-C SMLSCR devices are obvious difference as 10.7 and 12 V, respectively. The V_h value can also be effectively reduced by removing the P^+ guard ring, just like type-B SMLSCR device as 9.7 V. The reason for the lower V_h and V_{t1} of type-B SMLSCR device is due to the "edge effect." The crowding of the high electric field gives rise to excess leakage current and low breakdown voltage [24], which can be also confirmed by the previous measurement results. Although the V_h value of type-B SMLSCR device is closest to 9-V supply voltage, it will degrade to 8.7 V at 125 °C as shown in Fig. 8(b). Therefore, the type-B SMLSCR device is suitable for the circuit of operation voltage below 8 V in a high-temperature situation. The second breakdown current (I_{t2}) is a value which used to judge the ESD protection capability of devices. The higher value of device I_{t2} can provide a better ESD protection capability for circuits.

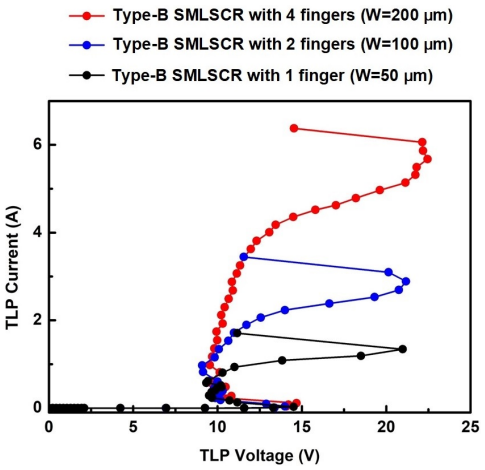

Fig. 10. TLP-measured *I–V* characteristics of the proposed type-B SMLSCR device with a different number of fingers under positive anode-to-cathode TLP stress.

Based on the type-A SMLSCR device, the I_{t2} value of devices would be degraded by increasing the width of the P^+ guard ring. The I_{t2} values of type-C SMLSCR devices is only 1.5 A. On the other hand, the type-B SMLSCR device has the highest I_{t2} value of 3.1 A by removing the P^+ guard ring. According to the abovementioned reasons, the proposed type-B SMLSCR device has better ESD protection ability due to the lower turn-on voltage (V_{t1}), suitable holding voltage (V_h), and the highest second breakdown current (I_{t2}) value.

To find out the difference between devices size, changing the number of fingers is a simpler way which can considerably influence the devices current-handling capability and ON-state resistance (R_{ON}). The increasing fingers number is expected to increase the devices current-handling capability and decrease R_{ON} because of the enlarged device size. Fig. 10 shows the TLP-measured *I–V* characteristics of the proposed type-B SMLSCR device with a different number of fingers under positive anode-to-cathode TLP stress. By using the Schottky barrier layer, the ON-state resistance (R_{ON}) of type-B SMLSCR device with 1, 2, and 4 fingers have an obvious change around 0.93, 2.06, and 4.18 A, respectively. Compared with the I_{t2} values of each device from finger 1 to 4 as 1.34, 3.10, 6.06 A, the ON-state resistance (R_{ON}) would be changed around 70% along the whole snapback region. In addition, from the VF-TLP measured *I–V* curves shown in Fig. 5, the ON-state resistance (R_{ON}) would be changed around 50% along the whole snapback region. According to the above-mentioned results, the number of device fingers should be carefully selected to meet the ESD protection window in the applications.

Fig. 11(a) shows the ON-state resistance (R_{ON}) of proposed type-B SMLSCR devices with a different number of fingers. The Ron values of the type-B SMLSCR device from 1 to 4 fingers are 4.91, 2.93, and 0.77 Ω, respectively, and when the number of finger increases, it sure has lower Ron value. Although the lower V_{t1} value can turn on the proposed SMLSCR device first to release the ESD current before internal circuit breakdown, the high clamping voltage shown in Fig. 6 may still have some risk to cause damage to the

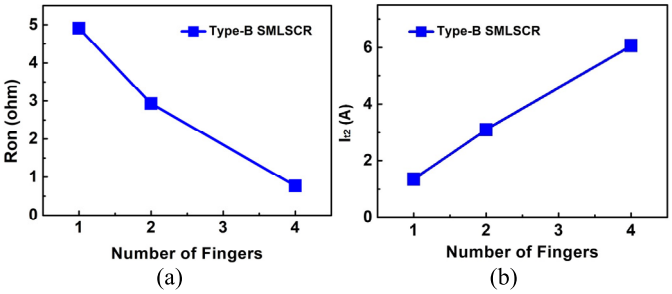

Fig. 11. (a) ON-state resistances of proposed type-B SMLSCR device with a different number of fingers. (b) TLP-measured second breakdown current (I_{t2}) of proposed type-B SMLSCR device with a different number of fingers.

TABLE II
MEASURED RESULTS OF DEVICES

Name	MLSCR	Type-A SMLSCR	Type-B SMLSCR
Total Width (μm)	100	100	100
Number of Fingers	2	2	2
V_{t1} (V)	11.6	15.4	13.9
I_{t2} (A)	7.5	2.1	3.1
Ron (Ω)	1.05	1.26	2.93
V_h (V)	2.8	10.7	9.7
HBM ESD Level	≧8 kV	4 kV	4.5 kV
Layout Area (mm^2)	1.45	1.45	1.45

internal circuits [25], [26]. To solve this issue, the number of device fingers should be increased to reduce its turned-on resistance, and therefore to reduce the clamping voltage at the same current level. Fig. 11(b) shows the TLP measured second breakdown current (I_{t2}) of proposed type-B SMLSCR devices with a different number of fingers. Compared with Fig. 11(a), the one-finger device has the highest R_{ON} and lowest I_{t2} value, while the four fingers device has the lowest R_{ON} and highest I_{t2} value, respectively. According to the abovementioned results, the ESD robustness can be enhanced by increasing the finger number of device.

Table II shows the HBM ESD Level of prior art MLSCR and proposed type-A, type-B SMLSCR devices. The HBM ESD robustness of prior art MLSCR is ≥8 kV, and the HBM ESD robustness of proposed type-A and type-B SMLSCR are 4 and 4.5 kV, respectively. According to the abovementioned results, the HBM ESD Level values of all devices are similar to their TLP measured results. All of the main measured results of MLSCR, type-A, and type-B SMLSCR devices are shown in Table II.

In summary, the proposed SMLSCR devices can provide a good ESD protection ability for high-voltage applications. However, the proposed SMLSCR devices would have a high voltage overshoot at a lower ESD transient voltage. To improve the capability of protecting the internal circuits, the finger number of the proposed SMLSCR device should be further increased to reach a lower R_{ON} value and therefore to get a lower voltage overshoot. In addition, the risk of high voltage overshoot can be mitigated by the two-stage ESD protection circuit structure [27] where an isolation resistor was connected between the primarily ESD protection device and

TABLE III
COMPARISON OF LAYOUT AREA AND ESD ROBUSTNESS BETWEEN SCR DEVICES

Name	MLSCR	Type-A SMLSCR	Type-B SMLSCR
Number of Stacking SCR	4	1	1
Stacked Device V_h (V)	11.2	10.7	9.7
I_{t2} (A)	7.5	2.1	3.1
Layout Area for 9-V Application (mm^2)	5.80	1.45	1.45
I_{t2}/ (Layout Area for 9-V Application) (A/ mm^2)	1.29	1.45	2.14

the I/O devices. With the two-stage protection structure, the ESD current can be released first by the co-designed I/O devices before the proposed SMLSCR is triggered. After the proposed SMLSCR is turned on, the ESD current can be fully discharged through the proposed SMLSCR to the GND.

B. FOM Comparison

Table III shows the figures of merit (FOMs) comparison of devices. To avoid the latch-up risk under normal circuit operation, the holding voltage (V_h) of ESD protection devices should be higher than the supply voltage. In this work, the discussion of ESD protection devices is focused on the 9-V supply voltage application. Although the prior art MLSCR device has a good I_{t2} value, the V_h value of the MLSCR device is too low to suffer the latch-up issue. There are many ways to increase the value of V_h, and one simple way is the stacking structure [28]–[30]. By using the stacking structure, the value of V_h can be effectively increased, and the V_h value will grow several times with the number of stacking devices [31], [32]. The value of device I_{t2} will not change drastically by increasing the stacking number of devices, and it can be maintained at the same level. For the 9-V supply voltage application, higher current-handling capability and high enough holding voltage (V_h) value are needed. According to the abovementioned reasons, higher value of I_{t2}/(Layout Area for 9-V Application) is preferable, and this FOM can more effectively reflect the ESD robustness of the SCR device than I_{t2} alone. To enhance the V_h value of MLSCR, the number of stacking MLSCR should be 4, and the V_h value of stacked MLSCR would be enhanced to 11.2 V. Thus, the test results of I_{t2}/(Layout Area for 9-V Application) for MLSCR, type-A SMLSCR, type-B SMLSCR are 1.29, 1.45, and 2.14 A/mm^2, respectively. According to the abovementioned results, type-A and type-B SMLSCR devices both have better I_{t2}/(Layout Area for 9-V Application) values under 9-V supply voltage applications.

V. CONCLUSION

The proposed SMLSCR devices have been successfully verified in a 0.18-μm 1.8-V/3.3-V CMOS process, where the devices holding voltage (V_h) can be increased effectively by using the Schottky barrier junction. The proposed SMLSCR devices have a high enough holding voltage (V_h) to avoid the latch-up risk under 9-V supply voltage applications, and the proposed type-B SMLSCR device has the highest second breakdown current (I_{t2}) value as 3.1 A. Compared to the prior art MLSCR device, the FOM of the proposed type-A and type-B SMLSCR devices both have better current-handling capability under the same layout area, and they also have sufficiently low leakage current under high-voltage circuit applications. Therefore, the proposed devices verified in this article will be a useful ESD protection solution for high-voltage circuit applications in the CMOS technology.

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