Optimization on Bi-Directional PNP ESD Protection Device for High-Voltage FlexRay Applications

Chen-Wei Hsu, Yu-Hsin Li, and Ming-Dou Ker, *Fellow, IEEE*

***Abstract*— The I/O of CMOS integrated circuits of for FlexRay communication has to be tolerant with the input signals of ±60 V in its normal applications. Thus, the on-chip electrostatic discharge (ESD) protection devices for such I/O pin must be kept off unless the bus voltage is higher than 60 V or lower than −60 V. In this work, the bi-directional p-n-p (Bi-PNP) device was proposed and optimized for bi-directional ESD protection in the FlexRay communication systems. The proposed Bi-PNP devices were verified in a 0.15-μm BCD technology. The relationships between the layout spacing of doping layers and other device characteristics, including trigger voltage (Vt1) and breakdown voltage (BV), were investigated, respectively. The size dependence on the ESD robustness was also studied. The transient response of the proposed Bi-PNP device under fast ESD stress was investigated by very fast TLP (vf-TLP) and TLP measurement. In addition, the empirical correlations of the It2 on the HBM and IEC 61000-4-2 failure levels were estimated. Finally, the recommended size and parameters of the proposed Bi-PNP device for ±60 V FlexRay application are provided.**

***Index Terms*— Bi-directional electrostatic discharge (ESD) protection, ESD, FlexRay, high voltage ESD protection.**

I. Introduction

With more functions for automobile applications, the request for in-vehicle systems is increasing. On the other hand, the electrical control units (ECUs) in automotive systems are now integrated through semiconductor chips, replacing numerous discrete components. There are several communication protocols for the data transmission interfaces of automobile electronics, such as CAN, LIN, and FlexRay. The FlexRay is the latest communication interface standard after CAN and LIN, that can be used to manage multiple functions including safety and comfort. FlexRay is suitable for operation by wire (X-by-Wire), chassis control, engine control, etc. For these functions directly related to safety, the reliability of the system is more significant. FlexRay has a faster data rate, more flexible data communication, topology selection, fault-tolerant operation, etc. to provide higher transmission speed and reliability for the next-generation in-vehicle control system.

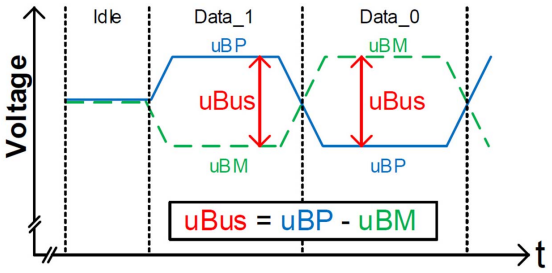

Fig. 1. FlexRay electrical signaling defined in [1].

Fig. 1 shows the FlexRay electrical signaling defined in [1]. The uBus is the voltage difference between bus plus (BP) and bus minus (BM). The bus (BP and BM) on the FlexRay transceiver may face a ±60 V short-circuited hazard with 90 mA maximum output current for a maximum of 400 ms, which originated from the load dump conditions [1]. Fig. 2 illustrates such a situation. As a result, the electrostatic discharge (ESD) protection devices must be "NOT" turned on whenever the voltages of BP and BM are from −60 to 60 V. Fig. 3 shows the schematic of the FlexRay transmitter (Tx) designed in [2]. The D1–D4 are high-voltage diodes, whose reverse breakdown voltages (BVs) are higher than 60 V, against the short-circuited hazard on the bus.

For FlexRay transceivers, some circuits had been designed with the high-voltage BCD technology [2], [3], [4], and some commercially available ICs can be found [5], [6], [7]. But, the ESD protection of the FlexRay system was usually using the

Manuscript received 5 May 2022; revised 22 June 2022, 22 July 2022, and 4 August 2022; accepted 9 August 2022. Date of publication 18 August 2022; date of current version 22 September 2022. This work was supported in part by the "Center for Neuromodulation Medical Electronics Systems" from the Featured Areas Research Center Program within the framework of the Higher Education Sprout Project by the Ministry of Education (MOE) in Taiwan and in part by the Ministry of Science and Technology (MOST), Taiwan, under Contract MOST 109-2221-E-009-100-MY3 and Contract MOST 110-2622-8-009-017-TP1. The review of this article was arranged by Editor C. Duvvury. *(Corresponding author: Ming-Dou Ker.)*

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Digital Object Identifier 10.1109/TED.2022.3198388

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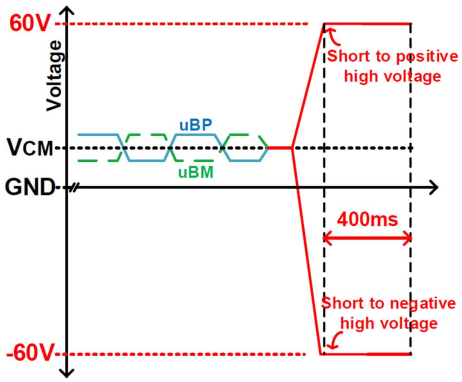

Fig. 2. Bus interface behavior under short-circuit conditions defined in [1].

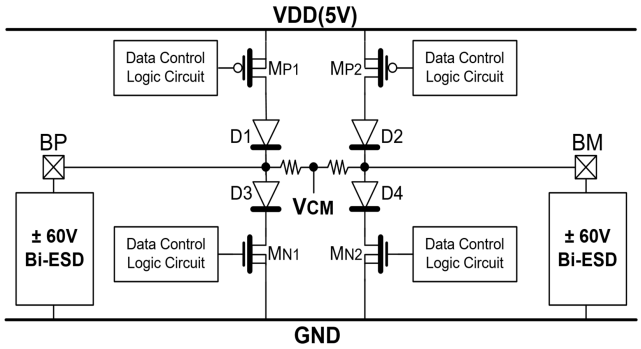

Fig. 3. Schematic of the FlexRay transmitter (Tx) designed in [2] with high-voltage diodes to perform ±60 V tolerance.

transient voltage suppressors (TVSs) on the PCB to sustain the high ESD specification [8]. If the ESD protection device can be integrated with the FlexRay bus driver together, it will help to reduce the system cost.

The on-chip ESD protection level of FlexRay specification [1] stipulates that high voltage pins (BP, BM, V_{IO}, and V_{BAT}) must pass ±6 kV of HBM ESD test. Other low voltage pins (TxD, RxD, idle, etc.) must pass ±2 kV of HBM ESD test. Besides, the bus pins (BP and BM) with direct contact to the external environment must pass 6 kV of IEC 61000-4-2 contact discharge, which directly zap the IC pin with a system-level ESD gun [1]. Compared with the HBM, the system-level ESD gun has a higher storage capacitor and a lower discharge resistor, which creates more than 5× ESD peak current to cause severe damage on the bus pins. Therefore, in FlexRay applications, the ESD protection devices should have ±60 V bi-directional tolerance, symmetrical ESD protection characteristics, and low ON-resistance for high ESD robustness. As shown in Fig. 4, the bus pins (BP and BM) of the FlexRay transceiver should be protected by ±60 V ESD devices.

In this work, a bi-directional p-n-p (Bi-PNP) was proposed and optimized to meet the FlexRay specification. The proposed Bi-PNP devices were fabricated in a 0.15-μm BCD technology.

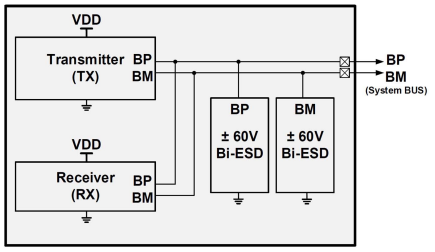

Fig. 4. Schematic of FlexRay transceiver with 60-V bi-directional ESD protection devices.

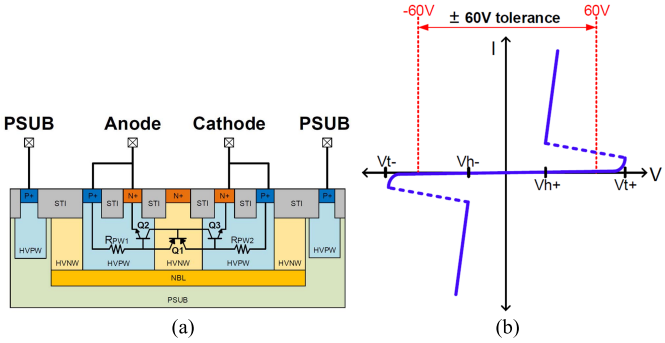

Fig. 5. (a) Cross-sectional view and (b) typical *I–V* curve of bi-directional SCR device.

II. Bi-Directional ESD Protection Devices

Most of the ESD protection devices in CMOS ICs are uni-directional. To achieve better area efficiency and lower ON-resistance, the stand-along bi-directional ESD devices are necessary for bi-directional ESD applications in FlexRay.

Silicon control rectifier (SCR) was regarded as a good ESD protection device due to its high ESD robustness in a small area. Conventional SCRs have snapback characteristics in one direction. As a result, the bi-directional SCR (Bi-SCR) was developed to provide bi-directional path for ESD protection [9], [10], [11], [12], [13], [14], [15], [16]. For example, Salcedo *et al.* proposed the symmetrical/asymmetrical bi-directional ESD devices with adjustable forward and reverse characteristics by different junction configurations [15], [16]. Fig. 5(a) and (b) shows the cross-sectional view and typical *I–V* curve of Bi-SCR, respectively. Bi-SCR is capable of conducting both positive and negative ESD currents with high ESD robustness, low ON-resistance, low holding voltage, and high area efficiency.

However, as shown in Fig. 5(b), the low holding voltages of Bi-SCR are often lower than 60 V on both the positive and negative sides. Such low holding voltages of Bi-SCR may suffer the failure of the signal integrity in application systems [17] and even may cause a latch-up threat. In [12], [13], and [14], some ways were tried to increase the holding voltage to solve this issue. Besides, the concerns with the low holding voltage in Bi-SCR devices could also be addressed by beta degeneration [18], for instance, by selectively reducing the effect of the n-p-n action and making the p-n-p action more

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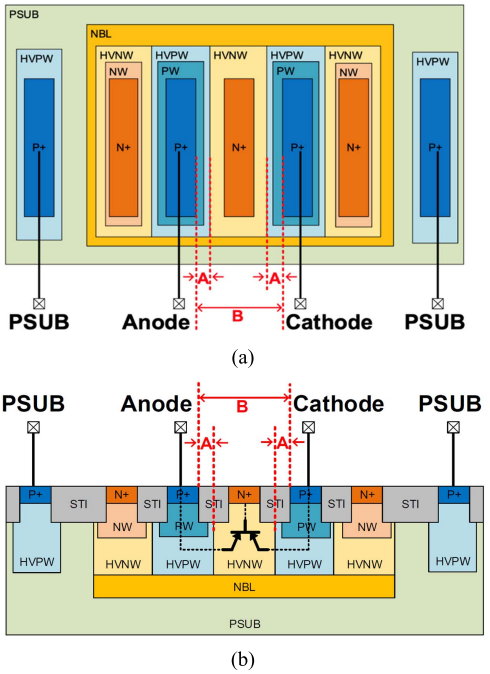

Fig. 6. (a) Top-view and (b) cross-sectional view of the proposed Bi-PNP device (take the uni-finger device for example).

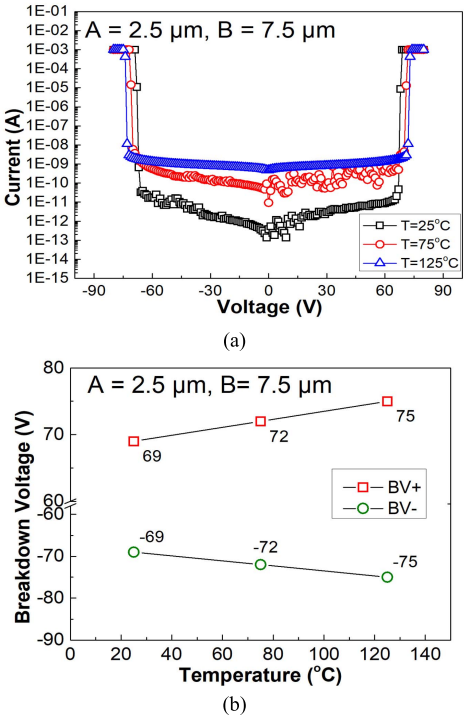

Fig. 7. (a) Measured dc *I–V* curves of the proposed Bi-PNP device with $A = 2.5\ \mu$m and $B = 7.5\ \mu$m when the temperature altered from 25 °C to 125 °C. (b) Dependence of dc BV of the proposed Bi-PNP device on the temperature.

dominant while still taking advantage of the SCR action at high current levels. Moreover, for FlexRay application, the ±60 V high-voltage tolerance must be fully considered when the ESD protection device is designed.

To obtain non-snapback characteristics and high ESD robustness, the p-n-p-based device is better than the SCR-based device for bi-directional ESD protection. The p-n-p devices neither damage the signal integrity nor cause latch-up threat because of their non-snapback characteristic. On the other hand, in a traditional PNP device, the junction between P+ diffusion and N-well has a low BV since the P+ diffusion region is heavily doped.

Fig. 6(a) and (b) shows the top-view and the cross-sectional view of the proposed Bi-PNP, respectively (take the uni-finger device for example). The proposed Bi-PNP is composed of HVPW, HVNW, PW, and NW layers. The HVNW with the NBL layer is kept for floating. The two HVPWs with symmetry structures are anode and cathode, respectively. Both anode and cathode provide low-impendence bi-directional discharging paths for the ESD current.

In Fig. 6, the spacing A is defined as the distance from P+ to HVPW. The spacing B is defined as the distance between the two P+ layers, which also represents the size of the HVNW. The breakdown junction consists of HVNW and HVPW. By modifying the spacings A and B in the test chip, the influence on the dc BV, trigger voltage (Vt1), and failure current (It2) can be investigated.

To further obtain the relationships between the ESD robustness and the device dimensions, the total finger numbers of the bi-directional devices are also split in test chip to find the device size that can meet the FlexRay ESD specification of both HBM and IEC61000-4-2. Besides, the spacings between the respective layers should be studied to reach a minimum value for saving the silicon area further. The proposed Bi-PNP test devices with different spacings and device dimensions have been drawn and fabricated in a 0.15-μm BCD technology.

III. Experimental Results

A. DC Characteristics

The semiconductor parameter analyzer of Keysight B1500A is used to measure the dc I–V curve and BV of the test devices. The compliance current was set at 1 mA to avoid burn-out failure during measurement.

Fig. 7(a) and (b) shows the dc measured results on the Bi-PNP device with $A = 2.5\ \mu$m and $B = 7.5\ \mu$m when the temperature altered from 25 °C to 125 °C. The dc BV is always higher than 66 V (1.1 times of 60 V) or lower than −66 V (1.1 times of −60 V) even in the high-temperature conditions. As shown in Fig. 7(b), the BV is increased with the increase of temperature, which is similar to the prior study result [19]. In this work, the BV is defined as the voltage that makes the current of DUT over the compliance current (1 mA).

Fig. 8 shows the BVs of the Bi-PNP devices at 25 °C with a fixed A of 2.5 μm, but B varying from 7.5 to 10.5 μm. Fig. 9 shows the BVs of the Bi-PNP devices at 25 °C with a fixed B of 7.5 μm, but A varying from 2.3 to 2.7 μm.

With the aforementioned measurement result, the BVs of all Bi-PNP devices in this test chip are higher than 66 V (1.1 times of 60 V), which meet the FlexRay applications. In addition, the measurement result shows that the BV of Bi-PNP device can be further increased when B is larger enough ($>10.5\ \mu$m).

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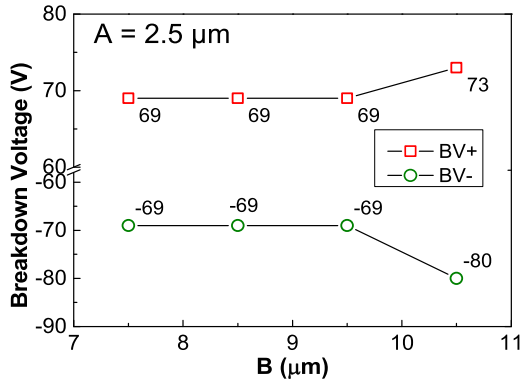

Fig. 8. BV of the proposed Bi-PNP device at 25 °C, when *A* is fixed at 2.5 μm with the value of *B* altering from 7.5 to 10.5 μm.

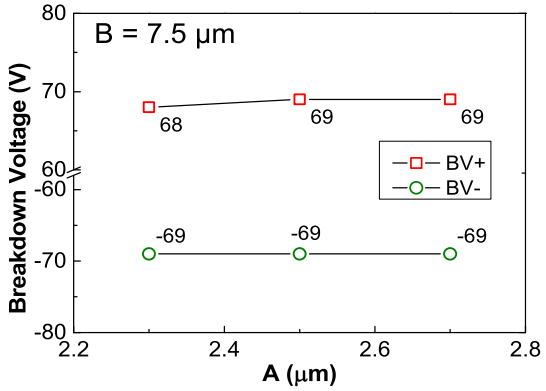

Fig. 9. BV of the proposed Bi-PNP device at 25 °C, when *B* is fixed at 7.5 μm with the value of *A* altering from 2.3 to 2.7 μm.

B. TLP Characteristics

The TLP tester (HED-T5000) with 100-ns pulsewidth and 2-ns rise time is utilized to measure the TLP I–V curves of the test Bi-PNP devices. The power supply (Keithley 2410) is used to bias the devices after each stress so that the leakage current can be observed. The TLP-measurement setup on the fabricated Bi-PNP devices is shown in Fig. 10(a). Both positive and negative TLP pulses are measured for the bi-directional applications. The typical TLP waveforms on the Bi-PNP device with positive voltage and current are shown in Fig. 10(b) and (c), respectively. The negative voltage and current waveforms are shown in Fig. 10(d) and (e), respectively. The typical TLP-measured positive I–V curve is shown in Fig. 11. The Vt1 is defined as the voltage that makes the TLP current higher than 10 mA. The It2 is defined as the current that makes the leakage current over 1 μA under the bias of 60 V.

Fig. 12(a)–(c) shows the TLP I–V curve of Bi-PNP device, in which *A* is fixed at 2.5 μm and *B* is altered from 7.5 to 10.5 μm. Fig. 13 shows the dependence of trigger voltage (Vt1) and failure current (It2) on the spacing *B*, when *A* is fixed at 2.5 μm. According to Fig. 12(b) and (c), the ON-resistances of the Bi-PNP devices slightly increase as the value of *B* increases because of the long current path. The Vt1+ and Vt1− of each Bi-PNP are close to 69 V, and the It2+ and It2− are close to 2.4 and −2 A, respectively. As a result, the Bi-PNP devices with spacing *B* increasing from 7.5 to 10.5 μm do not influence Vt1 and It2. Thus, the HVNW sizes (spacing *B*) in the test devices are all large enough to meet the applications of FlexRay with ±60 V input signals.

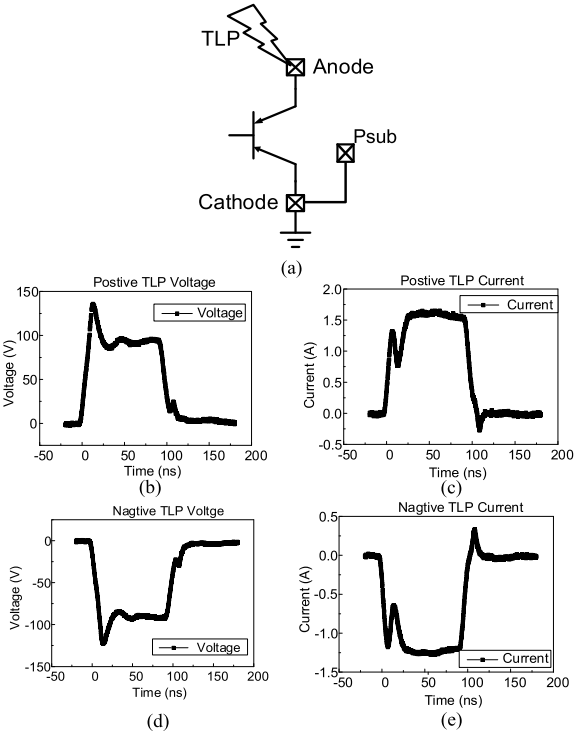

Fig. 10. (a) TLP-measurement setup on the Bi-PNP devices. (b) Positive voltage waveform, (c) positive current waveform, (d) negative voltage waveform, and (e) negative current waveform on the device under test.

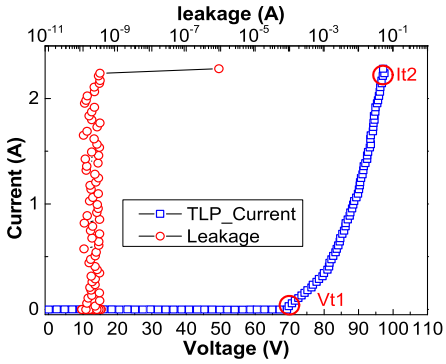

Fig. 11. Measured positive TLP I–V curve of the proposed Bi-PNP device with the definition of Vt1 and It2.

Fig. 14(a) shows the TLP-measured I–V curves of the Bi-PNP devices when *B* is fixed at 7.5 μm and the value of *A* is altered from 2.3 to 2.7 μm. Fig. 14(b) shows the dependence of trigger voltage (Vt1) and failure current (It2) on the spacing *A* of Bi-PNP device. The results showed that the Vt1+ and Vt1− of all Bi-PNP device are close to 70 V, and their It2+ and It2− are close to 2.3 and −2.1 A, respectively. The Bi-PNP devices with the spacing *A* increasing from 2.3 to 2.7 μm do not influence their Vt1 and It2. So, the P+ to HVPW sizes (spacing *A*) are all large enough to meet the FlexRay applications.

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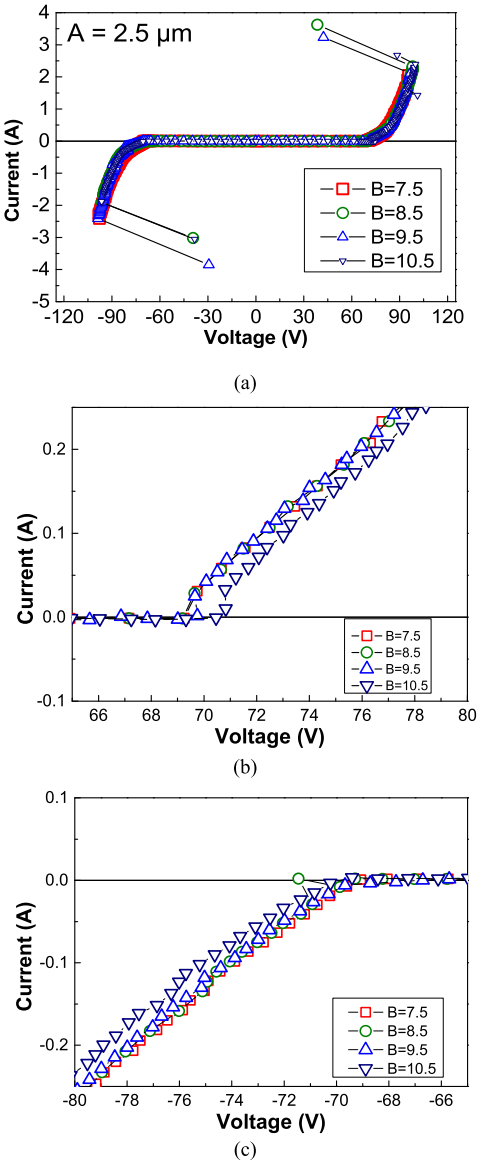

Fig. 12. TLP measured *I–V* curve of the Bi-PNP device with $A = 2.5\ \mu$m in (a) full view, (b) positive voltage side, and (c) negative voltage side when A is fixed at 2.5 μm with B altering from 7.5 to 10.5 μm.

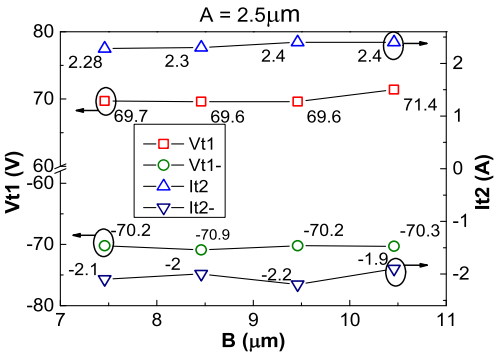

Fig. 13. Dependence of trigger voltage (Vt1) and failure current (It2) on the spacing B of the Bi-PNP device, when A is fixed at 2.5 μm.

Fig. 15(a) shows the TLP-measured I–V curves of the Bi-PNP devices with different finger numbers (device size) altering from 11 to 33 when A (B) is kept at 2.5 (7.5) μm. The

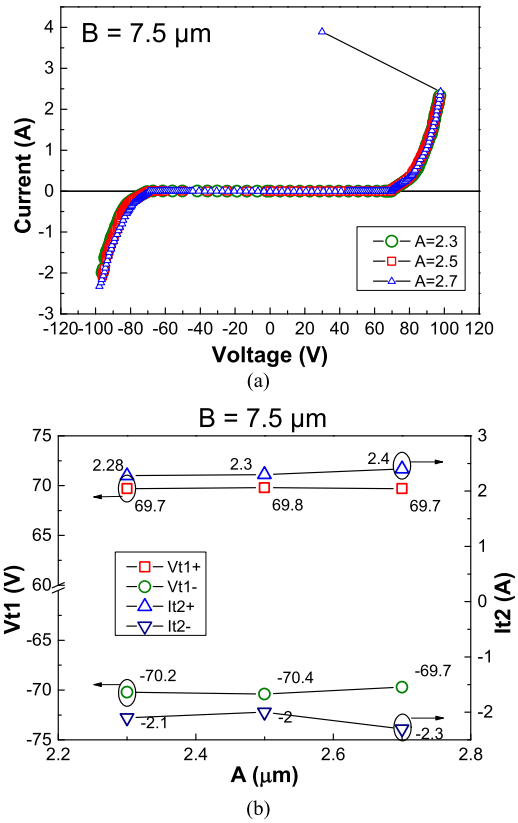

Fig. 14. (a) TLP-measured *I–V* curves of the Bi-PNP device and (b) dependence of trigger voltage (Vt1) and failure current (It2) on the spacing A of Bi-PNP device when B is fixed at 7.5 μm and A is altered from 2.3 to 2.7 μm.

ON-resistance of Bi-PNP device is reduced with the growth of device size. The dependence of trigger voltage (Vt1) and failure current (It2) on the size (finger number) of Bi-PNP device is shown in Fig. 15(b). From the measured results, Vt1+ and Vt1− are all close to 69 V. Besides, It2+ are 2.28, 4.37, and 6.51 A (It2− are 2.07, 3.33, and 4.75 A) when the Bi-PNP devices with 1×, 2×, and 3× sizes (11, 22, and 33 fingers), respectively. The It2 of Bi-PNP device is almost linearly increased as the growth of device size. This implies that the turn-on uniformity under ESD stress among the multifinger Bi-PNP device is good. As a result, Bi-PNP can offer higher ESD robustness by easily increasing its device size.

Finally, the relationships between the spacing A and trigger voltage (Vt1), as well as the relationships between the spacing A and BV, were investigated. This study can provide Bi-PNP device for different voltage applications by modifying its spacing A. Fig. 16 shows the dependence of BV and the TLP-measured Vt1 on the spacing A of the Bi-PNP device, where B is fixed at 7.5 μm with A altering from 0 to 2.0 μm. As seen in Fig. 16, Vt1 and BV increase linearly when A increases from 0 to 1.25 μm. On the other hand, Vt1 and BV almost keep the same value when A is higher than 1.5 μm. As a result, for the 60-V FlexRay application, A is recommended with the value of 1.25 μm to keep its BV to be 1.1 times more than the maximum signal voltage level.

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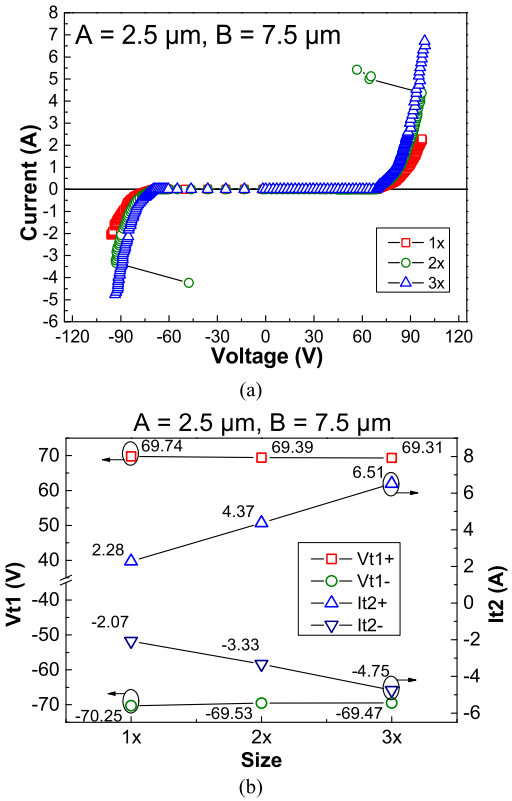

Fig. 15. (a) TLP-measured *I–V* curves of the Bi-PNP devices with different finger numbers altering from 11 to 33. (b) Dependence of trigger voltage (Vt1) and failure current (It2) on the size (finger number) of the Bi-PNP device, when *A* (*B*) is kept at 2.5 (7.5) μm.

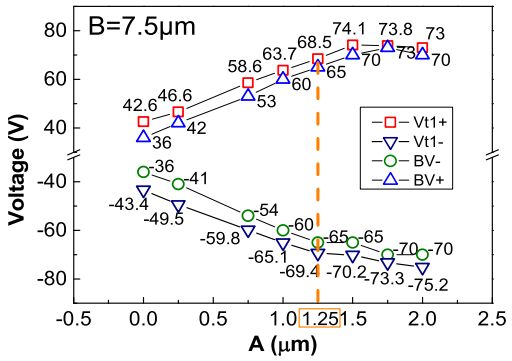

Fig. 16. Dependence of BV and the TLP-measured Vt1 on the spacing *A* of the Bi-PNP device, when *B* is fixed at 7.5 μm with *A* altering from 0 to 2.0 μm.

C. HBM and IEC61000-4-2 ESD Test Results

The HBM ESD tester (HED-W5000M) is utilized to evaluate the HBM ESD failure voltages among the fabricated Bi-PNP devices. As requested in the specification [1], both BP and BM pins in FlexRay transceiver must pass the ±6 kV of IEC 61000-4-2 test. The fabricated Bi-PNP devices were also tested by the system-level ESD gun under direct pin injection mode [20]. The test results of HBM and the IEC 61000-4-2 are listed in Table I.

The dependences of HBM failure voltage level and IEC failure voltage level on the size of Bi-PNP device under

TABLE I
HBM AND IEC 61000-4-2 FAILURE VOLTAGE LEVELS

Device Size	HBM (+)	HBM (-)	IEC (+)	IEC (-)
1x	4.3kV	-3.8kV	1.6kV	-1kV
2x	>8kV	-7.6kV	2.6kV	-2.1kV
3x	>8kV	>-8kV	3.4kV	-3.2kV

✧ Each failure level has been stressed three times and then bias the devices after each stress. If the leakage of DUT offsets over 10% from its original value, the DUT was judged as failure.

✧ HBM level and IEC 61000-4-2 level were initially set as 500V with voltage step of 100 V until the DUT failed after stress.

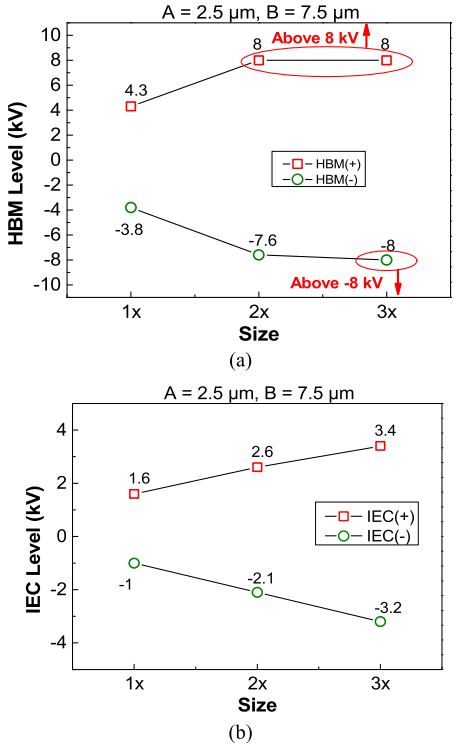

Fig. 17. Dependence of (a) HBM failure voltage level, and (b) IEC failure voltage level, on the size of Bi-PNP device under HBM ESD and IEC 61000-4-2 tests.

HBM ESD and IEC 61000-4-2 tests have been shown in Fig. 17(a) and (b), respectively. The Bi-PNP device that can pass ±6 kV HBM ESD test is the "2×" device, which has a total device layout of 144 × 300 μm^2 and drawing with finger number of 22. However, this "2×" device can only sustain the IEC 61000-4-2 stress of +2.6 and −2.1 kV. To pass the IEC 61000-4-2 stress of ±6 kV, the Bi-PNP device should be drawn with "6×" device size. Finally, from the test results of this work, the empirical correlations between them can be expressed in the following equations:

$$\text{HBM Level}(V) = \text{TLP It2} \times 2\ \text{k}\Omega \quad (1)$$

$$\text{IEC Level}(V) = \text{TLP It2} \times 0.6\ \text{k}\Omega. \quad (2)$$

The IEC 61000-4-2 failure level is about 0.6 kΩ times the It2 of ESD device, which is similar to the result of previous study [21]. In summary, Table II shows the comparisons among the fabricated Bi-PNP devices of different sizes,

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TABLE II
COMPARISONS AMONG THE PROPOSED BI-PNP WITH DIFFERENT SIZES

	Bi-Directional PNP (Bi-PNP)		
	1x Bi-PNP	2x Bi-PNP	3x Bi-PNP
Area (μm×μm)	144 × 174	144 × 300	144 × 427
Finger number	11	22	33
Width per finger	100 μm		
*Ron (Ω)	6.26	3.5	2.51
*It2 (A)	2.18	3.85	5.63
It2 / Area (μA/μm^2)	87.01	89.12	91.56
*HBM Level (kV)	4.05	7.8	>8
HBM / Area (mV/μm^2)	161.64	180.56	N/A
*IEC Level (kV)	1.3	2.35	3.3
IEC / Area (mV/μm^2)	51.88	54.4	53.67

*Because the proposed PNP are Bi-directional devices, all parameters have two measurement results on both positive and negative sides, respectively. The values in this Table of Ron, It2, HBM, and IEC are calculated on average.

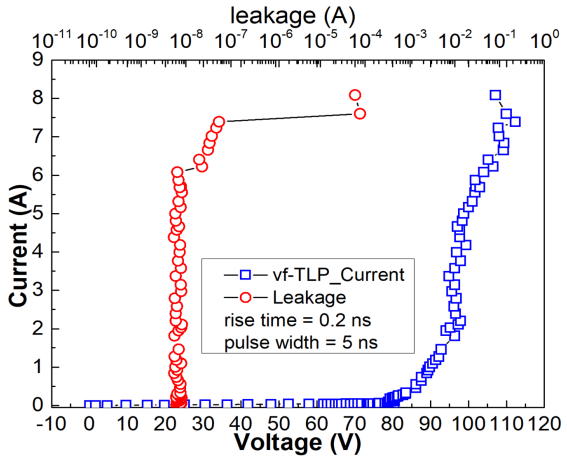

Fig. 18. Measured positive vf-TLP *I–V* curve of the Bi-PNP device with $A = 2.5$ μm and $B = 7.5$ μm.

including the area efficiency under HBM and IEC 61000-4-2 tests.

D. Transient Response

To analyze the transient response of the proposed Bi-PNP during ESD transient stress. The very fast TLP (vf-TLP) tester (Thermo Scientific Celestron) with 5-ns pulsewidth and 0.2-ns rise time is utilized to measure the vf-TLP $I–V$ curve of the proposed Bi-PNP device. The power supply (Keithley 2410) is used to bias the device after each stress so that the leakage current at 60-V bias can be observed. The measured positive vf-TLP $I–V$ curve is shown in Fig. 18. To further verify the transient response of the proposed Bi-PNP under the very fast ESD condition, the voltage and current transient waveforms corresponding to the points of vf-TLP current at 2 and 4 A are shown in Fig. 19(a) and (b), respectively. The proposed Bi-PNP can be turned on fast enough to discharge the vf-TLP

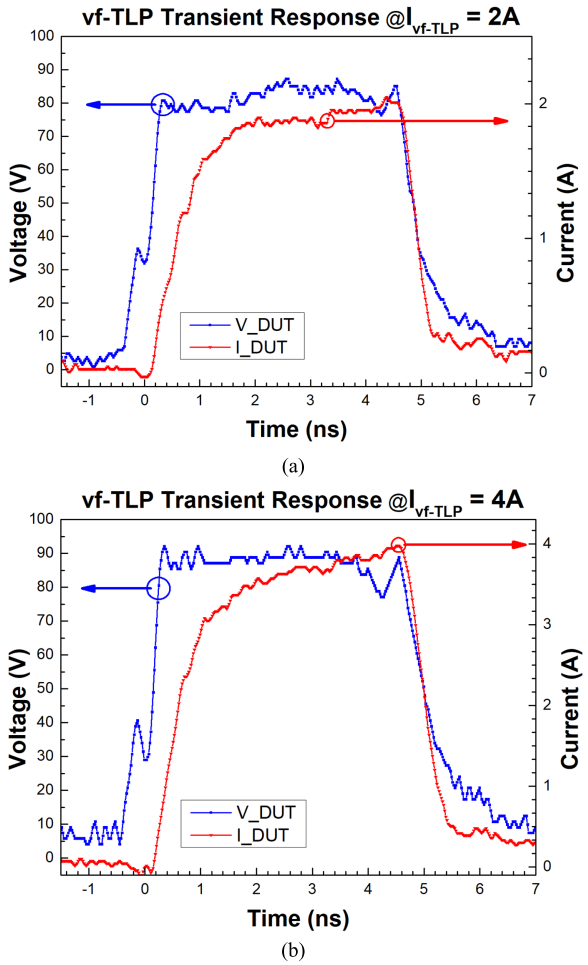

Fig. 19. Voltage and current transient waveforms corresponding to the points of vf-TLP current at (a) 2 and (b) 4 A, in Fig. 18.

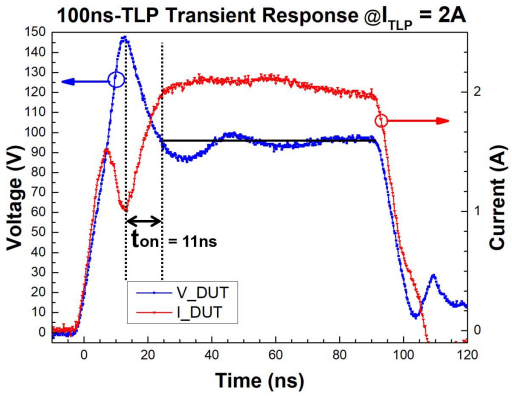

Fig. 20. Voltage and current transient waveforms corresponding to the point of TLP current at +2 A in Fig. 12 on the Bi-PNP device with $A = 2.5$ μm and $B = 7.5$ μm.

pulse, therefore the overstress voltage is clamped down to get the $I–V$ curve shown in Fig. 18.

Moreover, the voltage and current transient waveforms measured by 100-ns TLP are shown in Fig. 20, which is corresponding to the TLP current of +2 A in Fig. 12(a) on the

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TABLE III
COMPARISONS AMONG THE PROPOSED DESIGN AND PRIOR WORKS OF BI-DIRECTIONAL APPLICATIONS

Characteristic	This work	[9]	[10]	[11]	[12]	[13]	[14]
Structure	PNP-based	SCR-based	SCR-based	SCR-based	SCR-based	SCR-based	SCR-based
Turn-on Mechanism	Non-snapback	Snapback	Snapback	Snapback	Snapback	Snapback	Snapback
Process	0.15μm BCD	BiCMOS	0.5μm BiCMOS	N/A	0.18μm CMOS	0.18μm BCD	0.6μm BiCMOS
Operating voltage	± 60V	5V/20V/30V	+60V/-30V	N/A	N/A	± 40V	±8V
Trigger voltage	± 68V	± 22.55V	+60V/-30V	± 10.16V	± 16V	~ ± 55V	~ ± 15V
Holding voltage (TLP)	± 68V	± 1.55V	~ +/- 20V	± 4.64V	± 14V	± 40V	±7.5 V
Holding voltage (DC)	± 69V	N/A	N/A	N/A	N/A	N/A	N/A
Area Efficiency (ESD robustness/size)	0.09 mA/μm^2 (It2/Area)	80 V/μm (HBM/Width)	N/A	N/A	~ 20mA/μm (It2/Width)	0.15 mA/μm^2 (It2/Area)	75 mA/μm (It2/Width)
Latch-up risk	No	Yes	Yes	Yes	Yes	Yes	Yes
60-V FlexRay Applicability	Yes	No	No	No	No	No	No

Bi-PNP device with $A = 2.5$ μm and $B = 7.5$ μm. As shown in Fig. 20 with a rise time of ~10 ns in the 100-ns TLP pulse, the voltage is dropped down and the current is raised up obviously when the Bi-PNP is triggered on. The turn-on time (t_{on}) of the proposed Bi-PNP device with $A = 2.5$ μm and $B = 7.5$ μm is about 11 ns under 100-ns TLP measurement, which is marked in Fig. 20.

IV. DISCUSSION

Table III shows the comparisons among the proposed design and the other prior works of bi-directional applications. The proposed Bi-PNP is compared with other bi-directional ESD devices listed in [9], [10], [11], [12], [13], and [14], where the SCR-based ESD devices were designed to provide bi-directional path for ESD protection. The area efficiency (ESD robustness/size) among the proposed design and the prior works of bi-directional applications is also listed in Table III. However, the SCR-based devices often had obviously snapback characteristics, which would suffer the latch-up risk. The holding voltage of ESD devices must be greater than the maximum operating voltage of FlexRay applications. Even though the SCR has high ESD robustness, SCR-based devices were not suitable for FlexRay applications.

As shown in Table III, the devices in [9], [10], and [11] have high risk of latch-up concerns because their holding voltages are obviously below their operating voltages. The holding voltages of the ESD devices reported in [12], [13], and [14] somewhat equaled to their operating voltages. However, those holding voltages were measured by the 100-ns TLP. Because latch-up issue is a dc condition after power ON, the holding voltages of ESD devices should be measured under dc condition to ensure whether the device is really latch-up free, or not. As reported in [22], the snapback holding voltage of high-voltage ESD device was degraded as the increase of the pulsewidth during the TLP measurement. In this work, the holding voltages of the non-snapback Bi-PNP device measured by 100-ns TLP and curve tracer (dc condition) are 68 and 69 V, respectively. As a result, the proposed Bi-PNP is a latch-up-free device for on-chip ESD protection in the ±60 V FlexRay applications. Among the devices listed in Table III, only the proposed Bi-PNP is suitable for ±60 V FlexRay applications.

V. CONCLUSION

The Bi-PNP device for FlexRay applications had been designed, fabricated, and measured in a silicon chip. From the measured results in the given 0.15-μm BCD process, the Bi-PNP device with a spacing A of 1.25 μm and the total finger number of 66 is recommended to meet the 6-kV HBM and 6-kV IEC 61000-4-2 ESD specifications for ±60 V FlexRay applications. Overall, the proposed Bi-PNP device will be an excellent candidate for on-chip ESD protection in the FlexRay communication ICs.

ACKNOWLEDGMENT

The chip fabrication was supported by Vanguard International Semiconductor Corporation (VIS), Hsinchu, Taiwan. The authors would like to thank J.-H. Lee, S.-C. Huang, Y.-N. Jou, C.-H. Lin, Y.-J. Huang, C.-Y. Chuang, H.-F. Liao, H.-C. Chiou, C.-M. Lin, L.-Y. Hong, and T.-Y. Chang in the Device Engineering Division, VIS, for their valuable technical suggestions.

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