The Parasitic Latch-Up Path From Substrate P+ Guard Ring to the NMOS in Deep N-Well Operating With Negative Voltage Sources

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***Abstract*— For implanted neuro-modulation applications, the electrical stimulation circuits had been designed to be operating with positive and negative voltage sources. To support the circuit operation with negative voltage source, the deep n-well (DNW) layer has been added into the CMOS process to isolate the devices with negative voltage from the common grounded p-type substrate. In chip layout, the guard ring of grounded P+ diffusion is often drawn to surround the whole DNW layer for latch-up prevention and/or noise reduction. However, in the stimulation circuits operating with negative voltage sources, a parasitic latch-up path from the grounded p+ guard ring (p+ GR) to the N+ diffusion of the stacked-nMOS (STnMOS) biased at negative voltage source in a DNW may cause latch-up issue to the stimulation circuits. In this letter, such a parasitic latch-up path is first reported in the article. From the experimental results verified in a 0.18-μm 1.8-V/3.3-V CMOS process, the holding voltage (Vh) of such a parasitic latch-up path is related to the spacing between the p+ GR and the N+ diffusion of STnMOS, as well as to the series resistance that connect the isolation ring of DNW to ground. Furthermore, the magnitude of Vh is decreased when the operating temperature is increased.**

***Index Terms*— Latch-up, holding voltage, deep n-well (DNW), negative voltage supply, p+ guard ring.**

I. Introduction

THE implantable biomedical devices had been used to treat neurological disorders through functional electrical stimulation with the voltage/current stimulus patterns classified as mono-polar and bi-polar styles [1]. From the stimulus patterns, the mono-polar stimulation circuits for bi-phasic stimulation need to be supplied with positive and negative high-voltage power sources [1], [2]. In the mono-polar bi-phasic stimulator chip fabricated in a 0.18-μm 1.8-V/3.3-V CMOS process with a common grounded p-type substrate, the stacked-nMOS (STnMOS) biased at negative voltage source in a deep n-well (DNW) is needed to perform the desired negative voltage/current stimulation. The STnMOS was used to avoid voltage overstress issue for the 3.3-V NMOS's operating at the negative voltage level of −6V.

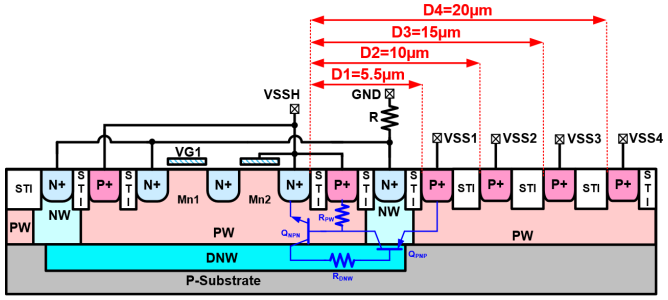

Fig. 1. The cross-sectional view to show the parasitic latch-up path and the test structure to investigate its holding voltage in a p-substrate CMOS process.

As shown in Fig. 1, the source side (N+) of STnMOS (formed by the Mn1 and Mn2 in a P-well, that is fully surrounded by a DNW and NW) is biased at VSSH (−6V) to meet the desired stimulation circuit applications. To isolate the STnMOS device operating with VSSH of −6V from the common grounded p-type substrate, the isolation ring of DNW/NW is biased at GND (0V). Some P+ guard ring (p+ GR) in the substrate was often drawn in the layout to surround the whole isolation ring of DNW/NW for latch-up prevention and/or noise reduction. However, a parasitic latch-up path exists from the grounded p+ GR of the common p-substrate, through the p-well and the isolation ring of DNW/NW, to the source side (n+ diffusion connected to VSSH) of the STnMOS. If such a latch-up path was triggered on, the turned-on low impedance p-n-p-n path from the VSS1 (0V) to VSSH (−6V) would cause malfunction to the circuit operations or even conduct huge latch-up current to burn out the chip.

In this work, the latch-up path between the p+ guard ring in the common p-substrate and the source side (n+ diffusion connected to VSSH) of STnMOS in a DNW was investigated by the test structures drawn with different layout spacings between them in silicon chip.

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II. Test Structures

The test structure used to investigate the holding voltage of this parasitic latch-up path from the p+ guard ring in the common p-substrate to the source side (n+ diffusion connected to VSSH) of STnMOS in a DNW is illustrated in Fig. 1, which was fabricated in a 0.18-μm 1.8-V/3.3-V bulk CMOS process. The different layout spacings from the anode (P+ diffusion of p+ guard ring) to the cathode (n+ diffusion connected to VSSH) of the parasitic latch-up path were drawn as 5.5 μm, 10 μm, 15 μm, and 20 μm, respectively, in the test structures.

To investigate the characteristic of the latch-up path, the curve tracer (Tek370B) is used to measure the dc I-V curve and its holding voltage (Vh) of every latch-up test structure. In addition, the grounded isolation ring of DNW/NW in the CMOS ICs may also cause another possible latch-up path from the neighbor PMOS devices (that biased at VDD or VCC) to this grounded DNW [3]. Due to the latch-up path in adjacent NWs at different potentials, a series resistance of $\sim$ 200 ohm was empirically suggested by foundry to connect the isolation ring of DNW/NW to its bias voltage source for overcoming the possible latch-up issue. Therefore, the grounded DNW/NW in the latch-up test structure was connected to GND (0V) through different series resistances (0 Ω, 40 Ω, 50 Ω, 100 Ω, 1 kΩ, and floating, respectively) during the dc I-V curve measurement.

III. Experimental Results

The dc I-V characteristics of the latch-up test structures are measured (from P+ at VSS1 $\sim$ VSS4 to the N+ at VSSH with the different spacings) by the curve tracer. The P+ (VSS1 $\sim$ VSS4) node is grounded (0V), the DNW is also grounded via a series resistance, and a negative voltage is swiping at the N+ (VSSH) node to measure the I-V curves in the negative domain, which is corresponding to the application scenario of the stimulation circuit with negative voltage source. Moreover, the latch-up test structures are also measured under different temperatures (25°C, 85°C, and 125°C) to investigate the temperature effect on them. The latch-up holding voltage (Vh) in this study was defined as the minimum voltage level that maintains the turned-on behavior of the latch-up path. Thus, the last point in the measured I-V curve that leaving from the snack-back holding region is defined as the Vh of the latch-up path.

The measured dc I-V characteristics of the parasitic latch-up path from VSS1 to VSSH with the anode-to-cathode spacing (D1) of 5.5μm, at the temperature of 25°C, and under different series resistance connected the DNW to ground, are shown in Fig. 2(a). When the isolation ring of DNW is directly biased to GND (via series resistance of 0Ω), the Vh of the latch-up path in the test structure is −10.64 V. But, when the isolation ring of DNW is biased to GND via different series resistances of 40Ω/50Ω/100Ω/1kΩ/floating, the Vh of the latch-up path is varying from −2.28 V to −2.04 V. Because the magnitude of Vh of the parasitic latch-up path was less than the magnitude of voltage difference between VSS1 (0V) and VSSH (−6V), the parasitic p-n-p-n path in the stimulation circuit with negative voltage source (−6V) may cause latch-up issue.

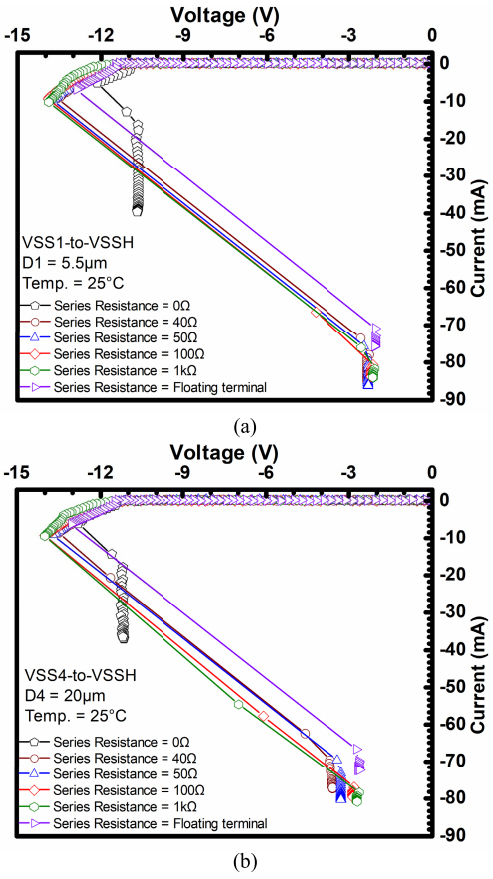

Fig. 2. The measured dc I-V characteristics of the parasitic latch-up paths in test structures at the temperature of 25°C from (a) VSS1 to VSSH of 5.5μm, and (b) VSS4 to VSSH of 20μm, with different series resistances.

The measured dc I-V characteristics of the latch-up path in the test structure from VSS4 to VSSH with the anode-to- cathode spacing (D4) of 20μm are shown in Fig. 2(b), where the Vh of the latch-up path is varying from −2.67 V to −3.7V at the temperature of 25°C under different series resistances to connect the DNW. The magnitude of Vh is raised while the spacing from the p+ GR to the DNW is increased. Furthermore, the magnitude of Vh is reduced sharply while the series resistance used to connect the isolation ring of DNW to ground is increased.

The dependences of Vh of the latch-up path on the anode-to-cathode spacing in the test structures under different temperatures (25°C, 85°C, and 125°C) with the series resistance of 40 Ω are summarized in Fig. 3. The magnitude of Vh is increased by increasing the anode-to-cathode spacing. In addition, the magnitude of Vh is decreased while the operating temperature is increased. To get a latch-up free result (the magnitude of Vh to be greater than 6V), the corresponding anode-to-cathode spacing can be estimated by heterodyning the dependence trend in Fig. 3. Based on the dependence trend of each line, the anode-to-cathode spacing should be greater than 43μm, 48μm, and 58μm under the temperatures of 25°C, 85°C, and 125°C, respectively, to get a latch-up free result. However, it is difficult to adopt as a solution because there is an area penalty.

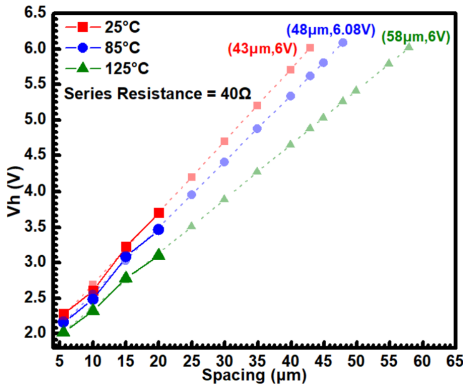

Fig. 3. The dependences of holding voltage (Vh) of the latch-up path on the anode-to-cathode spacing in the test structures under different temperatures (25°C, 85°C, and 125°C) with the series resistance of 40Ω.

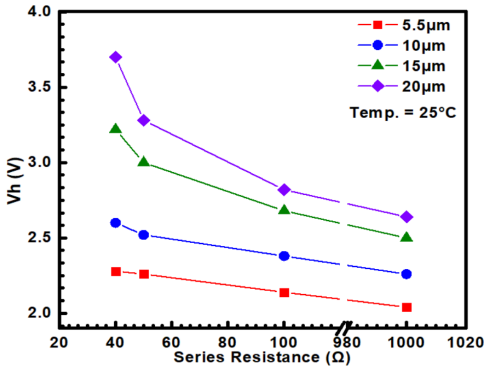

Fig. 4. The dependences of holding voltage (Vh) on the series resistance that connect the isolation ring of DNW to ground in the test structures under different anode-to-cathode spacings (5.5μm, 10μm, 15μm, and 20μm) in the test structures at the temperature of 25°C.

The dependences of holding voltage (Vh) on the series resistance that connect the isolation ring of DNW to ground in the test structures under different anode-to-cathode spacings (5.5μm, 10μm, 15μm, and 20μm) at the temperature of 25°C are summarized in Fig. 4. The magnitude of Vh is decreased while the series resistance is increased. Thus, the parasitic p-n-p-n path in the stimulation circuit with negative voltage source (-6V) may cause latch-up issue.

IV. Discussion

Conventionally, the P+ guard rings in the p-type substrate were often drawn and added into the chip layout to surround the whole DNW/NW for better latch-up prevention. On the contrary, in this study, the grounded P+ guard rings that surrounding the whole DNW/NW region, in which some NMOS devices operating with negative voltage source, do cause the parasitic latch-up path in the stimulator chip. The closer the P+ guard rings placed to the DNW/NW region, the lower holding voltage of the parasitic latch-up path to cause latch-up issue in the stimulation circuits.

If the isolation ring of DNW is directly connected to ground (with the series resistance of 0Ω), the magnitude of Vh can be greater than the voltage difference across the p-n-p-n structure to get a latch-up free result. But, such a directly-grounded DNW may cause another latch-up path when some PMOS devices biased with VDD or VCC is drawn close to it [3].

Therefore, while the CMOS ICs with the circuits operating at negative voltage levels that surrounded by DNW in a common grounded p-type substrate, the parasitic p-n-p-n structure in the chip layout to cause latch-up issue must be found out, and then the correct guard ring style with suitable layout spacing should be applied to overcome latch-up issue.

V. Conclusion

The parasitic latch-up path between the p+ guard ring in the common p-substrate and the source side (n+ diffusion connected to VSSH) of STnMOS in a DNW has been investigated by the test structures fabricated in a 0.18-μm 1.8-V/3.3-V CMOS process. From the experimental results, the magnitude of Vh of the latch-up path is decreased, while the anode-to-cathode spacing is decreased, the temperature is increased, or the series resistance that connect the isolation ring of DNW to ground is increased. With the magnitude of Vh lower than the voltage difference across the p-n-p-n structure, the circuit layout with such a parasitic latch-up path has high risk to latch-up issue. Thus, the circuit designers and the layout engineers should pay attention to the parasitic latch-up paths reported in this work, especially when their circuits are designed to be operating with negative voltage sources in a grounded P-type substrate. Moreover, it will be better that the corresponding design rules (layout rules) to prevent this kind of parasitic latch-up issue can be provided by the foundry.

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