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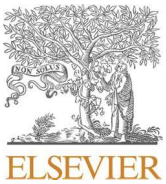

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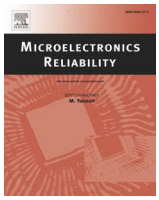

Research Paper

Investigation of safe operating area and behavior of unclamped inductive switching on 4H-SiC VDMOSFET

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ABSTRACT

The electrical safe operating area (eSOA) of the transmission-line pulse (TLP) test and the electrical behavior of the unclamped inductive switching (UIS) test on a 4H-SiC 600-V vertical double-implanted MOSFET (VDMOSFET) were investigated in this work. The snapback phenomenon of the 100-ns and 1000-ns TLP I-V curves can be inferred to be the triggering on of the parasitic BJT in the VDMOSFET. Moreover, the holding voltage of the 1000-ns TLP I-V curve was lower than that of the 100-ns TLP I-V curve, which can be attributed to the severer self-heating effect in the 1000-ns TLP test. In the UIS test, different experiments were conducted by varying pulse widths, gate resistances, and external inductors. The longer the falling time of the gate bias applied to the VDMOSFET, the lower the overshooting peak voltage on the drain side will be. Furthermore, the methods for improving the eSOA characteristic and the UIS ruggedness were also discussed and summarized in this work.

1. Introduction

SiC devices have been researched for more than 20 years, but have become popular recently due to some high-power applications, such as electric vehicles, charging stations, and equipment of renewable energy. Since SiC is one of the wide-bandgap semiconductor materials, compared with the Si-based device, the SiC device possesses higher blocking voltage and better thermal stability [1,2]. This is the reason why SiC is used widely in systems which operate under high-voltage and high-current conditions. Recently, a monolithic single chip fabricated in the same SiC process was proposed which contains the gate-driving circuit and the power MOSFET [3]. Because the whole circuit system was integrated into a monolithic SiC chip, the thermal stability will be substantially improved. Moreover, with no need for the integration of the Si-based gate driver and the SiC-based power MOFSET, the cost of heterogeneous integration will be also reduced. However, for the commercialization of the product, there is still a long way to go. Moreover, in order to fulfill the commercialization of the product, it is necessary to perform the reliability test.

For such high-power applications, the electrical safe operating area (eSOA) and unclamped inductive switching (UIS) ruggedness are the typical methods to test whether the power device is robust or not. Since there is overshooting or ringing on the drain of the power MOSFET during normal operation, designers need to guarantee that the switching locus of the power device is within the eSOA boundary. Through the TLP test with different pulse widths, the eSOA boundary of the power MOSFET under transient behavior can be obtained, which is helpful for designers to develop the power device or power management integrated circuit in the developing stage.

Since the external inductor is often connected to the drain of the power MOSFET in the high-power module as shown in Fig. 1, it is necessary to characterize the UIS ruggedness [4]. For example, in the traction inverter of the electric vehicle, when the gate of the device is turned on, there is a large current flowing into the drain of the power MOSFET, which can be referred to Fig. 1(a). When the gate is turned off, because the current cannot drop to zero immediately, it will flow out of the inductor continuously. Therefore, the V_{DS} voltage of the power MOSFET will be raised to a high level, and the device will be over-stressed for a short period. Once the V_{DS} voltage is high enough, the parasitic BJT of the power MOSFET will be triggered on, which can be referred to Fig. 1(b). With the large current flowing into the parasitic BJT, the device will be eventually damaged. As a result, UIS test is typically used to simulate the situation, and the switching ruggedness in the time domain can be investigated. Moreover, the pulse width of the overshooting peak V_{DS} voltage would be changed in different system topologies. Therefore, the TLP eSOA characteristics with different pulse widths are helpful for circuit designers to optimize their designs.

In the past, the eSOA characteristic of high voltage devices fabricated

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