Latchup Risk in a 4H-SiC Process

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***Abstract*— This is the first study related to the latchup issue in the SiC process. In this work, the latchup risk and the holding voltage of the parasitic latchup path have been investigated. The dc holding voltage of the parasitic latchup is only 14.9 V, which is below the voltage rating (20 V) of the devices. The holding voltage measured by the transmission line pulse (TLP) system decreases when the pulsewidth increases, which can be attributed to the self-heating effect on the device. Moreover, the holding voltage measured by TLP decreases as the temperature increases. The methods to prevent latchup events are summarized in this brief. The methods can be divided into two parts. One is the process solution, and the other is the layout solution. Therefore, the design rules for latchup prevention in the SiC process must be developed.**

***Index Terms*— Holding voltage, latchup, SiC, SiC-based integrated circuits (ICs).**

I. Introduction

WIDE bandgap semiconductor devices have gained much attention in recent years due to emerging high-power applications, such as electric vehicles, data centers, green-power infrastructures, and railway electric tractions. SiC is one of the most promising wide bandgap materials because of its high breakdown voltage and excellent thermal stability. In order to fulfill the commercialization of SiC products, the SiC-based integrated circuits (ICs) are the critical direction of research and development. Therefore, in recent years, some prior arts about the monolithic ICs fabricated by the 4H-SiC process have been reported [1], [2], [3]. However, the aforementioned high-power electronic equipment usually operates in high-voltage and high-temperature environments. Hence, the reliability specification of these products is stricter than that of consumer products. JESD78F is the typical standard specified by the joint electron tube engineering council (JEDEC) used to evaluate the latchup immunity of IC products [4]. As a result, SiC-based ICs are also required to pass the latchup test.

The latchup mechanism and the solutions for latchup prevention in Si-based ICs have been well studied [5], [6], [7], [8], [9]. The latchup issues are critical because they will cause the circuit to be in some wrong conditions, such as functional faults or abnormal leakage currents. The worst case is that the circuit will be even burned out. It is essential to consider latchup prevention when circuit designers design the circuit and implement the chip layout. Therefore, the design rules for latchup prevention had been well provided by foundry companies. Nevertheless, latchup-related research in SiC-based ICs or SiC processes has never been reported.

This work is the first latchup-related study in the SiC process and SiC-based ICs so far. The latchup risk can be evaluated by the holding voltage (V_h), which can be measured from the parasitic p-n-p-n path in the CMOS structure. With the dc measurement and transmission line pulse (TLP) system measurement, the snapback phenomenon can be observed. Furthermore, the correlation between V_h, the TLP pulsewidth, and the device temperature was also investigated in this work. All of the experimental results indicate that there is indeed latchup risk in the SiC-based ICs, especially in high-temperature environments.

TABLE I
DOPING LEVELS OF THE 4H-SIC PROCESS

Implantation	Doping element	Total dose (#/cm^2)
N-well	nitrogen	9.5×10^{12}
P-well	aluminum	2.76×10^{13}
N+	phosphorus	2.4×10^{15}
P+	aluminum	6.8×10^{15}

II. Latchup Test Structure

The test structure used in this work is a CMOS structure, which consists of a gate-V_{DD} PMOS (GDPMOS) and a gate-grounded (GGNMOS). In the given 4H-SiC process, the minimum gate length of nMOS/pMOS is 0.5 μm. Because latchup behavior is strongly related to the process parameters, the doping levels of different layers in this process are listed in Table I.

Fig. 1(a) shows the cross-sectional view of the CMOS structure with its parasitic latchup path from the pMOS source to the nMOS source. The schematic and the parasitic silicon-controlled rectifier (SCR) structure are shown in Fig. 1(b) and (c), respectively. When the noise current flowing into the base of the parasitic NPN or PNP BJT (p-well or n-well) is large enough, the parasitic BJT is turned on. With the structure of the positive feedback shown in Fig. 1(c), once the parasitic BJT is turned on, the latchup event occurs, and

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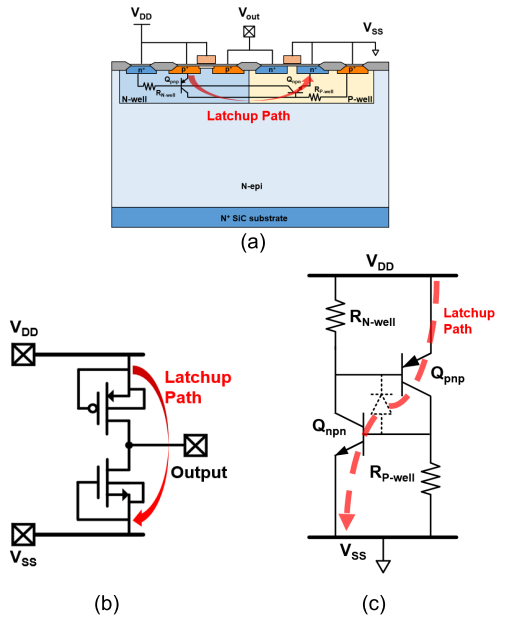

Fig. 1. (a) Cross-sectional view, (b) schematic, and (c) parasitic SCR structure with its corresponding latchup path in the CMOS structure.

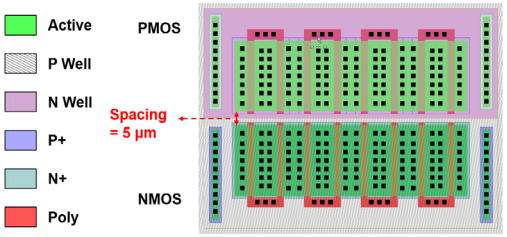

Fig. 2. Layout view of the CMOS structure with GDPMOS and GGNMOS.

the IC will finally be burned out due to the large current. Fig. 2 shows the layout diagram of the CMOS structure. The W/L of each finger in GDPMOS and GGNMOS is 25/1.5 μm, and the finger number is 8. Therefore, the total width is 200 μm. Because the minimum spacing between nMOS and pMOS is 5 μm, the latchup test structure was drawn with this parameter to investigate its latchup risk. Therefore, the spacing between the anode and the cathode of the parasitic P+/N-well/P-well/N+ path is 5 μm. The fabrication steps of nMOS and pMOS in the 4H-SiC process can be referred to [3], where the 20-V nMOS and pMOS devices can be integrated with the high-voltage SiC device together. Nominal V_{DS} and V_{GS} are targeted to 20 V. Therefore, the criterion for the latchup risk is whether the holding voltage (V_h) is below 20 V or not.

III. Latchup I–V Characteristics

A. Measured by Curve Tracer

The dc holding voltage (V_h) of the parasitic latchup path is measured by the curve tracer (Tektronix Tek370B) under a low-frequency and half-sinusoidal voltage waveform. The measured I–V curves are shown in Fig. 3(a) and (b). Before the device breakdown, the I–V curve is shown in Fig. 3(a). Because the critical electric field in SiC devices is higher

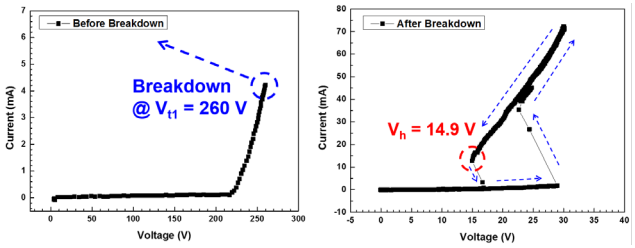

Fig. 3. I–V curves (a) measured by the curve tracer before the device breakdown and (b) remeasured by the curve tracer after the device breakdown.

than that in Si devices, the trigger voltage (V_{t1}) of the parasitic latchup path is 260 V. After the device breakdown, the I–V curve was remeasured and shown in Fig. 3(b), which performed the snapback phenomenon. The holding voltage is 14.9 V, and the trigger voltage is reduced to only 28.9 V. The device characteristic was changed after the device breakdown due to the large current flowing into the parasitic latchup path, because the breakdown current flowed through the reverse junction of NW/PW to cause damage on the NW/PW junction. Hence, after the device breakdown, the leakage current was large enough to trigger the parasitic latchup path.

B. Measured by TLP

Although the snapback phenomenon can be observed by curve tracer measurement, the TLP is used to acquire a more stable I–V curve. Fig. 4 shows the TLP I–V curves under different TLP pulse widths. All of these measurements were implemented at room temperature (25 °C). When the TLP pulse widths are 100, 500, and 1000 ns, the holding voltages (V_h) are 62.6, 47.8, and 32.8 V, respectively. Therefore, with the increment of TLP pulsewidth, the holding voltage is decreased. This phenomenon can be attributed to the effect of temperature on the device [10], [11]. According to the Wunsch–Bell model, the simplified temperature model $T(0, \tau)$ under the source of a rectangular pulse with duration τ can be referred to (1). q_0 is the constant strength of the rectangular pulse. D is the thermal diffusivity. K is the thermal conductivity. ρ_d is the mass density. c_p is the specific heat

$$\text{If } t \le \tau,\ T(0,\tau) = \left(\frac{q_0}{\sqrt{\pi D}}\right)\sqrt{t},\ \text{where } D = \left(\frac{K}{\rho_d c_p}\right). \tag{1}$$

As the TLP pulsewidth increases, the self-heating effect becomes more severe. As a result, the device temperature increases with longer TLP pulsewidth, and the current gain (β gain) of the parasitic BJT also increases, which results in lower V_h eventually.

In order to further analyze the correlation between TLP pulsewidth, dc measurement, and V_h, the corresponding data were drawn in Fig. 5. For TLP pulsewidth of 100, 500, and 1000 ns, V_h shows a linear correlation, but all of V_h extracted from TLP measurement is above 20 V. However, for the dc

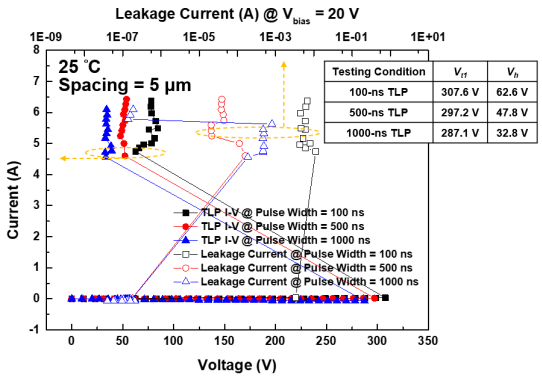

Fig. 4. *I–V* curves of the TLP measurement with the pulsewidth of 100, 500, and 1000 ns, respectively.

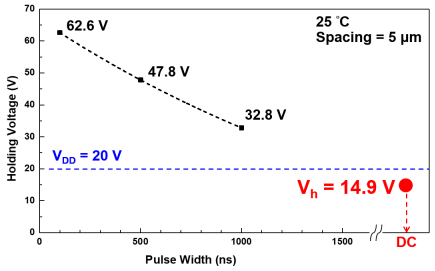

Fig. 5. Correlation between TLP pulsewidth, dc measurement, and holding voltage (V_h).

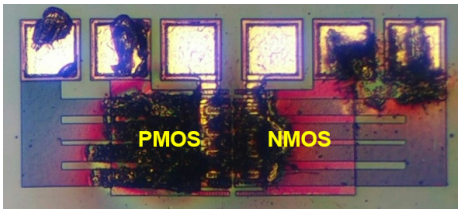

Fig. 6. Die image of the latchup failure photographed by the optical microscope.

measurement, V_h is only 14.9 V, which is less than 20 V. Therefore, there is latchup risk on the CMOS structure in the SiC-based ICs.

C. Failure Analysis

The die image with the latchup failure photographed by the optical microscope is shown in Fig. 6. The measuring condition was the TLP test with a pulsewidth of 1000 ns at room temperature. The die image was photographed after the 1000-ns TLP measurement at the stop point with the current of ~6 A. The device was burned out due to the large current flowing into the parasitic latchup path in the CMOS structure during the latchup period. The latchup mechanism can indeed cause unrecoverable damage to the SiC devices. Thus, in order to avoid the dangerous situation in the real application, it is necessary to prevent SiC ICs from causing latchup events.

D. Measured by TLP at Different Temperatures

Moreover, because power electronics often operate in high-temperature environments, it is necessary to verify V_h under

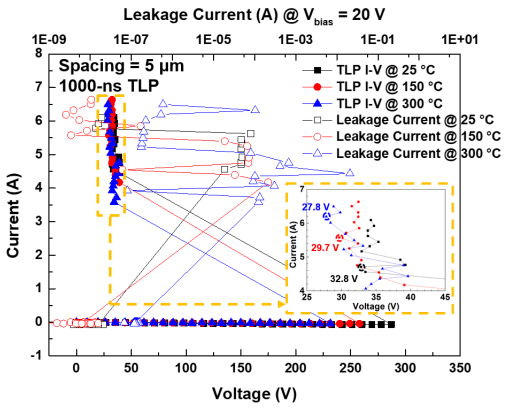

Fig. 7. *I–V* curves of the TLP measurement at 25 °C, 150 °C, and 300 °C, respectively.

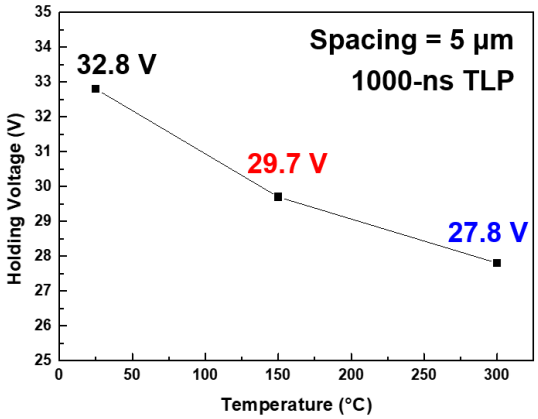

Fig. 8. Correlation between temperature and holding voltage (V_h).

high-temperature conditions. Fig. 7 shows the 1000-ns TLP *I–V* curves with different temperatures. At 25 °C, 150 °C, and 300 °C, V_h is 32.8, 29.7, and 27.8 V, respectively. Therefore, as the temperature increases, V_h gradually degrades, which can be referred to Fig. 8. The interpretation of physical mechanisms can be referred to an early published article [12]. When the temperature increases, the minority carrier lifetime increases, which can cause an increase in the current gain of SiC bipolar devices [12].

In addition, based on the experimental results mentioned in the previous section, it is predictable that the dc V_h under the high-temperature condition will be even lower, and the risk of latchup events in the actual application will be higher. Therefore, in order to design more robust SiC-based ICs, the design rules for preventing latchup are urgently needed.

IV. Methods to Prevent Latchup

Because the prevention concept in SiC-based ICs is similar to that in Si-based ICs, some methods to prevent latchup, which have been proposed in Si-based ICs, can also be applied in SiC-based ICs. The common methods to improve latchup immunity are summarized in this section.

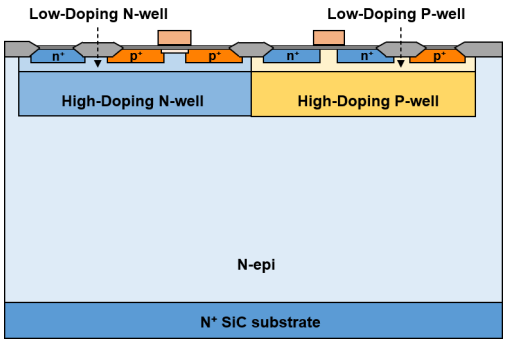

Fig. 9. Schematic of the CMOS structure with retrograde well.

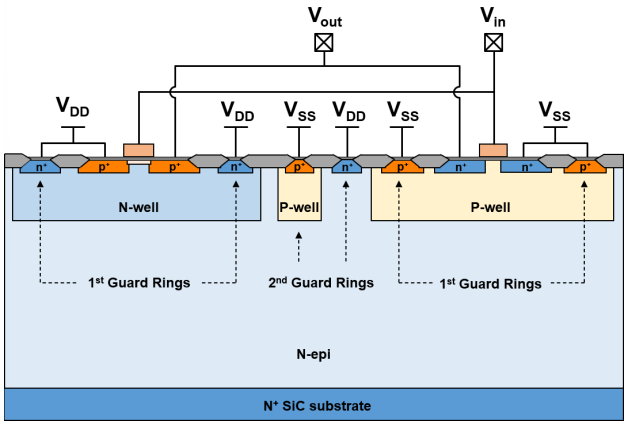

Fig. 10. Schematic of the CMOS structure surrounded by double guard rings.

A. Retrograde Well

The schematic of the CMOS structure with a retrograde well is shown in Fig. 9. The prior art of using the retrograde well to enhance the latchup immunity in the Si process can be referred to [13]. Reducing the resistance of the p-well ($R_{\mathrm{p-well}}$) and the resistance of the n-well ($R_{\mathrm{n-well}}$) is helpful to avoid mistriggering the parasitic lateral NPN BJT and vertical PNP BJT. Because the parasitic SCR structure with smaller $R_{\mathrm{p-well}}$ and $R_{\mathrm{n-well}}$ needs larger noise currents in the n-well and p-well to turn on the parasitic BJT, the latchup immunity can be improved. Moreover, because smaller $R_{\mathrm{p-well}}$ and $R_{\mathrm{n-well}}$ result from the high doping concentration, the current gain of parasitic BJT can be reduced. This is also helpful for reducing the latchup risk.

However, the threshold voltage will be increased due to the high doping concentration, which is unsuitable for real applications. Hence, the retrograde well is introduced to keep a lower doping concentration in the channel region but generate a higher doping concentration in the deeper bulk region. With a lower doping concentration in the channel region, the threshold voltage can be decreased.

B. Increasing Anode-to-Cathode Spacing

Based on the dc holding voltage measured by the curve tracer, which is lower than the voltage rating of 20 V, enhancing the dc holding voltage to a level higher than 20 V is an effective way to prevent latchup. The easiest way to enhance the holding voltage is to increase the anode-to-cathode spacing between the source of pMOS and the source of nMOS. Hence, in order to develop more robust SiC-based ICs, the design rules about the anode-to-cathode spacing should be developed. However, the area of the chip will be increased while enhancing the spacing. Therefore, the tradeoff between the latchup immunity and the cost of the chip must be taken into consideration.

C. Using Guard Rings

Because latchup events occur when the noise current in the n-well and p-well is large enough to trigger the parasitic latchup path, reducing the noise current is also an effective way to enhance the latchup immunity of SiC-based ICs. The prior arts about using the double guard ring to enhance the latchup immunity in the Si process can be referred to [14] and [15]. Fig. 10 shows the schematic of the CMOS structure surrounded by double guard rings. By surrounding the device with guard rings, the majority carriers are precollected by guard rings before they cause a voltage drop in the well region or inject into the base region of the parasitic BJT. N+/P+ of the second guard ring connected to $V_{\mathrm{DD}}/V_{\mathrm{SS}}$, which can absorb the electron/hole noise current, respectively.

Basically, for the core circuit of the IC, it is necessary to use the single guard ring to define the bias of the n-well and the p-well and prevent the noise current from flowing into the n-well and p-well. However, the input–output (I/O) cell of the IC is more susceptible to the noise current than the core circuit. Therefore, it is recommended to use the second guard ring to guarantee the capability of absorbing the noise current. By surrounding the pMOS and nMOS of the I/O cell with the double guard rings, the latchup immunity of the I/O cell can be substantially enhanced.

V. Conclusion

The holding voltage of the parasitic latchup path inherent in the CMOS structure of a 4H-SiC process has been investigated in this work. With the TLP measurement under different pulse widths, V_h decreases with the pulsewidth increasing because of the self-heating effect. Moreover, V_h decreases with the increase in temperature. From the dc measurement by curve tracer, the snapback characteristic appears after the device breakdown, and V_h is only 14.9 V. Therefore, the latchup risk indeed exists in SiC-based ICs with a voltage rating of 20 V. The methods for improving latchup immunity of SiC-based ICs are summarized in this work. Hence, the design rules for preventing latchup issues in SiC-based ICs should be developed when the corresponding SiC process is given.

References

[1] C.-L. Hung, B.-Y. Tsui, T.-K. Tsai, L.-J. Lin, and Y.-X. Wen, "Design, process, and characterization of complementary metal-oxide-semiconductor circuits and six-transistor static random-access memory in 4H-SiC," *ECS J. Solid State Sci. Technol.*, vol. 11, no. 4, Apr. 2022, Art. no. 045001, doi: 10.1149/2162-8777/ac6119.

[2] B.-Y. Tsui, T.-K. Tsai, C.-L. Hung, and Y.-X. Wen, "Design and characterization of the junction isolation structure for monolithic integration of planar CMOS and vertical power MOSFET on 4H-SiC up to 300 °C," in *IEDM Tech. Dig.*, Dec. 2022, pp. 9.3.1–9.3.4, doi: 10.1109/IEDM45625.2022.10019434.

[3] B. Y. Tsui et al., "First integration of 10-V CMOS logic circuit, 20-V gate driver, and 600-V VDMOSFET on a 4H-SiC single chip," in *Proc. IEEE 34th Int. Symp. Power Semiconductor Devices ICs (ISPSD)*, Vancouver, BC, Canada, May 2022, pp. 321–324, doi: 10.1109/ISPSD49238.2022.9813677.

[4] *IC Latch-Up Test, JEDEC Solid State Technology Association*, JEDEC Standard JESD78F, 2022.

[5] R. R. Troutman, *Latchup in CMOS Technology: The Problem and Its Cure*. Norwalk, MA, USA: Kluwer Academic, 1986.

[6] S. H. Voldman, *Latchup*. Hoboken, NJ, USA: Wiley, 2007.

[7] M.-D. Ker and S.-F. Hsu, *Transient-Induced Latchup in CMOS Integrated Circuits*. New York, NY, USA: Wiley, 2009.

[8] M.-D. Ker and C.-Y. Wu, "Modeling the positive-feedback regenerative process of CMOS latchup by a positive transient pole method. I. Theoretical derivation," *IEEE Trans. Electron Devices*, vol. 42, no. 6, pp. 1141–1148, Jun. 1995, doi: 10.1109/16.387249.

[9] M.-D. Ker and C.-Y. Wu, "Modeling the positive-feedback regenerative process of CMOS latchup by a positive transient pole method. II. Quantitative evaluation," *IEEE Trans. Electron Devices*, vol. 42, no. 6, pp. 1149–1155, Jun. 1995, doi: 10.1109/16.387250.

[10] D. L. Lin, "Thermal breakdown of VLSI by ESD pulses," in *Proc. 28th Annu. Rel. Phys. Symp.*, Mar. 1990, pp. 281–287, doi: 10.1109/RELPHY.1990.66101.

[11] W.-Y. Chen, M.-D. Ker, and Y.-J. Huang, "Investigation on the validity of holding voltage in high-voltage devices measured by transmission-line-pulsing (TLP)," *IEEE Electron Device Lett.*, vol. 29, no. 7, pp. 762–764, Jul. 2008, doi: 10.1109/LED.2008.2000910.

[12] S.-H. Ryu, A. K. Agarwal, R. Singh, and J. W. Palmour, "1800 V NPN bipolar junction transistors in 4H-SiC," *IEEE Electron Device Lett.*, vol. 22, no. 3, pp. 124–126, Mar. 2001, doi: 10.1109/55.910617.

[13] A. G. Lewis, R. A. Martin, T.-Y. Huang, J. Y. Chen, and M. Koyanagi, "Latchup performance of retrograde and conventional n-well CMOS technologies," *IEEE Trans. Electron Devices*, vol. ED-34, no. 10, pp. 2156–2164, Oct. 1987, doi: 10.1109/t-ed.1987.23211.

[14] M.-D. Ker and W.-Y. Lo, "Methodology on extracting compact layout rules for latchup prevention in deep-submicron bulk CMOS technology," *IEEE Trans. Semiconductor Manuf.*, vol. 16, no. 2, pp. 319–334, May 2003, doi: 10.1109/TSM.2003.811885.

[15] C.-T. Dai and M.-D. Ker, "Optimization of guard ring structures to improve latchup immunity in an 18 V DDDMOS process," *IEEE Trans. Electron Devices*, vol. 63, no. 6, pp. 2449–2454, Jun. 2016, doi: 10.1109/TED.2016.2549598.