Design of GaN-on-Silicon Power-Rail ESD Clamp Circuit With Ultralow Leakage Current and Dynamic Timing-Voltage Detection Function

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***Abstract*— A power-rail electrostatic discharge (ESD) clamp circuit for monolithic GaN-based integrated circuits (ICs) with ultralow leakage current and dynamic timing-voltage detection function was proposed, which has been successfully verified in a 0.5-μm GaN-on-Si process. The standby leakage current is only 0.8 nA. With the voltage detection, the proposed ESD clamp circuit can only be triggered by ESD events, and cannot be falsely triggered during fast power-on conditions. The experimental results demonstrate that the human-body-model (HBM) ESD robustness of the proposed design can be achieved over 6 kV. The triggered voltage of the ESD clamp circuit is flexible by adjusting the number of diode-connected high electron mobility transistors (HEMTs), so it can be utilized in different voltage ratings of V_{CC}.**

***Index Terms*— Electrostatic discharge (ESD), enhancement-mode high electron mobility transistor (E-HEMT), ESD protection, GaN, HEMT, power-rail ESD clamp circuit.**

I. Introduction

THE integrated circuits (ICs) fully integrated into a monolithic chip in a GaN process have been developed recently for high-power applications [1], [2], [3], [4]. Hence, considering the completeness of the system integration, the GaN-based ICs are promising components for power electronics. However, there are always challenging quality and reliability issues in new technologies, and electrostatic discharge (ESD) is one of the most critical issues in mass production. In the past, the ESD protection design in the Si-based technology has been widely researched for many years. The solution of the whole-chip ESD was also proposed in the previous study, and the power-rail ESD clamp circuit plays a vital role in whole-chip ESD protection [5], [6].

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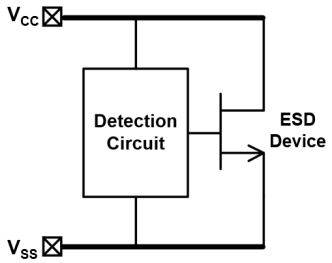

Fig. 1. Schematic of the power-rail ESD clamp circuit.

The schematic of the power-rail ESD clamp circuit is shown in Fig. 1. It contains a primary ESD device to discharge large ESD currents and a detection circuit to detect ESD events. The detection circuit can be divided into two categories. One is the timing detection function, which can be realized by the *CR*-coupling circuit or the *RC*-inverter. The other one is the voltage-level detection function, which can be realized by the diode string. For the timing detection function, the circuit can differentiate between the normal power-on conditions and the ESD conditions. The rise time of the voltage waveform on V_{CC} during normal power-on conditions is around 0.1∼1 ms, while the rise time of the ESD voltage waveform is generally around 2∼10 ns. During normal operating conditions, the gate bias of the ESD device will be kept at a low level, and the standby leakage can be kept very small. Through the suitable design of the *RC* time constant, the gate of the primary ESD device can be biased to a high-voltage level to discharge the ESD current during the ESD events. For the voltage-level detection function, there is a diode string in series with a resistor between V_{CC} and V_{SS}. During normal operating conditions, the diode string is kept off, and there is no voltage drop on the resistor, so the standby leakage of the ESD device can be kept very small. During the ESD events, the voltage level on the V_{CC} power line is large enough to turn on the diode string, and a voltage drop across the resistor will be generated to turn on the primary ESD device. Finally, the ESD currents can be discharged. However, the diode string suffers a large standby leakage current during normal operating conditions.

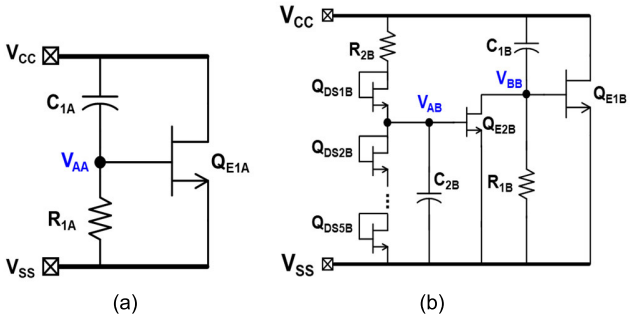

Fig. 2. Schematic of the prior arts of (a) *CR*-coupling circuit in [13] and (b) modified *CR*-coupling circuit in [14].

In addition, the rise time of V_{CC} during fast power-on conditions is in the order of several ten ns or even faster in some applications, such as hot plug and envelope tracking [7], [8]. In these applications, the *CR*-coupling circuit or the *RC*-inverter will be falsely triggered since they cannot distinguish the ESD events and the fast power-on events by the rise time detection and will cause large transient leakage currents during fast power-on conditions. Although the power-rail ESD clamp circuits against false triggering during fast power-on conditions have been researched in the Si-based process [8], there is no corresponding research in the GaN-based process. Recently, the power-rail ESD clamp circuits realized in the GaN-based process have been researched [9], [10], [11], [12], [13], [14]. However, these prior arts suffer either dc standby leakage current or transient leakage current. In prior arts [9], [10], [11], the diode strings will cause large dc standby leakage currents. In prior arts [12], [13], [14], the *CR*-coupling circuits will cause large transient leakage currents during fast power-on conditions.

Therefore, the proposed new design with a timing-voltage detection function not only possesses ultralow standby leakage current but also prevents transient leakage current during fast power-on conditions. The test chip was fabricated in a 0.5-μm GaN-on-Si technology. This study carefully verified the proposed design through many methods, including normal power-on conditions, fast power-on conditions, transmission-line-pulse (TLP) measurement, and human-body-model (HBM) test. Finally, the experimental results show that the proposed new design not only demonstrates robust ESD levels but also possesses ultralow leakage current. Hence, the proposed design is a promising circuit structure for whole-chip ESD protection in GaN-based ICs.

II. Circuit Design and Testkey Planning

A. Prior Arts Design

In order to compare the standby leakage current and transient leakage current with the prior arts in [13] and [14], the test structures were designed and verified in this study. One of the prior arts is the *CR*-coupling circuit, and the schematic is shown in Fig. 2(a). The circuit operations can be categorized into three conditions to systematically analyze the power-rail ESD clamp circuit. One is the normal power-on condition, another is the fast power-on condition, and the other is the ESD zapping condition. During normal power-on conditions, the rise time of voltage on V_{CC} is about 0.1∼1 ms. The *dV/dt* displacement current induced by the coupling capacitor C_{1A} will create a voltage drop V_{AA} across R_{1A}, and a leakage current will be induced. During fast power-on conditions, the rise time of the voltage on V_{CC} is in the order of 10 ns. Due to the higher *dV/dt*, the higher voltage drop V_{AA} across R_{1A} will result in a larger leakage current. After V_{CC} is powered to a 6-V steady state, the node V_{AA} will be kept at a low-voltage level to turn off the primary ESD device Q_{E1A}, and the standby leakage current will be very low. When ESD zaps onto the node V_{CC}, the rise time of voltage on V_{CC} is in the order of 10 ns. The larger *dV/dt* displacement current will create a higher voltage drop V_{AA} across R_{1A}, and Q_{E1A} will be turned on to discharge the large ESD current. The designed parameters are shown in Table I.

TABLE I
Device Parameters of the *CR*-Coupling Circuit

Testkey	C_{1A}	R_{1A}	Q_{E1A}
A1	24 pF	4.86 MΩ	W=6000 µm, L=1 µm

TABLE II
Device Parameters of the Modified *CR*-Coupling Circuit

Testkey	C_{1B}	R_{1B}	Q_{E1B}	C_{2B}	R_{2B}	Q_{DS1B}∼ Q_{DS5B}	Q_{E2B}
B1	24 pF	4.86 MΩ	W=6000 µm L=1 µm	1.8 pF	2.98 MΩ	W = 5 µm L=10µm	W=5 µm L=1 µm

The other design is the modified *CR*-coupling circuit, which can reduce the transient leakage, as shown in Fig. 2(b). The diode-connected high electron mobility transistors (HEMTs) (Q_{DS1B}∼Q_{DS5B}) are used as a voltage divider to prevent overvoltage issues on node V_{AB} in the steady state. During normal operating conditions, the node V_{AB} will be raised to a high level to turn on Q_{E2B}, and the node V_{BB} can be pulled to a low-voltage level to prevent the leakage current of Q_{E1B}. However, a leakage current can still be induced during fast power-on conditions since Q_{E2B} cannot be turned on efficiently. After V_{CC} is powered to a 6-V steady state, although the node V_{BB} is kept at a low-voltage level to turn off the primary ESD device Q_{E1B}, there is a standby leakage current induced by the path of R_{2B} and the diode-connected HEMTs (Q_{DS1B}∼Q_{DS5B}). When ESD zaps onto the node V_{CC}, V_{BB} will be coupled to a high-voltage level, and Q_{E1B} will be turned on to discharge the large ESD current. The designed parameters are shown in Table II.

B. Proposed Design

The schematic of the newly proposed power-rail ESD clamp circuit is shown in Fig. 3. It contains two detecting functions. One is the timing detector composed of the *CR*-coupling circuit, and the other one is the voltage detector composed of the diode-connected HEMTs.

In the normal power-on condition, the rise time of voltage on V_{CC} is about 0.1∼1 ms. Because the slew rate of V_{CC} is relatively low, the node V_A is kept at a low-voltage level, and Q_{E2} is turned off. Hence, the node V_B is kept at a low-voltage

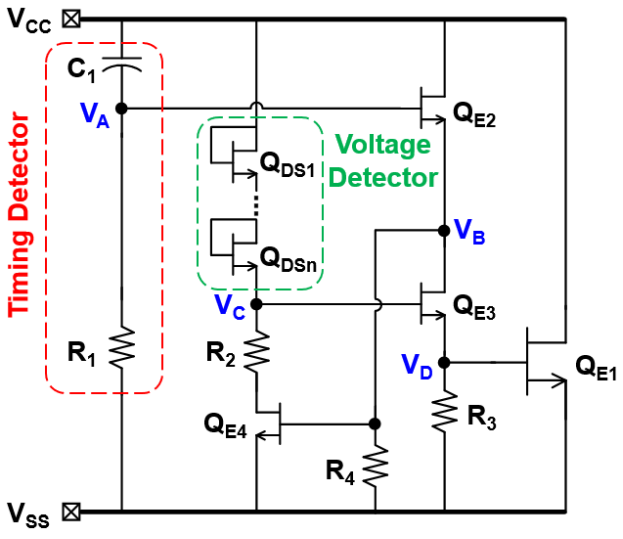

Fig. 3. Schematic of the newly proposed power-rail ESD clamp circuit.

level, and Q_{E4} is kept off. Besides, the threshold voltage (V_{th}) of the enhancement-mode HEMT (E-HEMT) is 1.46 V. Because the voltage rating of V_{CC} is 6 V, the voltage level is below the turn-on voltage of the diode-connected HEMTs. Hence, the node V_C is kept at a low-voltage level, and Q_{E3} will be turned off. Then, the node V_D is kept at a low-voltage level, and the primary ESD HEMT Q_{E1} is kept OFF-state. Therefore, there is no leakage path during normal power-on conditions. Moreover, since Q_{E4} is turned off in the steady state, it can block the leakage path of the voltage detector. Hence, there is no leakage path in steady states.

In the fast power-on condition, the rise time of the voltage on V_{CC} is in the order of 10 ns. Because the slew rate of V_{CC} is relatively high, the node V_A will be coupled to a high-voltage level, and Q_{E2} will be turned on. Then, the node V_B is raised to a high-voltage level, and Q_{E4} is turned on. However, because the voltage rating of V_{CC} is 6 V, the voltage level is below the turn-on voltage of the diode-connected HEMTs. The node V_C is kept at a low-voltage level, and Q_{E3} is kept off. Hence, the node V_D is kept at a low-voltage level, and the primary ESD HEMT Q_{E1} is kept OFF-state. Therefore, no transient leakage current will be induced during fast power-on conditions. After powering to a 6-V steady state, since Q_{E4} will be turned off, there is no leakage path in steady states.

In the condition of ESD zapping on V_{CC}, the rise time of voltage on V_{CC} is in the order of 10 ns. Because the slew rate of V_{CC} is relatively high, the node V_A will be coupled to a high-voltage level, and Q_{E2} will be turned on. Then, the node V_B is raised at a high-voltage level, and Q_{E4} is turned on. Because the voltage level of the ESD pulse is high enough, the diode-connected HEMTs will be turned on, and the node V_C will be pulled to a relatively high-voltage level to turn on Q_{E3}. Since Q_{E2} and Q_{E3} are both turned on, the node V_D will be charged to a high-voltage level and the primary ESD HEMT Q_{E1} will be turned on to discharge the large ESD currents.

The triggered voltage (V_{t1}) means the turn-on voltage of the power-rail ESD clamp circuit. Because the turn-on criterion of the power-rail ESD clamp circuit is that Q_{E2} and Q_{E3} must be turned on, V_{t1} is correlated to the turn-on voltage of the voltage detector. Therefore, V_{t1} of the proposed power-rail ESD clamp circuit can be adjusted by changing the number of the diode-connected HEMTs to meet different V_{CC} applications. In order to investigate how the device parameters affect the circuit operation during ESD events, the experimental splits of the testkeys can be referred to in Table III. In all testkeys, the capacitor C_1 is designed to be 1.5 pF, and it is realized by the metal–insulator–metal (MIM) capacitor. The resistor R_1 is designed as 400 kΩ, and the resistors $R_2/R_3/R_4$ are designed as 300 kΩ. These resistors are all realized by the 2D-electron-gas (2DEG) resistors.

TABLE III
DEVICE PARAMETERS OF THE NEWLY PROPOSED POWER-RAIL ESD CLAMP CIRCUIT

Testkeys	Q_{E2}, Q_{E3}	$Q_{DS1} \sim Q_{DSn}$	Q_{E1}	Q_{E4}
C1	W=100 μm L=1 μm	n=5 W=100 μm L=1 μm	4000 μm	W=50 μm L=1 μm
C2			6000 μm	
C3	W=50 μm L=1 μm			
C4	W=250 μm L=1 μm			
C5	W=100 μm L=1 μm	n=3 W=100 μm L=1 μm		
C6	W=100 μm L=1 μm	n=7 W=100 μm L=1 μm		

C. SPICE Simulation

For the simulation of normal power-on conditions, the rise time of voltage on V_{CC} is set to be 0.2 ms. The simulation waveforms among the prior arts (testkey A1, testkey B1) and the proposed design (testkey C4) can be referred to in Fig. 4(a). The voltage on the node V_{AA} in testkey A1, V_{BB} in testkey B1, and V_D in testkey C4 is 2.8, 1.8, and 0 V, respectively. Hence, during the normal power-on condition, the transient leakage in testkey A1 is the largest, while that in testkey C4 is the lowest. For the simulation of fast power-on condition, the rise time of voltage on V_{CC} is set to be 20 ns. The simulation waveforms can be referred to in Fig. 4(b). The voltage on the node V_{AA} in testkey A1 and V_{BB} in testkey B1 is both 5 V. Because the detection circuit in testkey B1 cannot be activated immediately, the transient leakage will be at the same value. However, the voltage on the node V_D in testkey C4 is only 1.4 V, which is below V_{th} (1.46 V) of the HEMT device. Hence, the transient leakage in testkey C4 will be the lowest during the fast power-on condition. For the simulation of the ESD-stress condition, the voltage level of V_{CC} is set to 16 V, and the rise time is set to 10 ns. The simulation waveforms can be referred to in Fig. 4(c). The voltage on the node V_{AA} in testkey A1 and V_{BB} in testkey B1 is both 13 V, which can be attributed to the same reason mentioned in the fast power-on condition. The voltage on the node V_D in testkey C4 is 8 V. Since the gate bias of the primary ESD HEMT among the three testkeys is high enough, ESD protection can be well performed.

The other design consideration is the tradeoff between the number of diode-connected HEMTs and the turn-on degree of the primary ESD HEMT during ESD events. The simu-

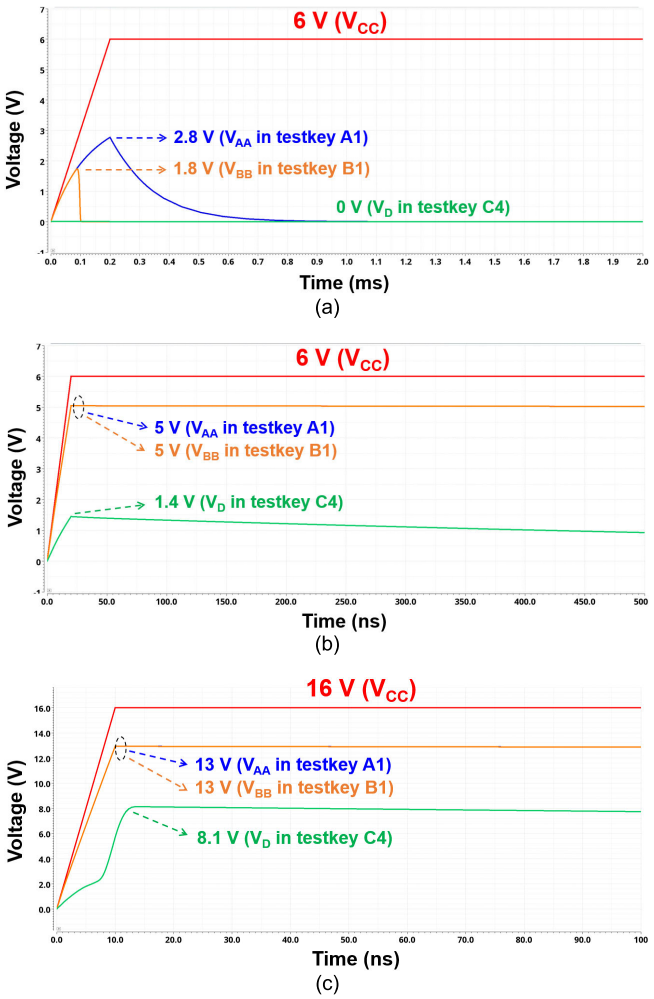

Fig. 4. Simulated waveforms of the gate voltage on the primary ESD HEMT among the testkeys under (a) normal power-on, (b) fast power-on, and (c) ESD-stress conditions.

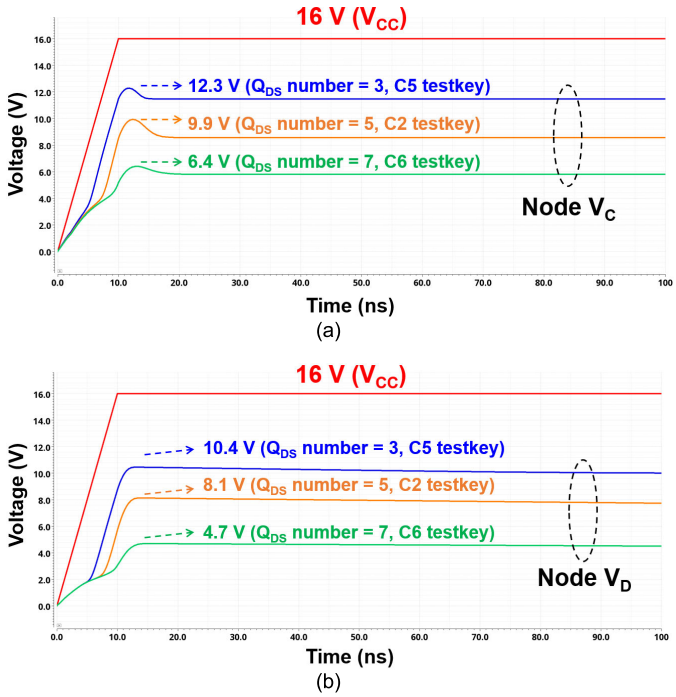

Fig. 5. Simulated waveforms on (a) node V_C and (b) node V_D of the proposed design with different numbers of diode-connected HEMTs under ESD-stress conditions.

lated waveforms on the nodes V_C and V_D of the proposed design with different numbers of diode-connected HEMTs under ESD-stress conditions are shown in Fig. 5(a) and (b), respectively. Because the voltage on the node V_C is correlated to the voltage drop on the diode-connected HEMTs, the more diode-connected HEMTs will result in a lower voltage level on node V_C, as shown in Fig. 5(a). Therefore, the voltage on the node V_D will be lower with the more diode-connected HEMTs, as shown in Fig. 5(b), and the ESD robustness will be also degraded. Therefore, although V_{t1} of the proposed power-rail ESD clamp circuit can be adjusted by changing the number of the diode-connected HEMTs to meet different V_{CC} applications, it is still necessary to adjust other component parameters to prevent the degradation of ESD robustness.

III. Experimental Results

A. TLP I–V Curves of Stand-Alone Main ESD HEMT

In order to verify whether the ESD robustness of the primary ESD HEMT is correlated to its gate bias, the TLP $I-V$ curves with different gate biases were measured by a TLP system with a rise time of 10 ns and a pulsewidth of 100 ns. The test device is a stand-alone E-HEMT with a total width of 6000 μm. From the experimental results of TLP $I-V$ curves shown in Fig. 6(a), it can be observed that the E-HEMT cannot conduct a large ESD current when the device is in OFF-state ($V_{gs} = 0$ V). The breakdown voltage under transient TLP measurement is 142 V. Moreover, the TLP failure current is higher with increasing gate bias, which can be attributed to the lower resistance existing in the channel region. Fig. 6(b) shows the correlation between the gate bias of HEMT and the TLP failure current. The TLP failure current shows good linearity in high-V_{GS} conditions. Since there is no parasitic BJT to conduct the ESD current in HEMT devices, the only discharging path is the channel region. Therefore, based on experimental results, it is important to make the gate bias of the primary ESD HEMT as high as possible during ESD events when designing the power-rail ESD clamp circuit.

B. Chip Implementation and DC I–V Characteristic

The test chip was fabricated in a 0.5-μm GaN-on-Si technology. The chip photograph of the testkeys A1, B1, and C4 is shown in Fig. 7(a)–(c), respectively. The primary ESD HEMT in the three testkeys is designed to be 6000 μm. For the *CR*-coupling circuit A1, the layout area is 201 650 μm^2, which is dominated by C_{1A} and R_{1A}. For the modified *CR*-coupling circuit B1, the layout area is 219 040 μm^2, which is dominated by C_{1B}, R_{1B}, and R_{2B}. For the proposed design C4, the layout area is only 92 241 μm^2, which is 0.46 times smaller than the *CR*-coupling circuit. The primary ESD HEMT and the detection circuit occupy half of the chip area. The area comparison of the detection circuit and the primary ESD

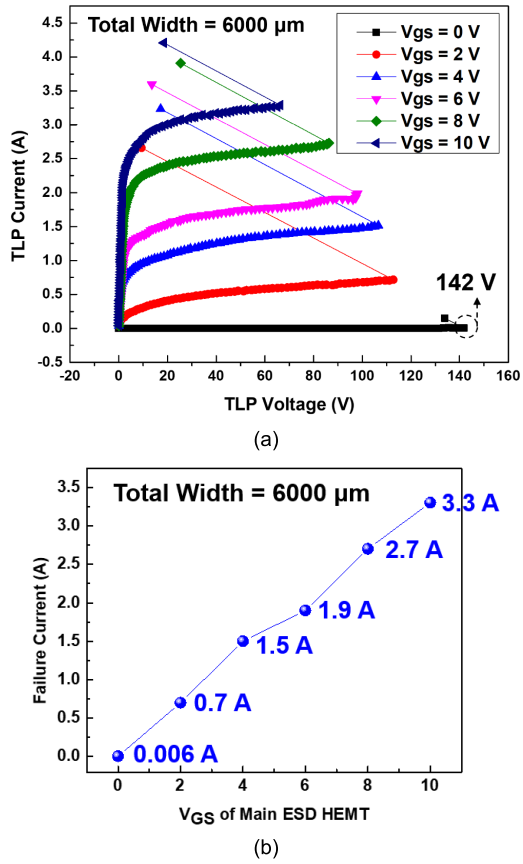

Fig. 6. (a) TLP *I–V* curves of a 6000-μm HEMT with different gate biases. (b) Correlation between the gate bias of HEMT and the TLP failure current.

TABLE IV
AREA COMPARISON AMONG THE PRIOR ARTS AND THE PROPOSED DESIGN

Testkey	Primary ESD HEMT (Q_{E1A}, Q_{E1B}, Q_{E1})	Area of detection circuit (μm^2)	Total area (μm^2)	Total area normalized to A1 testkey
A1 (CR-coupling)	W=6000 μm L=1 μm Active area = 35791 μm^2	165859	201650	1
B1 (Modified CR-coupling)		183249	219040	1.09
C4 (The proposed design)		56450	92241	0.46

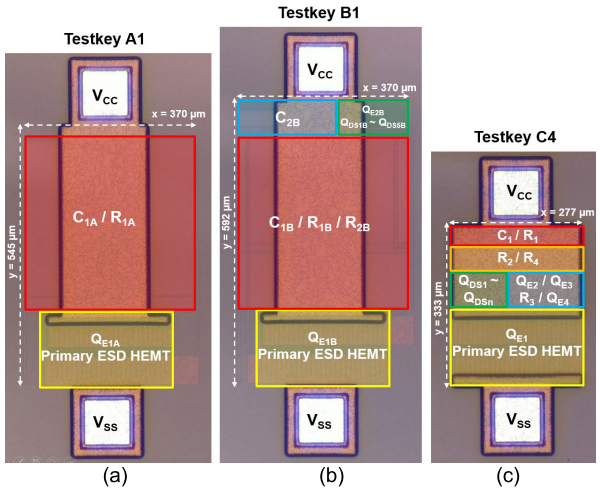

Fig. 7. Chip photograph of (a) *CR*-coupling circuit A1, (b) modified *CR*-coupling circuit B1, and (c) proposed design C4.

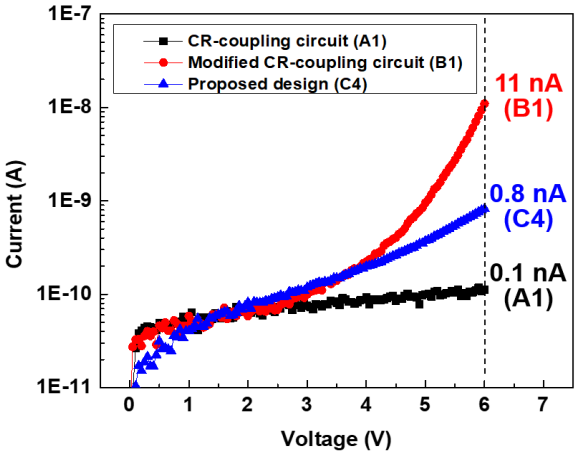

Fig. 8. Comparison of dc standby leakage current among the prior arts (A1 and B1) and the proposed design (C4) under the same 6000-μm primary ESD HEMT.

HEMT among the testkeys was listed in Table IV. The dc *I–V* curves of the proposed design and the prior arts are shown in Fig. 8. The *I–V* measuring range is from 0 to 6 V, which is within the operating voltage of the circuit. The dc standby leakage current of the *CR*-coupling circuit A1 is 0.1 nA, which is the lowest among the three structures. It can be attributed to the lack of a detection circuit, so no other leakage path exists. However, the transient leakage current of the *CR*-coupling circuit is highest, which will be discussed in the next section. The leakage current of the proposed design C4 with 0.8 nA is lower than that of the modified *CR*-coupling circuit B1 with 11 nA. The root cause is that the modified *CR*-coupling circuit has a leakage path formed by R_{2B} and the diode-connected HEMTs (Q_{DS1B}~Q_{DS5B}).

C. Normal Power-on Condition

A 6-V voltage waveform with a rise time of around 0.2 ms is used to investigate the transient leakage current during normal power-on conditions. The measured waveforms are shown in Fig. 9. For the prior arts of the *CR*-coupling circuit A1 and the modified *CR*-coupling circuit B1, the peak value of the transient leakage current is 35 and 28 mA, which is shown in Fig. 9(a) and (b), respectively. These two prior arts have transient leakage currents because there is a coupling capacitor C_1 between the V_{CC} power line and the gate of the primary ESD HEMT Q_{E1}. Although the coupling capacitor can help the gate of the primary ESD HEMT to be coupled to a high-voltage level, it can induce transient leakage current during power-on conditions. However, there is no transient leakage current in the proposed design of the C4 testkey because the voltage level of V_{CC} is not high enough to trigger the voltage

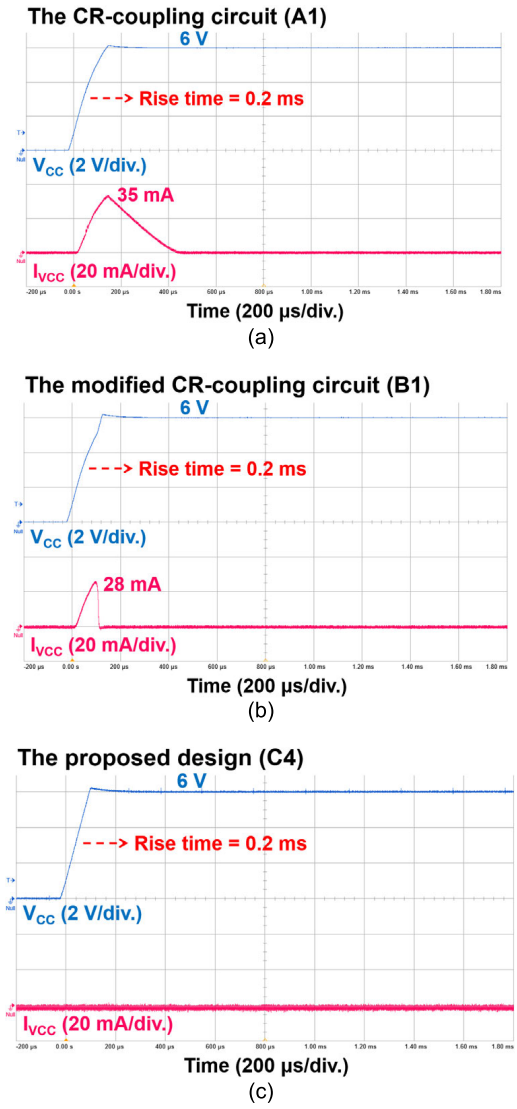

Fig. 9. Measured waveforms of transient leakage current during normal power-on conditions with (a) prior art A1, (b) prior art B1, and (c) proposed design C4.

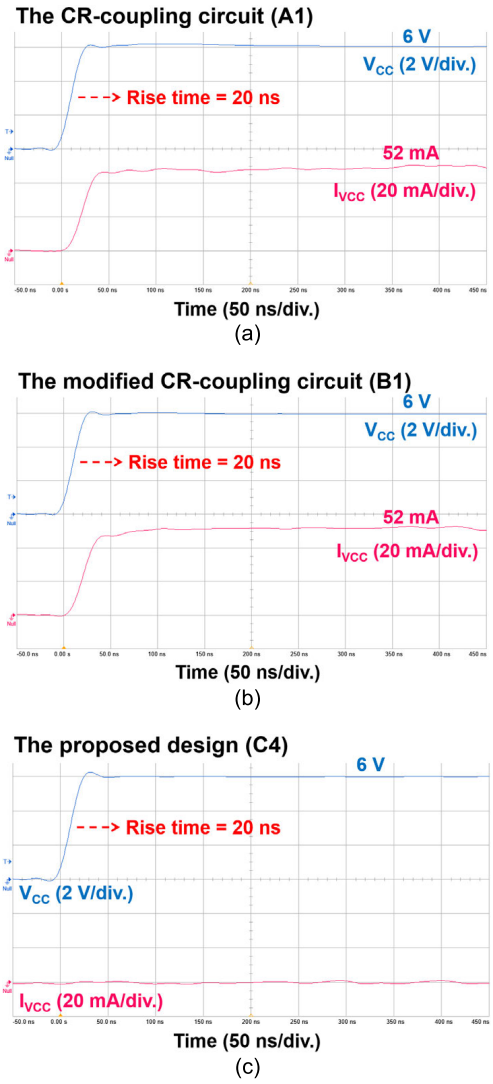

Fig. 10. Measured waveforms of transient leakage current during fast power-on conditions in (a) prior art A1, (b) prior art B1, and (c) proposed design C4.

detector, as shown in Fig. 9(c). As a result, the proposed power-rail ESD clamp circuit has the best leakage performance of the three designs during normal power-on conditions.

D. Fast Power-on Condition

A 6-V voltage waveform with a rise time of around 20 ns is used to verify the circuit under fast power-on conditions. The measured waveforms are shown in Fig. 10. For the two prior arts of the *CR*-coupling circuit A1 and the modified *CR*-coupling circuit B1, the peak values of the transient leakage currents are both 52 mA, which are shown in Fig. 10(a) and (b), respectively. Compared to the normal power-on conditions, the larger transient leakage current under fast power-on conditions can be ascribed to the larger dV/dt across the coupling capacitor C_1. Hence, if the slew rate of V_{CC} is higher, the coupled gate voltage of the primary ESD HEMT will be higher, and the leakage current will be larger. However, there is no transient leakage current in the proposed design of the C4 testkey because the voltage level of V_{CC} is not high enough to trigger the voltage detector, as shown in Fig. 10(c). In conclusion, the proposed design shows excellent leakage performance under normal power-on and fast power-on conditions. Therefore, the system's power consumption can be reduced considerably when the proposed design is implemented in the ESD protection of GaN-based ICs.

E. ESD Analysis by TLP Measurement and HBM Test

This section will mainly focus on how the ESD robustness is affected by the design parameters of the proposed power-rail ESD clamp circuit. The TLP system with a 10-ns rise time/100-ns pulsewidth and the HBM tester were used to investigate the ESD robustness.

1) Adjusting the Size of Main ESD HEMT Q_{E1}: The ESD robustness of the proposed power-rail ESD clamp circuit is mainly affected by the size of the primary ESD HEMT Q_{E1}. Because Q_{E1} occupies almost half of the chip area, as shown

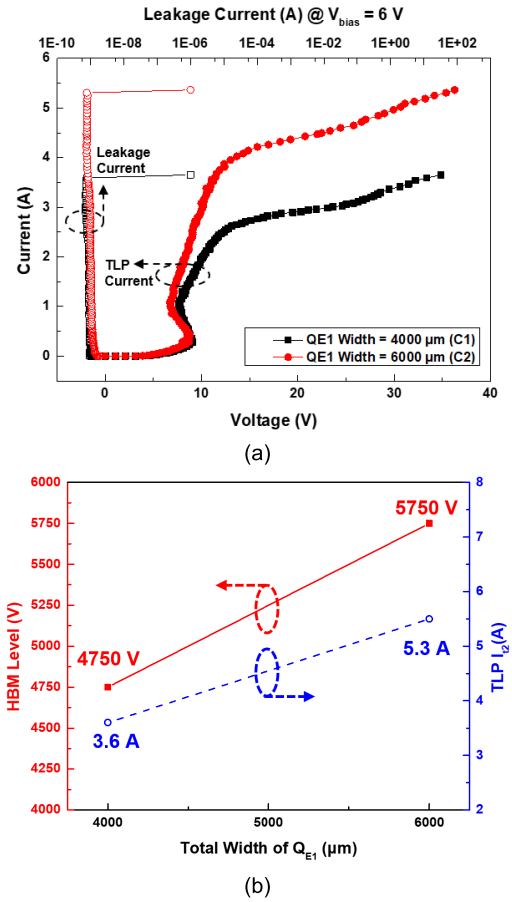

Fig. 11. (a) TLP I–V curves of the proposed design with different sizes of. (b) Correlation between the TLP failure current and the HBM ESD level under different sizes of.

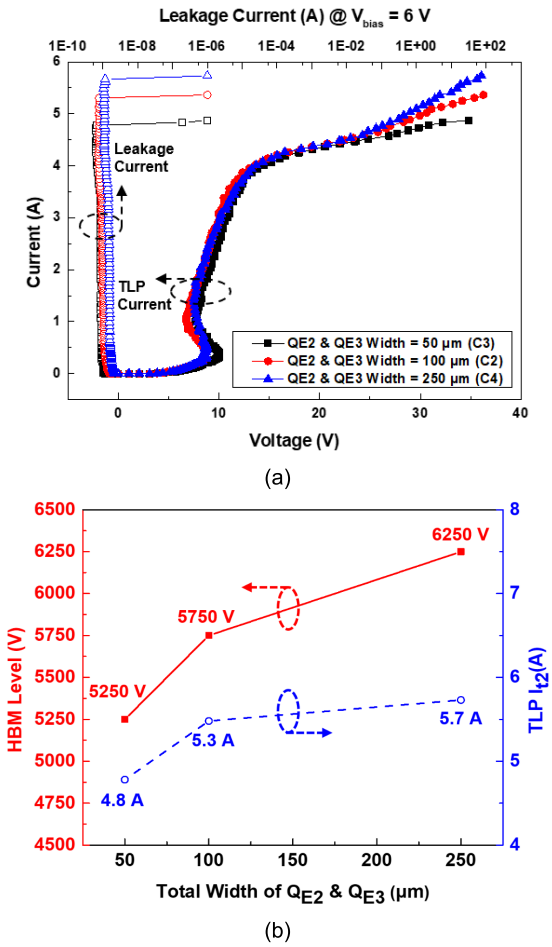

Fig. 12. (a) TLP I–V curves of the proposed design with different sizes of . (b) Correlation between the TLP failure current and the HBM level under different sizes of and.

in Fig. 7(c), it is necessary to properly design the size of the primary ESD HEMT to guarantee sufficient ESD robustness. Fig. 11(a) shows the TLP I–V curves with the primary ESD HEMT of 4000 and 6000 μm, respectively. The experiment was conducted with testkeys C1 and C2. The triggered voltage (V_{t1}) of the TLP I–V curves is defined to be the turning point, at which the I–V curves happen snapback phenomenon. V_{t1} of the proposed design with 4000 and 6000 μm are 9.0 and 8.8 V, respectively. In addition, the failure currents are 3.6 and 5.3 A, which is scalable in the total width of Q_{E1}. Moreover, it is noteworthy that there is a snapback phenomenon in the TLP I–V curves. The slight current before the snapback can be attributed to the turn on of the detection circuit. After that, the weak snapback can be interpreted as the gradual turn on of Q_{E1}. After the holding voltage, Q_{E1} may be fully turned on to conduct the large TLP current. Fig. 11(b) shows the correlation plot of the TLP failure current, HBM ESD level, and the device total width of Q_{E1}. The HBM levels of the proposed design with 4000 and 6000 μm are 4750 and 5750 V, respectively. Hence, the ESD robustness can be enhanced by increasing the size of Q_{E1}.

2) Adjusting the Size of Q_{E2} and Q_{E3}: Based on the conclusion in Section III-A, because the maximum ESD discharging current can be directly affected by the gate bias of the primary ESD HEMT (the voltage drop on node V_D) in Fig. 3, it is essential to properly design the size of Q_{E2} and Q_{E3} to guarantee sufficient current flowing into resistor R_3. The experiment was conducted with testkeys C3, C2, and C4. The experimental splits of the total width of Q_{E2} and Q_{E3} are designed as 50, 100, and 250 μm, and the corresponding TLP I–V curves are shown in Fig. 12(a). It can be observed that V_{t1} was affected by the size of Q_{E2} and Q_{E3}. With sizes of 50, 100, and 250 μm, V_{t1} is 10, 8.8, and 8.7 V, respectively. Hence, it can be inferred that the larger size of Q_{E2} and Q_{E3} will lead to an earlier turn on of the primary ESD HEMT Q_{E1} during ESD events. The turn-on resistance beyond the holding voltage does not show a noticeable difference because it is dominated by the size of Q_{E1}. However, the size of Q_{E2} and Q_{E3} can still affect the ESD robustness to some degree. As shown in Fig. 12(b), the TLP failure currents with sizes of 50, 100, and 250 μm are 4.8, 5.3, and 5.7 A, respectively, and their corresponding HBM levels are 5250, 5750, and 6250 V. Therefore, it is certain that the size of Q_{E2} and Q_{E3} still play a role in ESD robustness.

3) Adjusting the Number of Q_{DS}: In the proposed power-rail ESD clamp circuit, because it contains a voltage detector comprised of a series of diode-connected HEMTs (Q_{DS}), V_{t1} of the ESD clamp circuit is mainly determined by the number of Q_{DS}. Moreover, it is essential that the turn-on voltage of

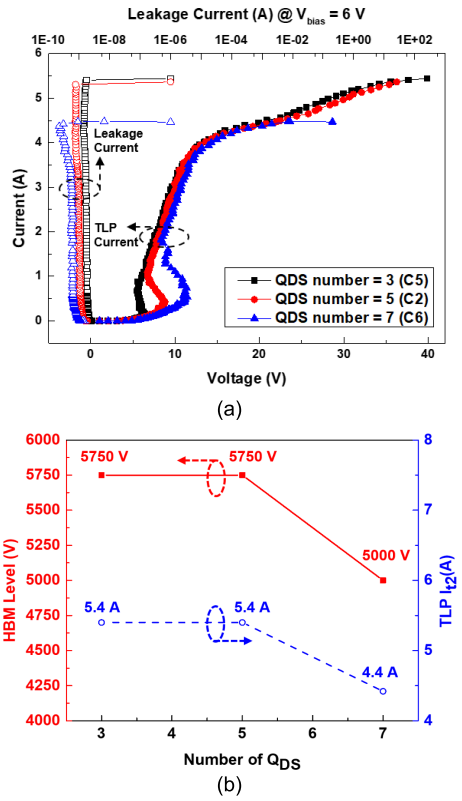

Fig. 13. (a) TLP I–V curves of the proposed design with different numbers of Q_{DS}. (b) Correlation between the TLP failure current and the HBM level under different numbers of Q_{DS}.

the voltage detector should be designed to be higher than V_{CC} so that it will not induce false triggering issues during fast power events. The measured TLP I–V curves are shown in Fig. 13(a). The experiment was conducted with testkeys C5, C2, and C6. The number of Q_{DS} is designed as 3, 5, and 7, and V_{t1} extracted from the TLP $I-V$ curves is 6.4, 8.8, and 11.3 V, respectively. Thus, the turn-on voltage of the proposed design is tunable to meet different V_{CC} applications. Besides, the turn-on resistance beyond the holding voltage does not show a noticeable difference because it is dominated by the size of Q_{E1}. Fig. 13(b) shows the correlation between the Q_{DS} number, TLP failure current, and HBM level. The TLP failure currents are 5.4, 5.4, and 4.4 A, and the HBM levels are 5750, 5750, and 5000 V, respectively. The degradation of the ESD robustness can be ascribed to the higher turn-on voltage of the voltage detector with the Q_{DS} number of 7. Because the higher turn-on voltage of the voltage detector will result in a lower voltage drop on the node V_C, the turn-on degree of Q_{E3} will be degraded. Hence, it will result in the degradation of the voltage drop on node V_D and reduce the discharging capability of Q_{E1}. Therefore, the ESD robustness will be degraded when the number of Q_{DS} is too many. Thus, the tradeoff between the turn-on voltage and the ESD robustness must be taken into consideration when using the proposed design.

IV. Comparison With Prior Arts

Table V lists some key indexes of the power-rail ESD clamp circuit to compare with the prior arts mentioned previously.

TABLE V
COMPARISON AMONG THE PROPOSED POWER-RAIL ESD CLAMP CIRCUIT AND THE PRIOR ARTS

Circuit/Device under test	Prior art A IEDM'23 [12]	Prior art B ICMTS'24 [13]	Prior art C JEDS'24 [14]	This work (testkey C4)
Topology	Modified CR-coupling	CR-coupling	Modified CR-coupling	Dynamic timing-voltage detection
Main ESD HEMT size	N/A	6000 μm	6000 μm	6000 μm
Layout Area	N/A	201650 μm^2	219040 μm^2	99241 μm^2
HBM ESD level	3000 V	6250 V	6000 V	6250 V
DC standby leakage @ 6 V	3.81 μA	0.1 nA	11 nA	0.8 nA
Against fast power-on issue	No	No	No	Yes

The prior art A is the reference study published in 2023 *IEDM* [12]. The prior art B is the *CR*-coupling circuit in Fig. 2(a) [13]. The prior art C is the modified *CR*-coupling circuit in Fig. 2(b) [14]. The prior A did not show the size information of the primary ESD HEMT and layout area in its article. The total width of the main ESD HEMT in the proposed design and prior art B/C is 6000 μm. For the ESD HBM level, the prior art A, B, and C possess 3000-, 6250-, and 6000-V HBM levels, respectively. The proposed design of this work possesses a 6250-V HBM level.

With respect to the dc standby leakage, the prior art A possesses a leakage current of 3.81 μA. The prior art B possesses a leakage current of 0.1 nA, which is the lowest among the designs due to the lack of leakage path. The prior art C possesses a leakage current of 11 nA, and the leakage path was ascribed to the diode-connected HEMTs. However, because the proposed design eliminates the leakage path of the diode-connected HEMTs, it also possesses a low leakage current with only 0.8 nA. Regarding the transient leakage current issue during fast power-on conditions, the three prior arts are mainly based on the timing detection function realized by the *CR*-coupling circuit, so they cannot prevent this issue. However, because the proposed design has a voltage detection function realized by the diode-connected HEMTs, it can solve this issue effectively.

V. Conclusion

The proposed power-rail ESD clamp circuit is the first structure in a GaN-on-Si process to solve the transient leakage current during fast power-on conditions. The proposed design with dynamic timing-voltage detection function has been successfully verified in the fabricated chip. The experimental results demonstrate that the proposed design possesses an ultralow standby leakage current with only 0.8 nA. Moreover, the proposed design has no transient current due to the voltage detection function, which is realized by the diode-connected HEMTs, under either normal power-on or fast power-on conditions. The ESD robustness can be effectively enhanced by increasing the size of the main ESD HEMT Q_{E1}.

Through increasing the size of Q_{E2} and Q_{E3}, the triggered voltage can be slightly reduced. The HBM ESD robustness can be enhanced to 6250 V. Regarding the voltage detection function, the triggered voltage can be increased by adding the number of the diode-connected HEMTs, which makes the proposed design more flexible when it is utilized in different voltage ratings of V_{CC}. Therefore, the proposed design is an excellent solution for whole-chip ESD protection in monolithic GaN-based ICs.

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