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Investigation of ESD protection devices for SiC-based monolithic integrated circuits

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ESD protection diode

ABSTRACT

ESD characterization of on-chip ESD protection devices, including the gate-grounded NMOS (GGNMOS), the gate-VDD PMOS (GDPMOS), the N+/PW diode, and the P+/NW diode was investigated. With respect to GGNMOS and GDPMOS, ESD robustness was unrelated to the number of fingers under the breakdown mode. On the contrary, under the forward mode, ESD robustness can be effectively enhanced by increasing the number of fingers. Similar results were observed on the N+/PW and the P+/NW diodes. Under the breakdown mode, ESD robustness was not related to the junction perimeter of the diode. Under the forward mode, ESD robustness can be effectively enhanced by increasing the junction perimeter. By comparing the figure of merit (FoM) among these four devices, the FoM of diode is higher than that of MOS-based ESD devices. Moreover, the concept of whole-chip ESD protection with power-rail ESD clamp circuit was recommended to guarantee the sufficient ESD robustness of SiC-based integrated circuits.

1. Introduction

Because of the increasing demands on emerging high-power applications, such as electric vehicles, data centers, and equipment of the renewable energy, the SiC devices have been widely studied in recent years. Since the electric field for breakdown and the thermal conductivity in SiC devices are higher than those in Si devices, SiC is suitable for use in high-power systems operating under high-voltage and high-current conditions. The prior art about integrating the gate-driving circuit and the power MOSFET into a monolithic chip fabricated in the same SiC process was demonstrated [1]. Because the Si-based gate driver is replaced with the SiC-based gate driver, the thermal stability of the system can become better. The SiC-based monolithic integrated circuits (ICs) will be commercialized in the near future.

In order to fulfill the mass production, it is essential to verify the reliability of the SiC ICs. It is worth mentioning that the reliability specifications of electric vehicles are often stricter than those of consumer electronics [2]. Among the reliability issues of SiC ICs, the robustness of electrostatic discharge (ESD) is essential since ESD events would occur during manufacturing and assembly. The human body model (HBM) is an international standard to identify the ESD robustness of electronic devices or ICs [3]. The HBM test is used to simulate the device under test (DUT) being stressed by the ESD energy stored in the human body during fabrication. To observe the transient I-V behavior of devices under ESD stress, the transmission-line-pulse (TLP) system was traditionally used to analyze ESD characteristics of devices for ESD protection design. Based on the TLP-measured I-V curves of the victim devices, the ESD design window can be identified, and the suitable ESD protection circuit can be well designed.

Some previous studies on ESD devices in SiC processes were ever reported [4,5], including the silicon-controlled rectifier (SCR) device

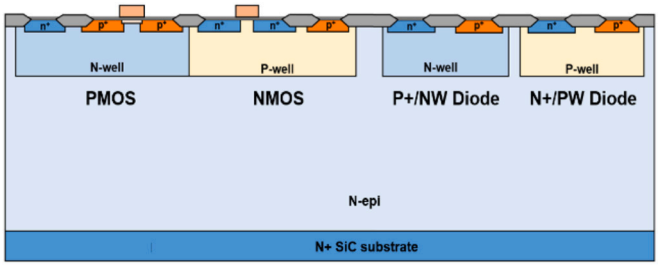

Fig. 1. The cross-sectional views of the device structures, including the GGNMOS, the GDPMOS, the N+/PW diode, and the P+/NW diode.

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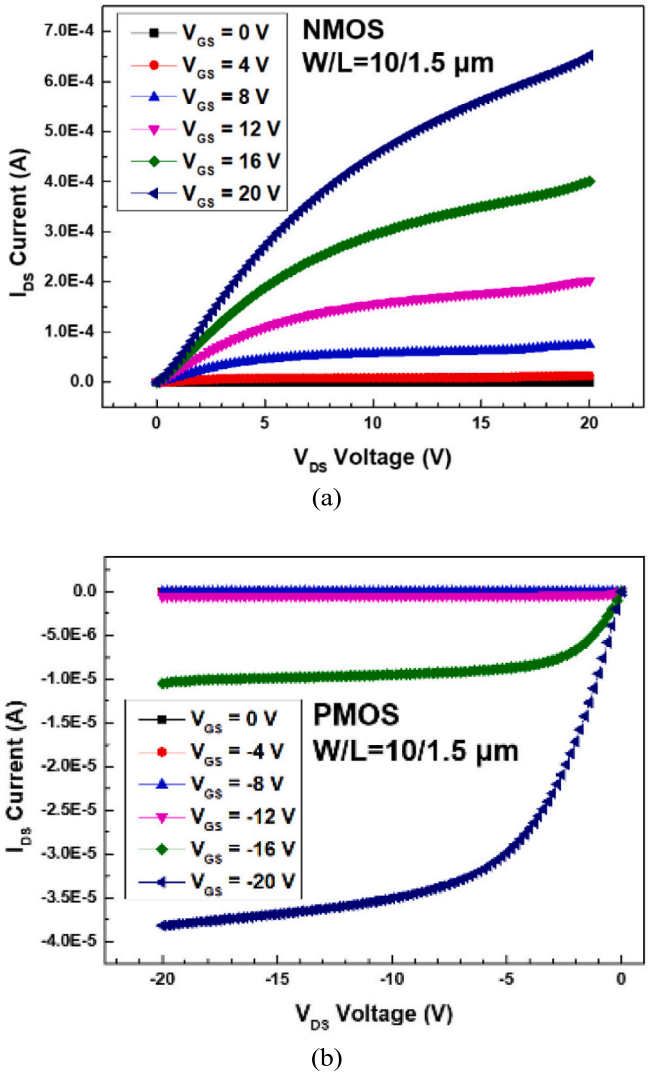


Fig. 2. The DC I_{ds}-V_{ds} curves of (a) the NMOS and (b) the PMOS with their W/L of 10 μm/1.5 μm, respectively.

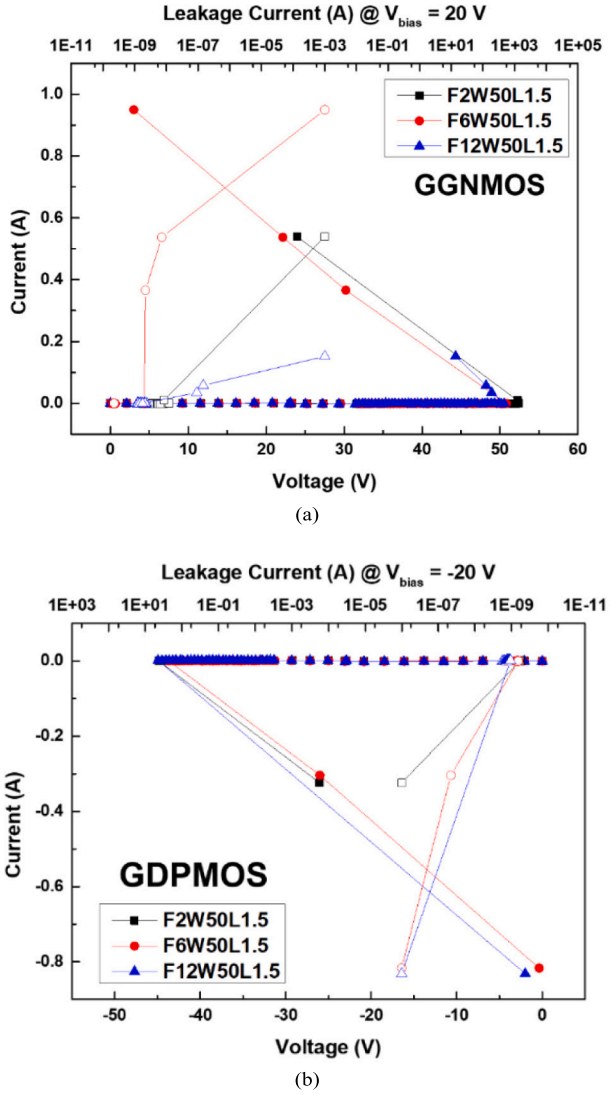


Fig. 4. The TLP I_{ds}-V_{ds} curves of (a) the GGNMOS and (b) the GDPMOS under the breakdown mode with different finger numbers.

[6–8]. The commonly-used ESD protection devices, such as the gate-grounded NMOS (GGNMOS), the gate-VDD PMOS (GDPMOS), the N+/PW diode, and the P+/NW diode, were not clearly investigated. Hence, this work aims to investigate these four ESD protection devices by the TLP measurement and HBM ESD test [9]. The failure analysis was also conducted to investigate the failure site. The characterization of the ESD testkeys in this work can be the reference of the design for the on-chip ESD protection of SiC ICs.

2. Test structure and measurement setups

The ESD protection devices investigated in this study included GGNMOS, GDPMOS, N+/PW diode, and P+/NW diode. The cross-sectional views of those device structures are shown in Fig. 1. In this structure, there was no P-type isolation under the devices. However, the P-type isolation layer and the corresponding floating guard rings are necessary to be added to guarantee that the low-voltage devices can sustain the high voltage from the backside of the chip when the high-

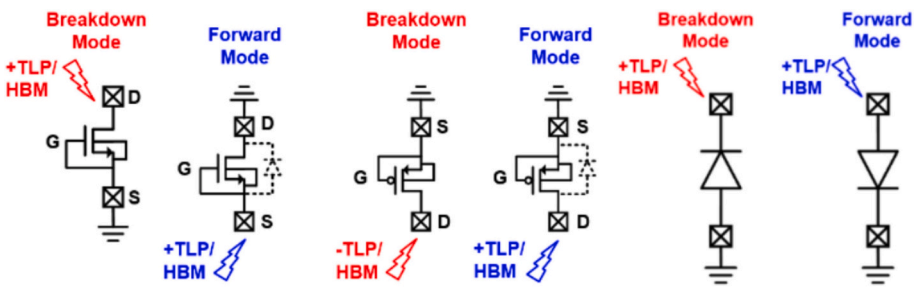


Fig. 3. The schematic diagram of the testing setup during TLP measurement and HBM ESD test.

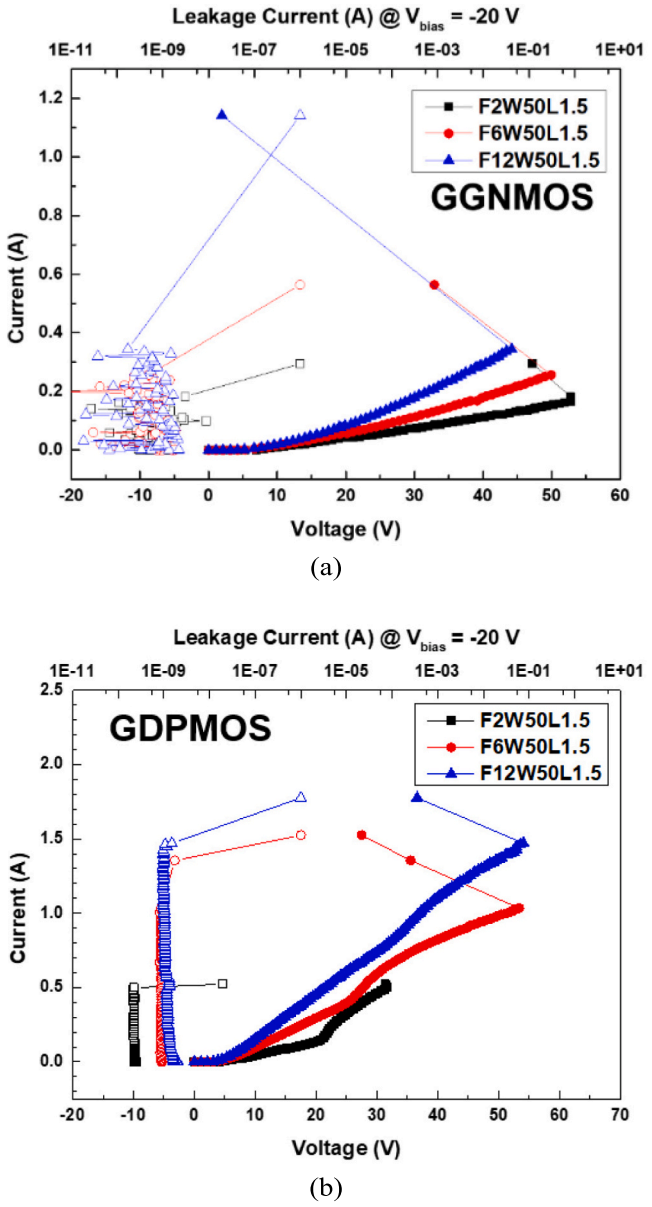


Fig. 5. The TLP I_{ds}-V_{ds} curves of (a) the GGNMOS and (b) the GDPMOS under the forward mode with different finger numbers.

voltage VDMOSFET is integrated into the same monolithic SiC chip. The DC characteristics of the NMOS and the PMOS can be referred to the I_{ds}-V_{ds} curves shown in Fig. 2(a) and (b). The maximum operating voltage of $|V_{GS}|$ and $|V_{DS}|$ of the NMOS/PMOS are both 20 V. For the 20-V single-finger NMOSFET with W/L of 10 μm/1.5 μm, the maximum driving current under V_{GS} of 20 V and V_{DS} of 20 V was 0.65 mA. For the 20-V single-finger PMOSFET with the same W and L values, the maximum driving current under V_{GS} of −20 V and V_{DS} of −20 V was 0.038 mA.

The test structures of GGNMOS and GDPMOS are drawn with multiple fingers in parallel. The W/L ratio of each finger is 50 μm/1.5 μm. With fingers of 2, 6, and 12, the device's total widths are 100 μm, 300 μm, and 600 μm, respectively. The test parameter of N+/PW diode and P+/NW diode is the junction's total perimeter, and the diode layout is also drawn in multiple-finger style. The perimeter can be adjusted by different finger lengths by fixing 10 fingers. With finger lengths of 5, 15, and 35, the total perimeter of the diode junction is 200 μm, 400 μm, and 800 μm, respectively.

The testing setup is illustrated in Fig. 3, where all of the devices were

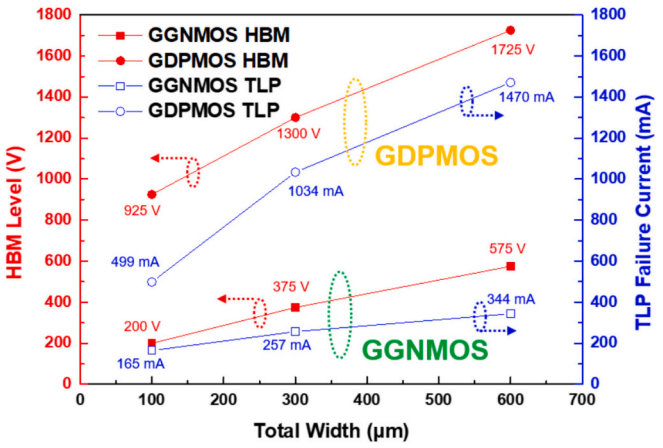


Fig. 6. The correlation of the ESD robustness under the forward mode versus different device total widths.

tested under breakdown and forward modes. The TLP test equipped by HANWA HED T-5000 can provide the TLP waveform with a rising time of 10 ns and a pulse width of 100 ns. The DC bias for monitoring the leakage measurement is 20 V after each TLP pulse. The HBM ESD tester used in this work is HANWA HCE-5000. All of the devices were tested under the breakdown and forward modes. The breakdown mode means that the testing waveform was zapped onto the reverse junction of the device. On the contrary, the forward mode means that the testing waveform was zapped onto the forward junction of the device.

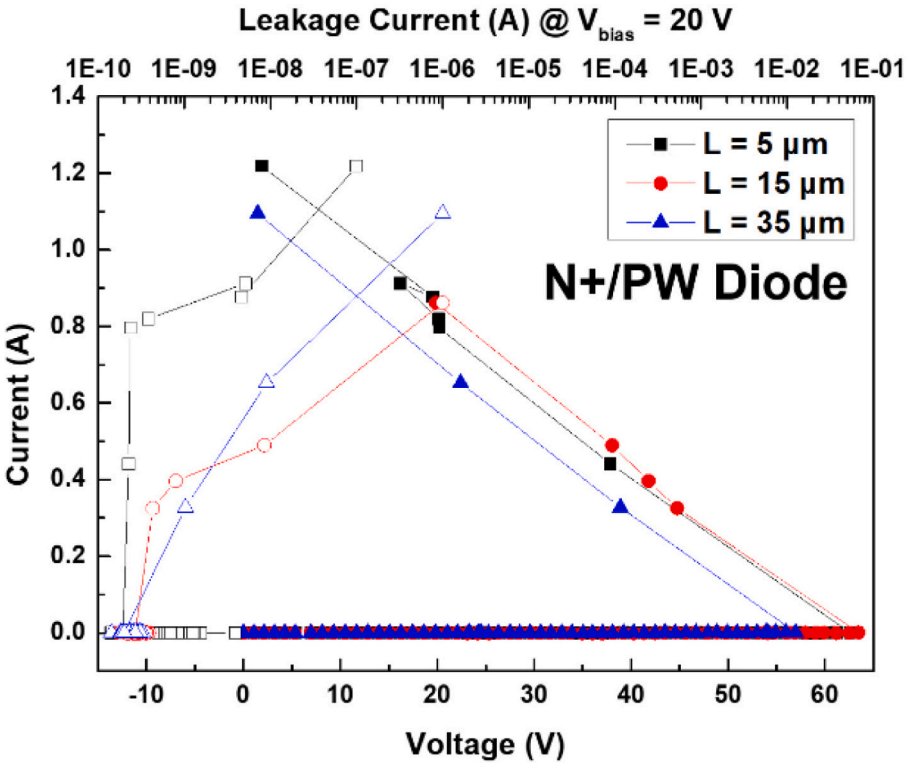
3. Experimental results

3.1. GGNMOS and GDPMOS

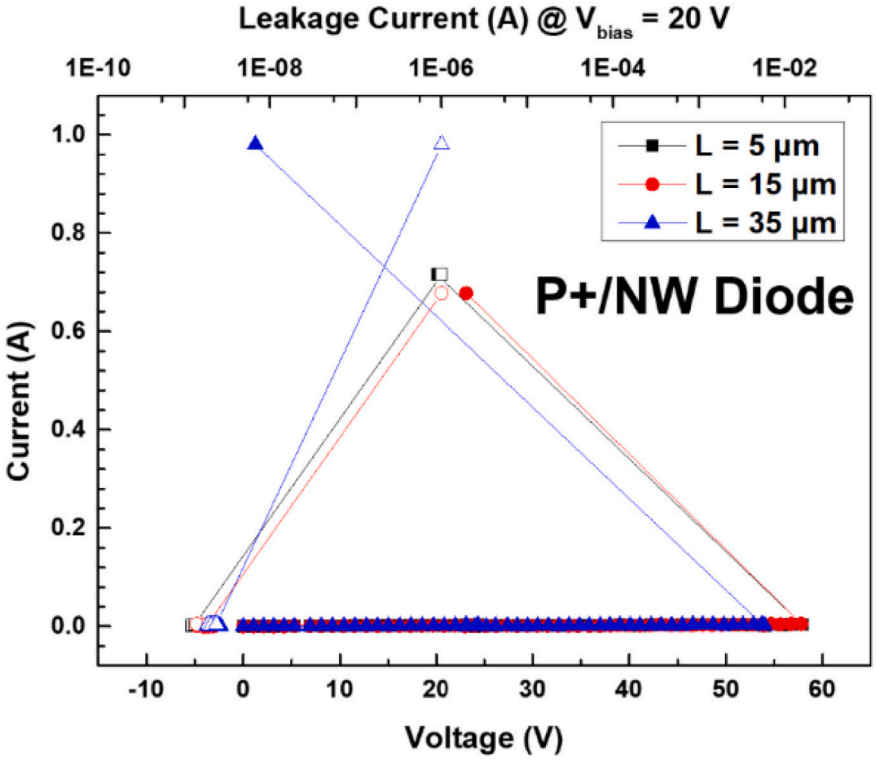
The TLP I_{ds}-V_{ds} curves of the GGNMOS and the GDPMOS under the breakdown mode with different finger numbers are shown in Fig. 4(a) and (b), respectively. The trigger voltage (V_{t1}) of GGNMOS and GDPMOS is not increased with the increase in finger number. For GGNMOS, the device was damaged after a breakdown without any snapback phenomenon. The failure currents of GGNMOS and GDPMOS under breakdown mode are around 0.1–0.4 mA. Since the triggering voltage of GGNMOS and GDPMOS is very high (40–50 V), the power across the reverse junction (P = I x V) is high enough to make the junction burn out immediately. Therefore, increasing the number of fingers cannot improve ESD robustness of the GGNMOS and GDPMOS under the breakdown mode.

The TLP I_{ds}-V_{ds} curves of the GGNMOS and the GDPMOS under the forward mode with different finger numbers are shown in Fig. 5(a) and (b), respectively. The failure current is enhanced by increasing the number of fingers because the perimeter of the body diode is increased. Furthermore, the turn-on resistance of the device is lower in the devices with more fingers. For GGNMOS, the failure currents of devices with finger numbers of 2, 6, and 12 are 165 mA, 257 mA, and 344 mA, respectively. For GDPMOS, the failure currents of devices with finger numbers of 2, 6, and 12 are 499 mA, 1034 mA, and 1470 mA, respectively. Hence, increasing the number of fingers can effectively enhance the ESD robustness of the GGNMOS and GDPMOS under the forward mode.

The correlation of ESD robustness under the forward mode versus different device total widths is summarized in Fig. 6. The red line indicates the HBM level, and the blue line indicates the TLP failure current. The HBM levels of GGNMOS and GDPMOS are also enhanced with the increase in total width. Moreover, the HBM level and TLP failure current in the GGNMOS are lower than those in the GDPMOS, which can be ascribed to the fact that the sheet resistance of the PW is ten times higher than that of the NW in the given SiC process.

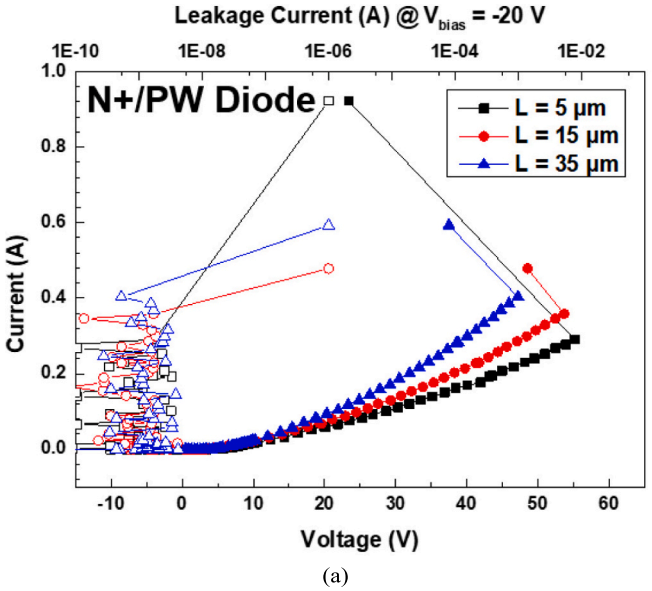


(a)

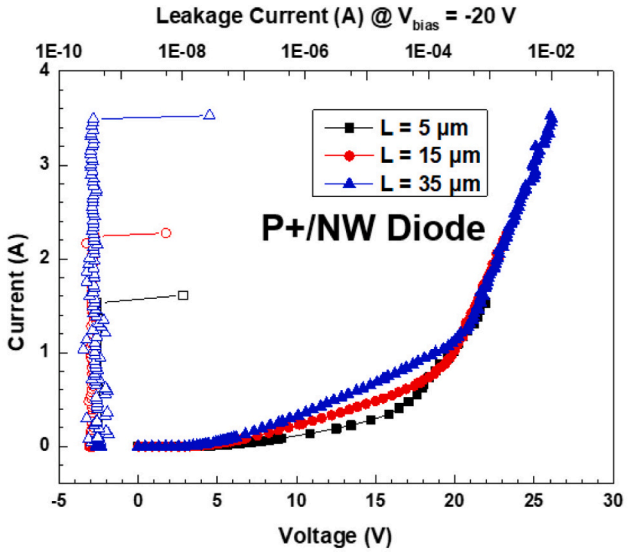


(b)

Fig. 7. The TLP *I-V* curves of (a) the N+/PW diode and (b) the P+/NW diode under the breakdown mode with different finger lengths.



(a)



(b)

Fig. 8. The TLP *I-V* curves of (a) the N+/PW diode and (b) the P+/NW diode under the forward mode with different finger lengths.

3.2. N+/PW diode and P+/NW diode

The TLP *I-V* curves of the N+/PW diode and the P+/NW diode under the breakdown mode with different finger lengths are shown in Fig. 7(a) and (b), respectively. The finger of the diode was fixed to be 10, and the perimeter of the junction can be adjusted by different lengths. The breakdown voltage of the N+/PW diode and the P+/NW diode did not increase with the increase in finger length. The device was damaged immediately after the breakdown. The ESD robustness of the N+/PW diode and P+/NW diode under the breakdown mode cannot be improved by increasing the perimeter of the junction.

The TLP *I-V* curves of the N+/PW diode and the P+/NW diode under the forward mode with different finger lengths are shown in Fig. 8(a) and (b), respectively. The failure current is enhanced by increasing the finger length because the perimeter of the junction is increased. For the N+/PW diode, the failure currents of the device with finger lengths of 5 μm, 15 μm, and 35 μm are 291 mA, 359 mA, and 403 mA, respectively. For the P+/NW diode, there is a soft failure phenomenon, so the failure current was defined in the first point of the abrupt change in the leakage current. The failure currents of the devices with finger lengths of 5 μm, 15 μm, and 35 μm are 1612 mA, 2275 mA, and 3527 mA, respectively. Hence, the ESD robustness of the N+/PW diode and the P+/NW diode under the forward mode can be effectively improved by increasing the finger length.

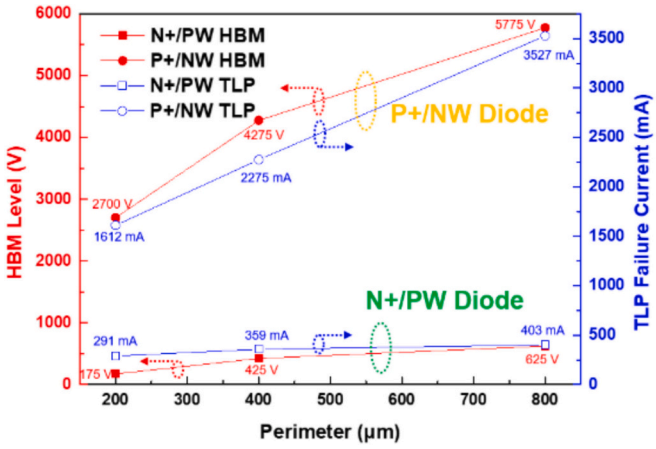


Fig. 9. The correlation of the HBM level and the TLP failure current versus different junction perimeters of the diodes.

The correlation of the ESD robustness under the forward mode versus different perimeters of the junction is summarized in Fig. 9. The red line indicates the HBM level, and the blue line indicates the TLP failure current. The HBM level of the N+/PW diode and the P+/NW diode are also enhanced with the increase in the perimeter of the junction. Moreover, the HBM level and the TLP failure current in the N+/PW diode are lower than that in the P+/NW diode, which can also be ascribed to the fact that the sheet resistance of the PW is ten times higher than that of the NW in the given SiC process.

4. Discussion

4.1. Failure analysis

To further investigate the failure site on the failure sample, the *Optical Beam Induced Resistance Change* (*OBIRCH*) was used. The images of the GGNMOS, GDPMOS, N+/PW diode, and P+/NW diode after the HBM ESD test are shown in Figs. 10–14, respectively. Figs. 10 and 11 show the *OBIRCH* images of the GGNMOS/GDPMOS with the total dimension of 600 μm/1.5 μm after the 50-V HBM ESD test and the corresponding layout figures. The failure mechanism can be regarded as the overheating effect inducing junction burnout after junction breakdown. Because the I-V curves did not show snapback behavior, the voltage drop of the device after junction breakdown is high enough. In addition, the current after junction breakdown is also high enough, so the large power (P=I × V) will induce the overheating effect. The failure site on the GGNMOS is located between the drain and the guard ring. The failure site on the GDPMOS is located between the drain and the source. The failure sites are both located at the edge of the finger, which can be ascribed to the maximum electric field concentrated at the edge of the finger. Because the electric field in the junction corner is higher than that in the junction plane, the edge of the finger is more vulnerable during ESD conditions. Since these two failure sites are located in only a small region of a finger, the miscorrelation between the total width of the device and the ESD robustness under the breakdown mode can be reasonably explained.

The HBM levels of the N+/PW diode and the P+/NW diode under the breakdown mode are 60 V and 80 V, respectively. Figs. 12–13 show the *OBIRCH* images and the corresponding layout figures of the N+/PW diode and the P+/NW diode, which are drawn with the finger length of

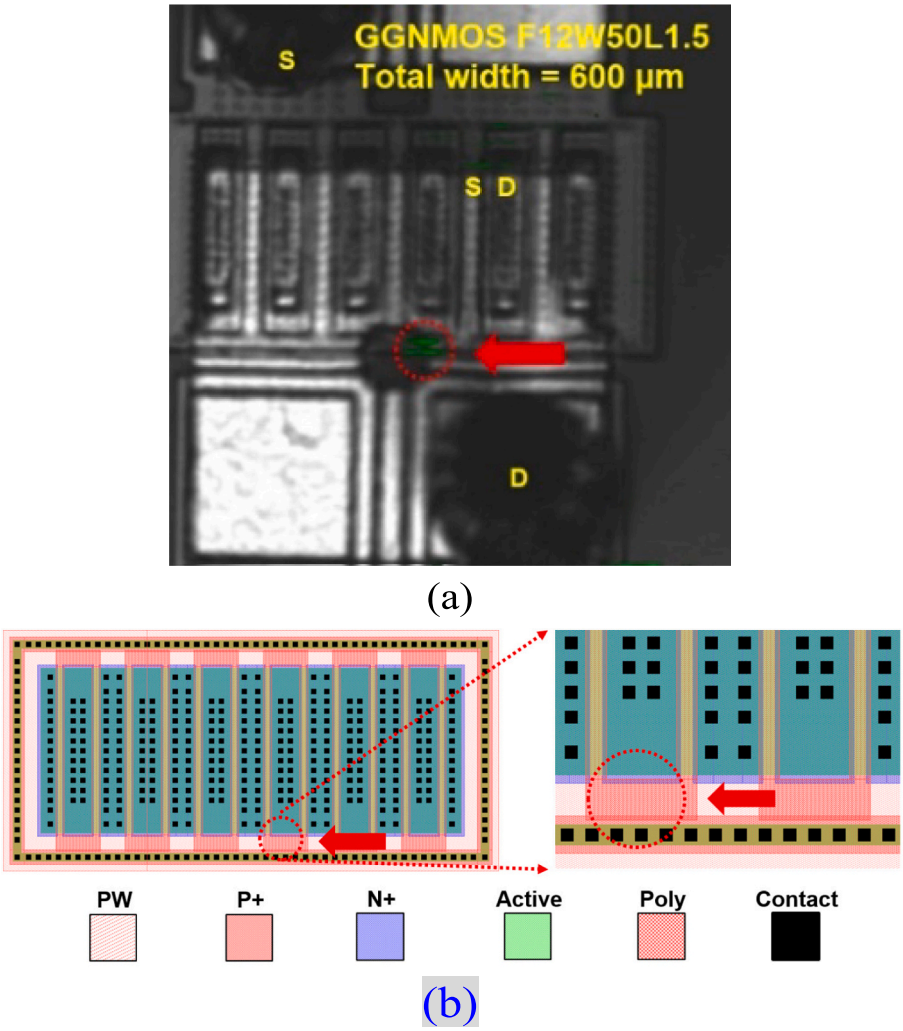


Fig. 10. (a) The *OBIRCH* images of the GGNMOS after the 50-V HBM ESD test under the breakdown mode. (b) The corresponding layout figure of the GGNMOS, where the red arrow indicated the failure location. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

35 μm, the finger number of 10, and the total perimeter of 800 μm. The failure mechanism can be also regarded as the overheating effect inducing junction burnout after junction breakdown. The failure site on the N+/PW diode is located at a small region of the N+/PW junction near the bottom of the finger. The failure site on the P+/NW diode is also located at a small region of the P+/NW junction near the top of the finger. The failed N+/PW diode of a smaller perimeter (with the finger number of 5) was also analyzed by *OBIRCH*. The failure site of the smaller device was also found at a small region of the N+/PW junction near the bottom of the finger, as shown in Fig. 14. Thus, it is obvious that the failure sites are all located at the edge of the finger, which can be also ascribed to the maximum electric field concentrated at the edge of the finger. Similar to the reason discussed above, the edge of the finger near the junction corner with a higher electric field makes it more vulnerable during ESD conditions. As a result, this evidence indicated no correlation between the diode junction perimeter and ESD robustness under the breakdown mode. Hence, for implementing the effective ESD protection design, it is strongly recommended to use the forward mode of these four ESD devices instead of the breakdown mode.

4.2. Figure of merit (FoM)

In order to further compare the area efficiency among these four ESD devices under the forward mode, the figure of merit (FoM) is proposed to evaluate the efficiency. The definition of the FoM in this work is the HBM level divided by the device area. Table 1 summarizes the HBM level, the device area, and the FoM of the four devices, and the bar chart of the FoM is shown in Fig. 15.

It can be observed that the FoM of the P+/NW diode is higher than that of the GDPMOS, and the FoM of the N+/PW diode is higher than that of the GGNMOS. This phenomenon can be attributed to the junction perimeter. For the GGNMOS and GDPMOS, the junction of the body diode is surrounded by the body pick-up ring. However, for the N+/PW diode and the P+/NW diode, the junction of the diode exists in each finger. Hence, the junction perimeter in the diode-based ESD device is inherently larger than that in the MOS-based ESD device. Therefore, the diode-based ESD device has a better FoM.

Moreover, the FoM of the P+/NW diode is the highest among these four ESD devices. It is recommended to use the N+/PW diode and the P+/NW diode to design the whole-chip ESD protection. In addition, it is necessary to conduct the ESD current through the diode under the forward mode instead of the breakdown mode. In order to guarantee such a forward-mode operation during ESD stress, the power-rail ESD clamp circuit should be built into the chip together, which will be discussed in the next subsection.

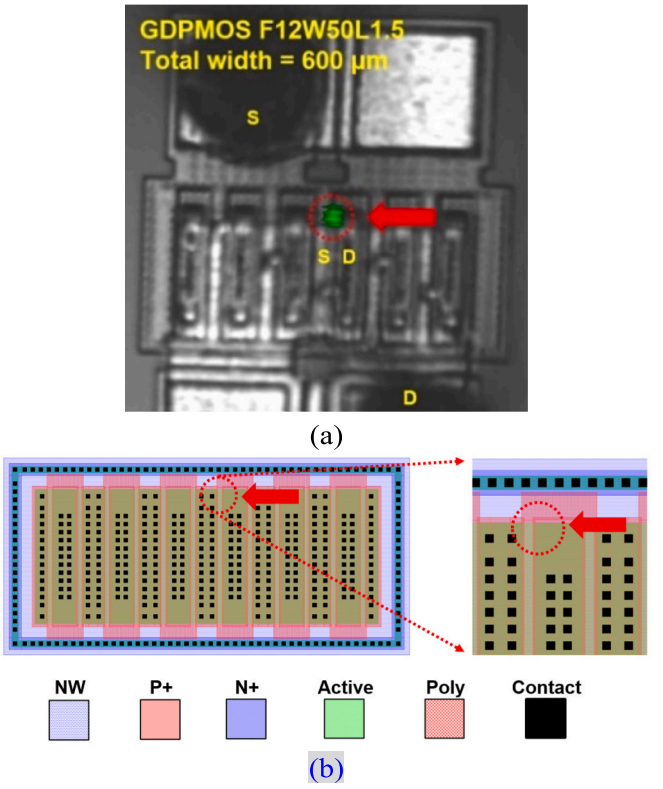


Fig. 11. (a) The *OBIRCH* images of the GDPMOS after the 50-V HBM ESD test under the breakdown mode. (b) The corresponding layout figure of the GDPMOS, where the red arrow indicated the failure location. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

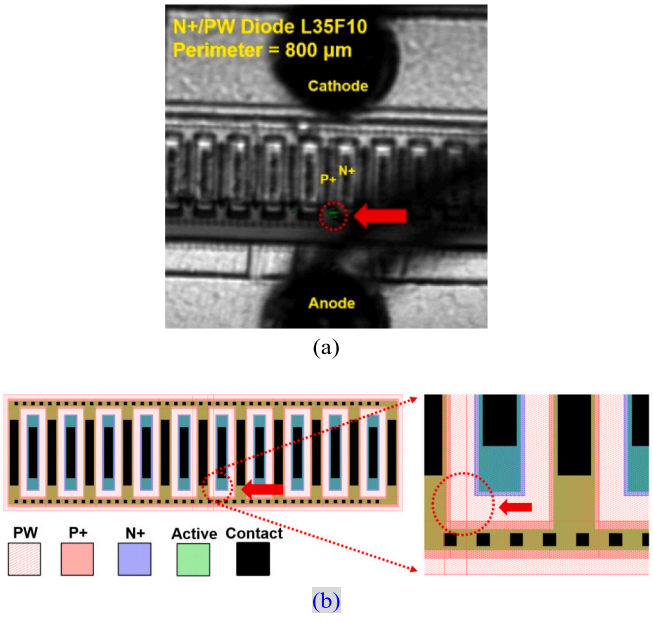


Fig. 12. (a) The *OBIRCH* images of the N+/PW diode with ten fingers after the HBM ESD test under the breakdown mode. (b) The corresponding layout figure of the N+/PW diode, where the red arrow indicated the failure location. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

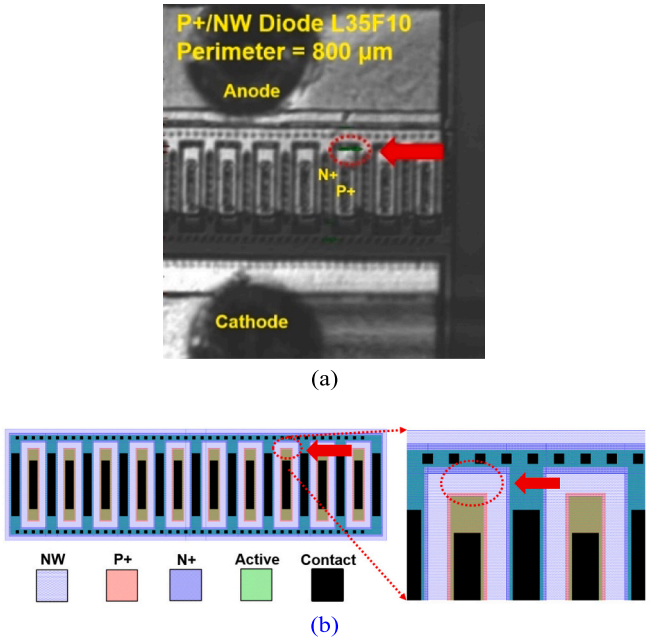
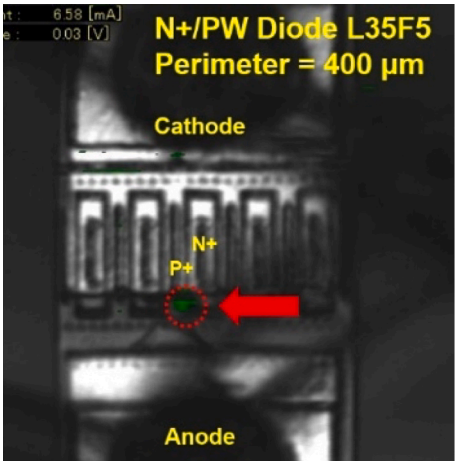


Fig. 13. (a) The *OBIRCH* images of the P+/NW diode with ten fingers after the HBM ESD test under the breakdown mode. (b) The corresponding layout figure of the P+/NW diode, where the red arrow indicated the failure location. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

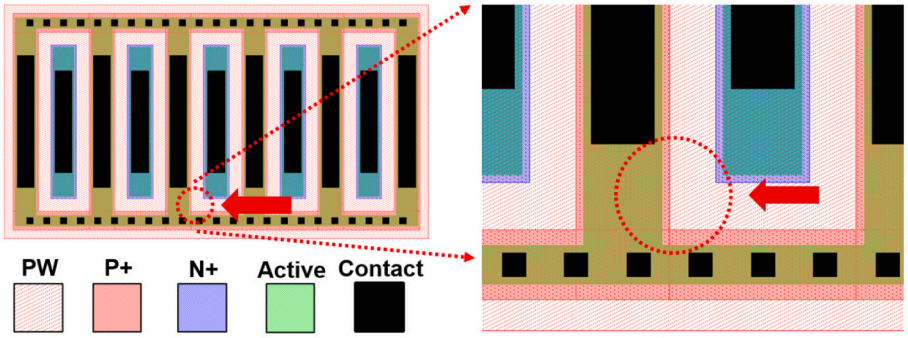
4.3. Whole-Chip ESD protection design

The concept of whole-chip ESD protection in the Si-based process had been reported [10]. However, there was no study correlated to the SiC-based process. Based on the aforementioned experimental results, the ESD protection of the input pin can be implemented with the N+/PW diode and the P+/NW diode. To discharge the ESD current through the forward mode of the diodes, the power-rail ESD clamp is an indispensable component. The power-rail ESD clamp circuit must be placed between V_{DD} and V_{SS}, so the ESD current can be conducted through the forward mode of the diodes to guarantee a high enough ESD robustness. The schematic diagrams of the SiC-based power IC with whole-chip ESD protection design under the PS mode (positive ESD voltage zapping from input to V_{SS}) and the ND mode (negative ESD voltage zapping from input to V_{DD}) of ESD events are indicated in Fig. 16(a) and (b), respectively. These two conditions are the most critical in the ESD events when ESD zaps on the input pin. Concerning the PS mode shown in Fig. 16(a), when the positive ESD stress zaps onto the input pin with the V_{SS} pin grounded, the ESD current will be first conducted to the power line (V_{DD}) through the P+/NW diode under the forward mode. Then, it will be conducted to the grounded line (V_{SS}) through the power-rail ESD clamp. Concerning the ND mode shown in Fig. 16(b), the negative ESD stress zaps onto the input pin with the V_{DD} pin grounded, which can be considered as the positive ESD stress zapping onto the V_{DD} pin with the input pin grounded. Hence, the ESD current will be first conducted from the power line (V_{DD}) to the grounded line (V_{SS}) through the power-rail ESD clamp. Then, it will be conducted to the input pin through the N+/PW diode under the forward mode. With the help of the power-rail ESD clamp circuit, ESD currents during these two HBM ESD zapping modes can be conducted by the diodes in the forward-mode operation. Therefore, the requested high ESD level of some specified SiC-based ICs can be successfully achieved.

Furthermore, the SiC power MOSFET was often drawn with larger device dimensions to provide large enough current for high-power applications. The typical device structure for high-voltage SiC power MOSFET, the vertical double-implanted MOSFET (VDMOSFET), is



(a)



(b)

Fig. 14. (a) The *OBIRCH* images of the N+/PW diode with five fingers after the HBM ESD test under the breakdown mode. (b) The corresponding layout figure of the N+/PW diode, where the red arrow indicated the failure location. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

Table 1
Summarization of the HBM Level under the Forward Mode, the Device Area, and the FoM of the Four Devices.

Device	HBM Level (V)	Device Area (μm^2)	FoM HBM Level/Device Area (V/μm^2)
GGNMOS	575	10,508	0.055
GDPMOS	1725	11,023	0.156
N+/PW Diode	625	9486	0.066
P+/NW Diode	5775	10,450	0.553

shown in Fig. 17. The test results of ESD robustness on such a standalone VDMOSFET under different stress modes are shown in Fig. 18, whereas the total channel width of the standalone SiC VDMOSFET is 193,432 μm. The DS mode represents the ESD pulse zapping onto the drain side with the source side grounded, and the HBM ESD level under DS mode can be over 8 kV. The robust self-protection capability of the VDMOSFET can be achieved when its total width is large enough. Hence, it was unnecessary to implement additional ESD protection on the drain pin of the VDMOSFET. However, the ESD level under GS mode (gate to source) ESD stress was very low (~225 V). Hence, the ESD protection between the gate and the source must be developed when the stand-alone VDMOSFET is used. However, if the corresponding gate driver circuit and VDMOSFET are integrated together into the same monolithic chip, the gate of the VDMOSFET will not be directly connected to the bond pad. There will be no ESD risk for the gate of the VDMOSFET in such a monolithic chip, and the whole monolithic chip with SiC VDMOSFET can also be enhanced to a high enough ESD robustness.

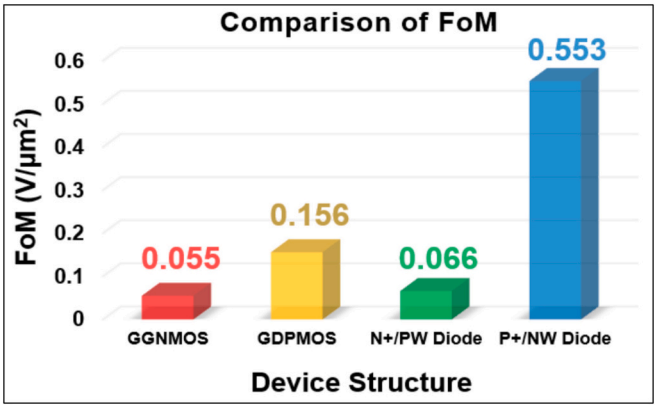


Fig. 15. The bar chart of the FoM among four ESD devices in SiC process.

5. Conclusions

The robustness of four ESD devices fabricated in a SiC process has been investigated. For the GGNMOS and the GDPMOS, under the breakdown mode, the experimental results show no correlation between

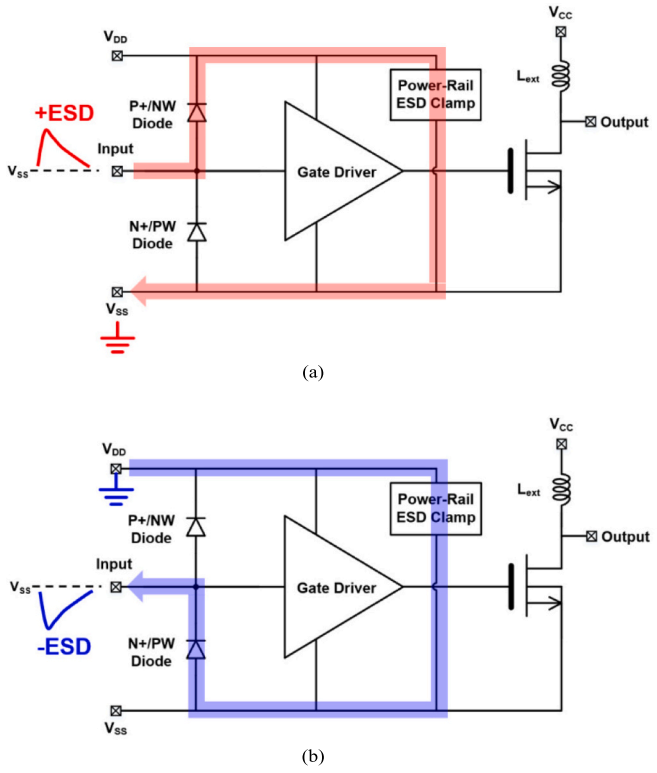


Fig. 16. The schematic diagram of the SiC-based power IC with the design of whole-chip ESD protection under the ESD zapping condition of (a) PS mode and (b) ND mode, respectively.

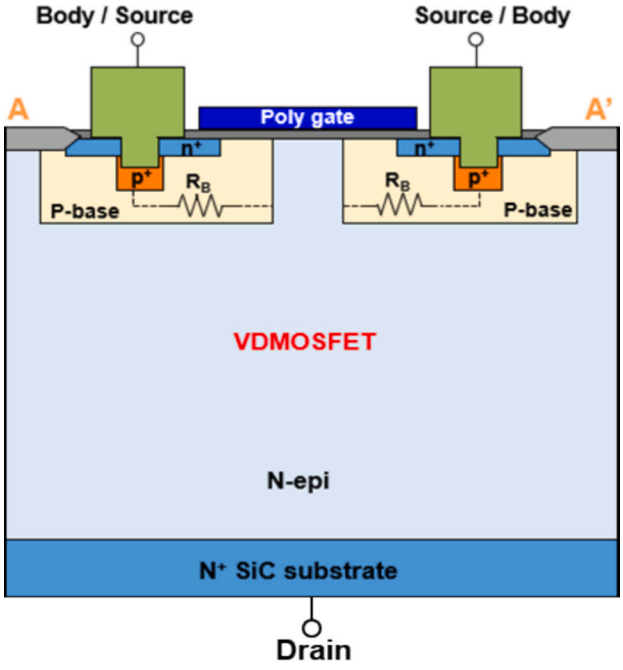


Fig. 17. The cross-sectional view of a high-voltage SiC VDMOSFET.

the ESD robustness and the number of fingers. However, under the forward mode, the ESD robustness can be effectively enhanced by increasing the number of fingers. Similarly, for the N+/PW diode and the P+/NW diode, under the breakdown mode, the experimental results show that there is no correlation between the ESD robustness and the perimeter of the device. However, under the forward mode, the ESD robustness can be effectively enhanced by increasing the perimeter of the device. Because the FoM of diodes is higher than that of MOS-based ESD devices, it is recommended to use the diodes for ESD protection design. Moreover, to conduct ESD current through the diode under forward mode, the power-rail ESD clamp circuit must be added to achieve whole-chip ESD protection for SiC-based ICs. Therefore, the power-rail ESD clamp circuit in the SiC process should be developed in the near future.

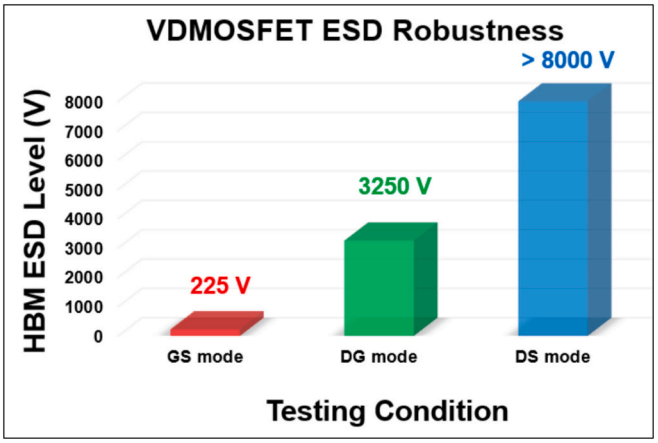


Fig. 18. The ESD robustness of a standalone SiC VDMOSFET with a total channel width of 193,432 μm.

CRediT authorship contribution statement

Chao-Yang Ke: Methodology, Validation, Data analysis, Writing–original draft. **Ming-Dou Ker**: Supervision, Writing – review & editing, Resources.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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Data availability

Data will be made available on request.

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