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Real-Time ESD Monitoring and Control in Semiconductor Manufacturing Environments With Silicon Chip of ESD Event Detection

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ABSTRACT Integrated circuits are susceptible to electrostatic discharge (ESD) events. Real-time detection and alerting of ESD events in semiconductor manufacturing environments is the key to achieving well ESD control. Additionally, the magnitude and duration of an ESD event are strongly correlated with the specific type of ESD events. The development of a novel ESD event detector, integrated on a single chip and featuring a logarithmic amplifier, a magnitude discriminator, and a time discriminator, has been motivated by this. This detector has been designed and fabricated in a 0.18-μm CMOS process. The magnitude of the ESD event can be detected and converted to 5-bit digital output codes, whereas the time duration of the ESD event can be converted to 3-bit digital output codes by the newly developed ESD event detector. It has been proven in field applications that the detected ESD events can be successfully transmitted to the ESD control center through the RF Wi-Fi module, enabling real-time ESD monitoring and control in manufacturing environments.

INDEX TERMS Charge-device model (CDM), electrostatic discharge control, electrostatic discharge (ESD), ESD event detector, magnitude discriminator, successive detection logarithmic amplifier (SDLA), time discriminator.

I. INTRODUCTION

Circuit performance is enhanced by the progress of semiconductor technology by employing scaled-down transistors. However, electrostatic discharge (ESD) damage and associated reliability issues often result in severe yield loss to IC products [1], [2]. Traditional ESD protection circuits operate passively, safeguarding internal circuits by overdesigning ESD cells to withstand potential ESD events [3]. However, if the production processes are safer, the required ESD tolerance can be lowered, reducing the area cost of ESD protection cells.

An active, real-time ESD monitoring detector for semiconductor manufacturing environments is proposed in this paper. ESD events are identified by the detector as they occur, warning messages are sent to the control center, and real-time production process safety is ensured. Compared to the traditional approach of completing IC mass production followed by individual testing, production halts immediately upon detecting an ESD event, which is allowed by this system. Only the most recently produced ICs need inspection, which is ensured by this active monitoring method. Labor efforts are minimized, and yield is improved by preventing further defective outputs. The critical importance of real-time ESD monitoring interconnected through Internet of Things (IoT) in modern manufacturing settings, including smart manufacturing and industry-4.0 is emphasized [4]. Additionally, valuable insights can be provided by analyzing and statistically evaluating the frequency of ESD occurrences at specific locations over time. A targeted focus on location-specific ESD mitigation methods is enabled by such analysis, leading to long-term advancements and the creation of safer environments for IC manufacturing.

Canonical ESD events have been characterized into several models, and the corresponding test standards have

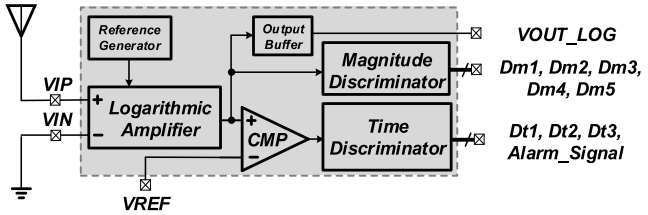


FIGURE 1. Block diagram of the new proposed ESD-event detector.

been issued, including the human-body model (HBM) [5], the charged-device model (CDM) [6], and the IEC ESD model [7]. The amplitude and duration of those ESD events are somewhat different [8], [9].

Numerous possibilities for system integration and architectural design have been unlocked by 3D integration technology [10]. However, the risk of CDM ESD during the stacking process has become a critical concern [10], [11]. Besides, ESD events are simulated using the CDM test method. It is widely regarded as more representative of real-world occurrences in production environments, such as die peeling, package assembly, IC function testing, and other back-end processes [12], [13], [14], [15]. Failure to address CDM-related issues may lead to substantial yield loss, making the control and elimination of CDM ESD hazards essential in IC manufacturing.

After identifying the ESD events, the corresponding methods or procedures to eliminate these ESD sources vary across manufacturing facilities [16]. Therefore, detecting ESD events and determining what kind of ESD sources are essential for ESD control. Antennas are used to observe and monitor the electromagnetic waveforms generated by ESD events and their characteristics [8], [9], [17], [18]. There is a correlation between the magnitude and duration of the antenna-received ESD waveform. For example, if the magnitude is enormous, its duration will extend slightly [9]. Despite occasional extreme cases, this method proves effective in typical semiconductor manufacturing environments. Extremely high-speed ADC can also be adopted to characterize antenna-received ESD event waveform; nevertheless, power consumption and fabrication cost are considered. Therefore, the ADC-based solutions turn out to be inefficient and impractical. Therefore, this real-time ESD event detector, fabricated using a 0.18 μm CMOS process, is well-suited for mass production and can be easily deployed throughout the factory, offering power-efficient and widespread monitoring capabilities.

Recently, a single chip of ESD event detector was reported to detect ESD events [9]. In that prior work, while the occurrence of ESD events could be successfully detected, the amplitude and duration of ESD sources could not be distinguished. This information is crucial for accurately identifying ESD events [19]. A new ESD event detector to measure the amplitude and duration of antenna-received ESD events is proposed. The detected results are converted into digital output codes, which can be transmitted to the ESD control center to identify ESD sources. Different solutions are implemented to address the diverse range of ESD events encountered [16]. Consequently, various methods tailored to different ESD events can be adopted to eliminate those specific types of ESD events. The scenario of the proposed real-time ESD event detector is illustrated.

The architecture of the ESD event detector is first briefly discussed in this work. Then, each functional block is measured and verified. Finally, this chip is used in field applications, detecting real-world ESD events, including IEC, HBM, and CDM ESD events.

II. CIRCUIT DESIGN OF NEW ESD EVENT DETECTOR

The block diagram of the newly proposed ESD event detector is shown in Fig. 1, including the main circuit blocks of the reference generator, logarithmic amplifier, output buffer, comparator (CMP), magnitude discriminator, and time discriminator.

Three input pins, V_{IP}, V_{IN}, and V_{REF}, are featured by the ESD event detector. V_{IP} and V_{IN} are the positive and negative inputs of the logarithmic amplifier in the ESD event detector, respectively. V_{REF} is the external reference voltage for the time discriminator. There are four output ports, which are V_{OUT_LOG}, *Dm1-Dm5*, *Dt1-Dt3*, and *Alarm_Signal*. V_{OUT_LOG} is the analog output signal of the logarithmic amplifier sent out by an output buffer for experimental observation. The analog output of the logarithmic amplifier is sent to the magnitude discriminator, which is converted to the five thermometer codes *Dm1-Dm5*. Besides, the output of the logarithmic amplifier is directed to the time discriminator via the CMP, where it is converted to the three thermometer codes *Dt1-Dt3* and an output code of *Alarm_Signal*.

A. LOGARITHMIC AMPLIFIER

The successive detection logarithmic amplifier (SDLA) used in this work is designed to operate at DC-500 MHz since the antenna-received ESD event signal is only up to about 500 MHz [9], [18], [20], [21]. Logarithmic operations are frequently employed in mathematics to compress data with a high dynamic range into a format with a lower dynamic range. Both transforming values using logarithmic functions and effectively condensing the range of values while preserving their relative proportions are involved in this process. Applications in various fields, such as signal processing, image processing, and data analysis, which aid in managing large and diverse datasets efficiently, are found by this compression technique [22], [23]. By leveraging logarithmic operations, the representation of expansive input ranges becomes more manageable and suitable for further analysis or visualization, facilitating more precise insights and more effective processing [22], [23]. The SDLA consists of six limiting amplifiers (LA) and seven full-wave rectifiers (FWR), as depicted in Fig. 2. Operating on a power supply of 1.8 V, signal processing and conditioning within specified voltage constraints are enabled by this configuration. The SDLA operates as follows: if the input signal power is small, the input signal will be amplified by all six limiting

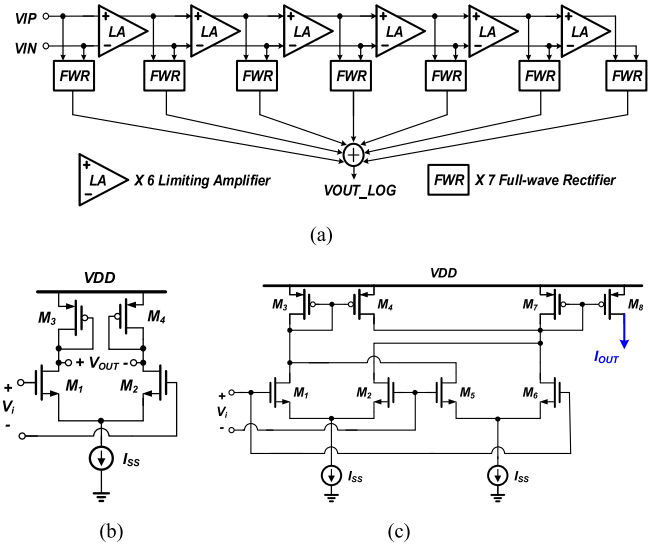


FIGURE 2. (a) Block diagram of the logarithmic amplifier, (b) circuit of limiting amplifier (LA), and (c) circuit of full-wave rectifier (FWR).

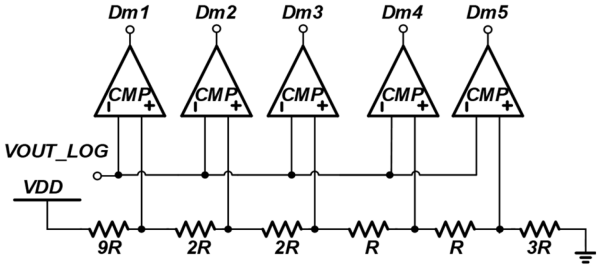


FIGURE 3. Circuit view of magnitude discriminator in the ESD event detector.

TABLE 1. Thermometer code of magnitude discriminator.

Output	(Dm1, Dm2, Dm3, Dm4, Dm5)	Log. Amp. Output Range
0	(0, 0, 0, 0, 0)	>0.9 V
1	(1, 0, 0, 0, 0)	0.9 V-0.7 V
2	(1, 1, 0, 0, 0)	0.7 V-0.5 V
3	(1, 1, 1, 0, 0)	0.5 V-0.4 V
4	(1, 1, 1, 1, 0)	0.4 V-0.3 V
5	(1, 1, 1, 1, 1)	<0.3V

amplifiers, whereas if the signal power is large, some of the stages will saturate. Hence, the input and output logarithmic correlation is maintained [20], [21]. Initially, V_{OUT_LOG} is at standby voltage without any ESD event taking place. If any ESD event is detected, V_{OUT_LOG} will be pulled down accordingly and further characterized by the following stages.

The block diagram is depicted in Fig. 2(a). The circuit schematics of the limiting amplifier and the full-wave rectifier are shown in Fig. 2(b) and 2(c). In Fig. 2(b), the limiting amplifier constructed by the M_1-M_2 differential source-coupled pair is used to effectively suppress common-mode noise from VDD since the input of SDLA is compassionate. Furthermore, high bandwidth to fulfill ESD event detection requirements is ensured by the M_3-M_4 diode-connected load with low output impedance. In Fig. 2(c), the full-wave rectifier is implemented by a dual unbalanced source-coupled pair of M_1, M_2, M_5, and M_6. Compared to a diode-based rectifier, the SDLA configuration may result in higher power consumption; However, the circuit is enabled to operate at higher frequencies and achieve a more extensive dynamic range, making it better suited for detecting ESD events.

B. MAGNITUDE DISCRIMINATOR

The schematic of the magnitude discriminator, which consists of five comparators, is shown in Fig. 3. The comparator in Fig. 3 is also demonstrated in Fig. 4. To achieve high accuracy, various internal reference voltage levels are achieved through layout-matched resistors. Besides, their power supply comes from an external voltage regulator to alleviate VDD noise and perturbation, which may cause inaccuracy during the comparison. A trade-off between resolution and speed is faced by the comparator-based magnitude discriminator [24]. However, since the primary goal of magnitude discrimination is the coarse classification of ESD events and their distances, high resolution is not critical for this application. Since there are five output codes, the magnitude V_{OUT_LOG} is categorized into six distinct categories. The corresponding output range of the logarithmic amplifier is indicated by the digital output from *Dm1* to *Dm5*, as detailed in Table 1.

C. COMPARATOR (CMP)

In the magnitude discriminator, the comparator is applied to compare V_{OUT_LOG} to internal reference voltages. Meanwhile, in the time discriminator, V_{OUT_LOG} is compared with a threshold external reference voltage (V_{REF}) by the comparator to determine whether it constitutes an ESD event. Subsequently, a pulse-shaped stimulus sent into the time discriminator is generated by this comparison.

D. TIME DISCRIMINATOR

For relative timing accuracy, edge-triggered flip-flops with large capacitance and resistance are employed to minimize capacitor mismatch and accurately record the timing of ESD events, although a trade-off between area and timing accuracy is introduced by this. The duration of the ESD events to be obtained with greater precision is enabled by this approach. To discriminate the duration of ESD events efficiently, an adjustable V_{REF} is applied to the negative pin of the comparator. Once ESD events occur, V_{OUT_LOG} is lowered to a certain level by the received signal. If V_{OUT_LOG} is higher than V_{REF}, the signal will not be recognized as an ESD event. However, if V_{OUT_LOG} falls below V_{REF}, the comparator output will go low, generating a pulse whose duration matches that of the input signal, which is then sent to the time discriminator.

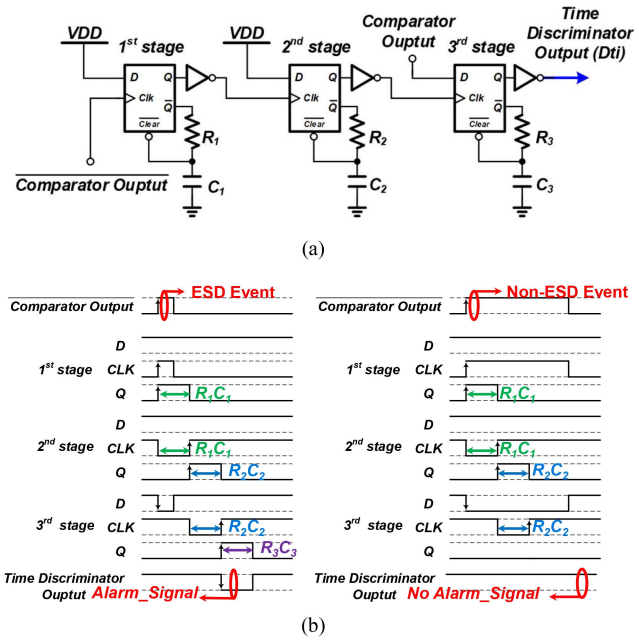


FIGURE 4. (a) Circuit view of time discriminator and (b) output waveform analysis.

The circuit view of time discriminator is shown in Fig. 4(a). Three DFFs are cascaded to output a time discriminator output code. Besides, the output waveforms of the time discriminator are demonstrated in Fig. 4(b) in detail.

Assuming the pulse-shaped stimulus with duration T, the time discriminator (Dt) output corresponds to the following equation.

$$Dt = \begin{cases} 1, T > R_1C_1 + R_2C_2 \\ 0, T < R_1C_1 + R_2C_2 \end{cases} \quad (1)$$

The received signal is ultimately classified into five categories by the time discriminator, utilizing its three output codes, *Dt1* to *Dt3* and the *Alarm_Signal*, as outlined in Table 2. Fluctuations in the absolute value of the RC time constant can be caused by process variations, leading to inconsistencies across chips. To address this issue, the external reference voltage V_{REF} can be adjusted to compensate for these variations, enabling a precise time discriminator to determine the duration of ESD events.

E. OUTPUT BUFFER

Direct observation of the analog signal output is hindered by the capacitive loading introduced by the I/O pads. Moreover, since the preceding stage (SDLA) output voltage can be as low as 0.2V to 0.3V, employing a rail-to-rail operational amplifier in a unity-gain configuration is essential to minimize loading effects.

III. SIMULATION RESULT

A fast-damping sinusoidal waveform is applied in the SPICE simulation to characterize the ESD event signal received by the antenna [9]. In Fig. 5(a), five input signals with durations of 36 ns, 87 ns, 155 ns, 320 ns, and over 450 ns are fed into the ESD event detector. The logarithmic amplifier output voltage drops accordingly. The time discriminator is activated once *VREF* is reached and discriminates the duration of the input signal. Consequently, according to Table 2, the expected outputs are generated. In addition, since the duration of the fifth input signal is more significant than 450 ns, the *Alarm_Signal* isn't activated, leading to its classification as a non-ESD event. The function of the magnitude discriminator is depicted in Fig. 5(b). V_{OUT_LOG} are measured at 966 mV, 794 mV, 558 mV, 410 mV, and 317 mV, respectively. Consequently, based on Table 1, the output of the magnitude discriminator should be "0", "1", "2", "3", and "4", as expected.

TABLE 2. Thermometer code of time discriminator.

Output	(*Dt1*, *Dt2*, *Dt3*, *Alarm_Signal*)	Duration
0	(0, 0, 0, 0)	<50 ns
1	(1, 0, 0, 0)	50 ns-100 ns
2	(1, 1, 0, 0)	100 ns-200 ns
3	(1, 1, 1, 0)	200 ns-450 ns
4*	(1, 1, 1, 1)	>450 ns

***Note:** If the output is 4, the duration of this event >450 ns will be classified as a non-ESD event. This is because canonical ESD events will not last that long in typical cases. For instance, the duration of the antenna-received CDM signal falls in the range of 50-75 ns [9].

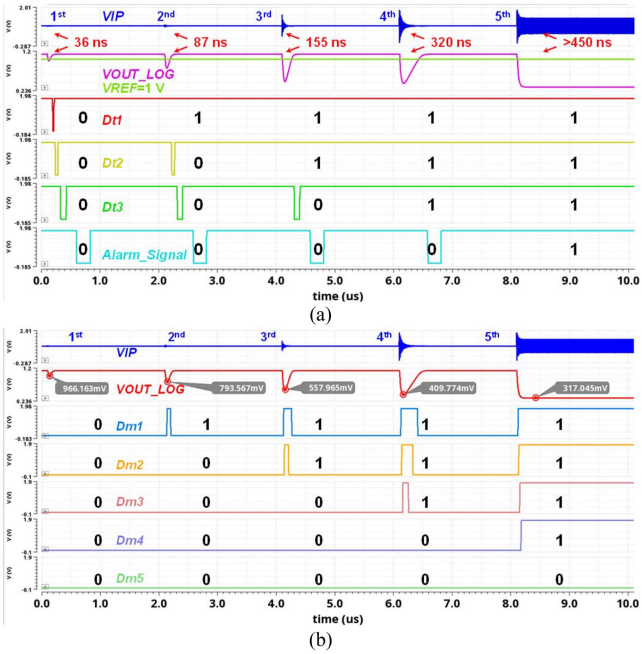


FIGURE 5. Simulation result of (a) time discriminator and (b) magnitude discriminator.

IV. MEASUREMENT ON SILICON CHIP

The newly proposed ESD event detector has been fabricated in a 0.18-μm CMOS process with a supply voltage of 1.8 V.

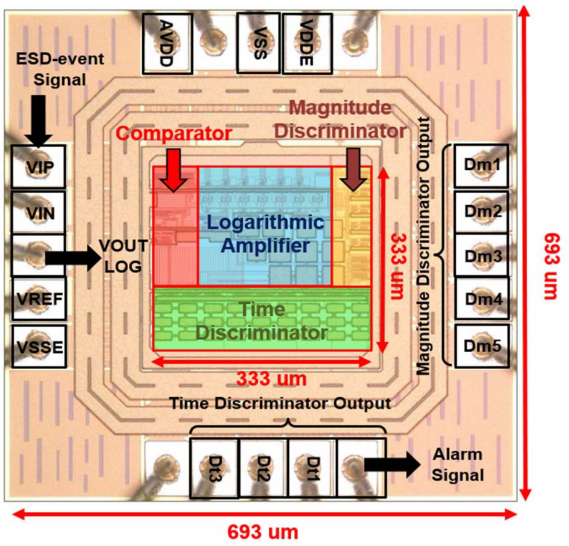


FIGURE 6. Die microphotograph of the proposed ESD event detector.

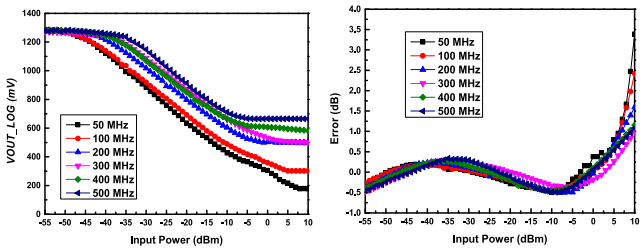


FIGURE 7. Measurement results of the logarithmic amplifier (a) responses vs. input power and (b) error vs. input power at different frequencies.

The die photograph of the fabricated chip is shown in Fig. 6 with a total die size of 693 × 693 μm^2, where the center area of 333 × 333 μm^2 is occupied by the proposed ESD event detector [25]. The efficiency and optimization achieved in the layout of the ESD event detector are underscored by this compact core circuit design.

A. LOGARITHMIC AMPLIFIER

A sinusoidal waveform with varying frequency and magnitude is generated by a signal generator. The analog output DC voltage, V_{OUT_LOG}, is governed by a logarithmic function relative to the input-output relationship. The measured input dynamic range of the logarithmic amplifier achieving less than +/- 1 dB error is from -55 to +5 dBm.

In Fig. 7(a), the input and output relationship of the logarithmic amplifier at different frequencies is depicted, while the error of the logarithmic amplifier is shown in Fig. 7(b).

B. MAGNITUDE DISCRIMINATOR

The magnitude of the signal input is indicated by the digital output *Dm1-Dm5* of the magnitude discriminator. The measurement test bench for the magnitude discriminator is

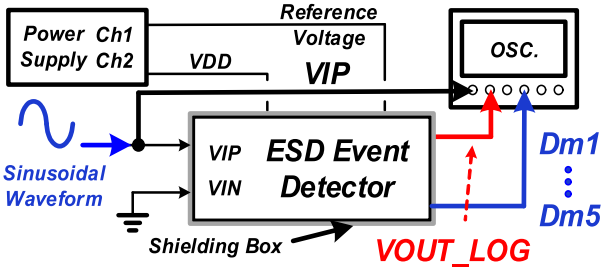


FIGURE 8. Measurement testbench for magnitude discriminator.

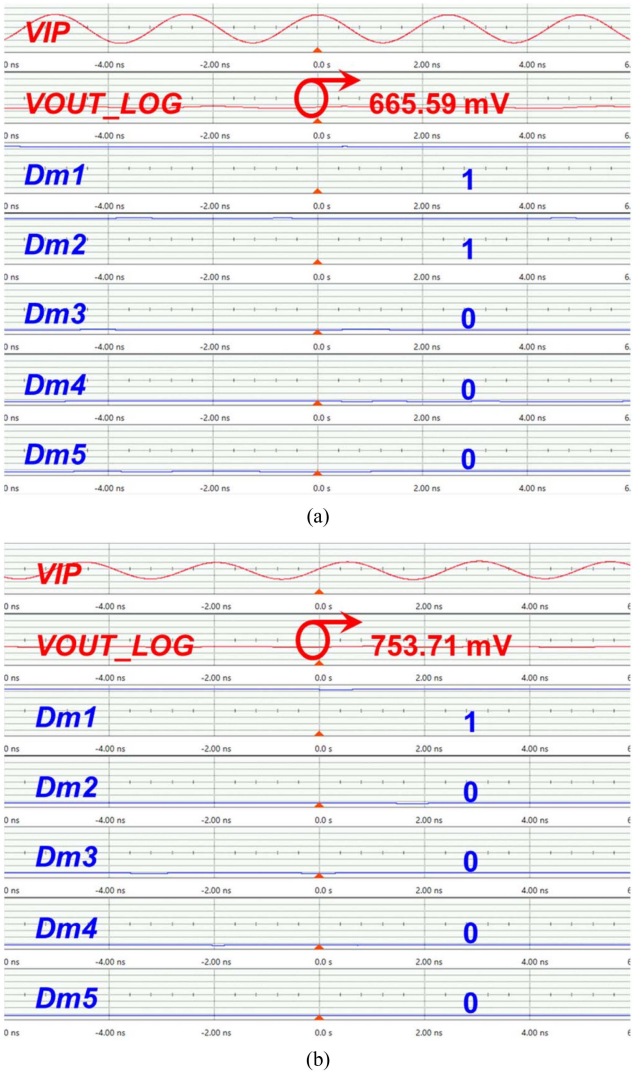


FIGURE 9. Measured results of the magnitude discriminator with (a) input power -10 dBm and (b) input power -15 dBm, under 400 MHz operating frequency.

shown in Fig. 8. The measurement results for two input patterns are revealed in Fig. 9(a) and 9(b). In Fig. 9(a) and 9(b), V_{OUT_LOG} is increased from 666 mV to 754 mV as the input power is decreased from -10 dBm to -15 dBm. Thus, the transition of *Dm2* from logic "1" to "0" occurs when the input power is decreased.

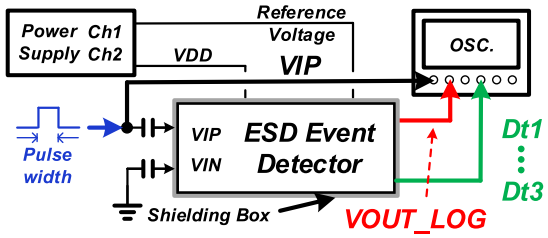


FIGURE 10. Measurement testbench for time discriminator.

C. TIME DISCRIMINATOR

The duration of the input signal is signified by the digital outputs *Dt1-Dt3* of the time discriminator and the *Alarm_Signal*. The measurement test bench is shown in Fig. 10. Examples of time discriminators are demonstrated in Fig. 11. In Fig. 11(a), (b), and (c), the duration of the input signal is 45 ns, 65 ns, and 500 ns, therefore, the time discriminator output *Dt* is "0", "1", and "4", respectively. If the duration of the input signal is over 450 ns, a zero pulse to identify this ESD event will also be delivered by the *Alarm_Signal*. The measured results of the time discriminator output on the input pulse duration are summarized in Fig. 12.

D. SUMMARY OF MEASUREMENT RESULTS

ESD events can be identified, and their magnitude and duration can be distinguished by the newly proposed ESD event detector. An integrated circuits system-on-chip (SoC) solution is preferable for real-time ESD monitoring devices, especially when they are well-distributed throughout the factory. Efficient performance, seamless integration, and scalability across the monitoring network are ensured by this approach.

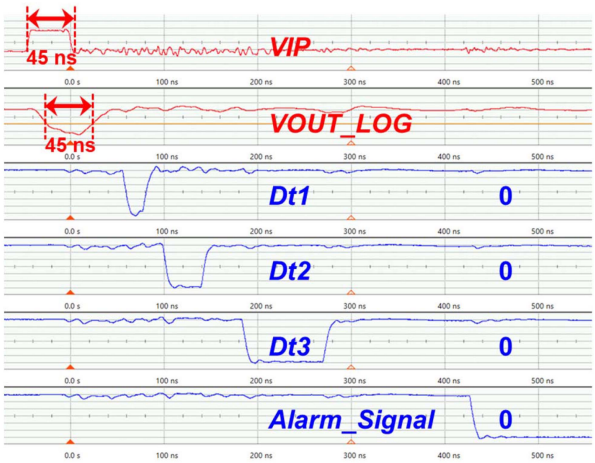
The performance of the SoC can be degraded due to variations in the manufacturing process and temperature fluctuations, which may impact the accuracy and reliability of the real-time ESD monitoring system. Compared to the prior art [9], the power consumption has been significantly reduced, and the input dynamic range has been expanded (from -55 dBm to 5 dBm) in this work. An enlarged input dynamic range ensures that minor ESD events remain "visible" within the monitoring system, enhancing its sensitivity and ability to effectively detect low-level occurrences.

The ability to characterize different types of ESD events is facilitated by the novel concept of adding magnitude and time discriminators. The detailed comparisons among prior art and other works [26], [27], [28], [29], [30] are listed in Table 3.

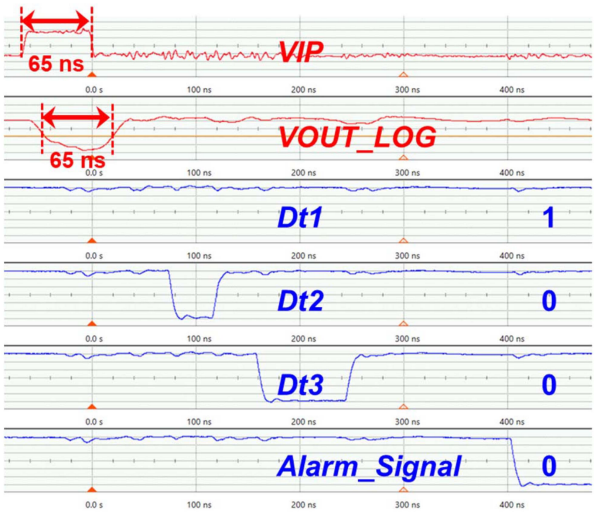
V. APPLICATION FOR ESD FIELD TEST

A. ESD GENERATOR

An ESD generator is used to simulate ESD events following the standard of IEC 61000-4-2 [7]. The measurement setup is depicted in Fig. 13. The measured waveforms are shown in Fig. 14(a) and 14(b) under ESD zapping voltage of 500 V. The input signal generated by the ESD generator exhibits characteristics of higher input power and longer duration, consistent with the findings in [9]. Ultimately, the magnitude and duration of the ESD event signal can be successfully discriminated against by the newly proposed ESD event detector, which converts them to digital output codes.



(a)



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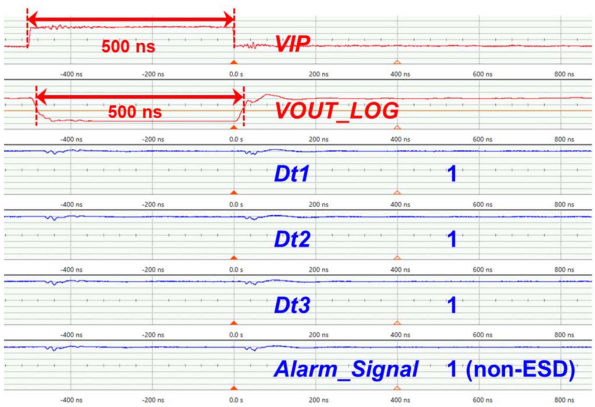


(c)

FIGURE 11. Measured results of the time discriminator with the input pulse of 60 mV, V_{REF}=0.7 V, and the pulse duration (a) 45 ns, (b) 65 ns, and (c) 500 ns.

TABLE 3. Comparison of new proposed ESD detector with other works.

	Prior Art [9]	This Work	[26]	[27], [28]	[29], [30]
Supply Voltage	1.8 V	1.8 V	N/A	9 V	9 V
Technology	TSMC 0.18 μm	TSMC 0.18 μm	N/A	N/A	N/A
System-on-a-chip (SoC)	Yes	Yes	No	No	No
Dynamic Range	-25 dBm ~ 5 dBm	-55 dBm ~ 5 dBm	N/A	N/A	N/A
Power Consumption	4.178 mW	2.58 mW	N/A	N/A	270 mW
Alarm ESD Event	Yes	Yes	Yes	Yes	Yes
Adjustable Reference	Yes	Yes	No	Yes	Yes
Time Discrimination	No	Yes	No	No	Yes
Magnitude Discrimination	No	Yes	No	Yes	No

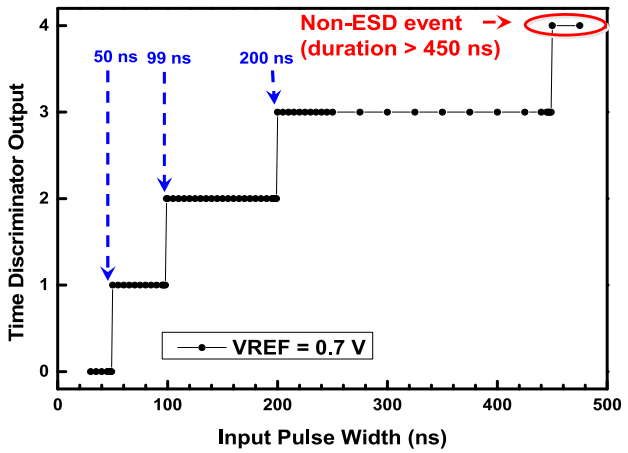


FIGURE 12. Time discriminator output vs. input pulse duration.

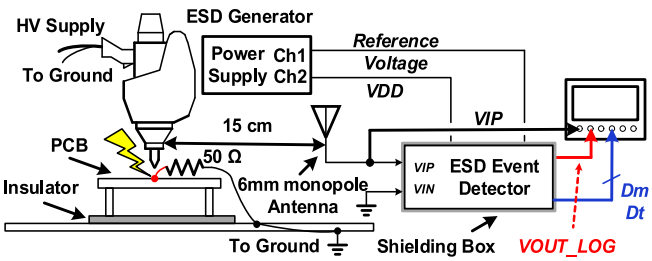


FIGURE 13. Experimental setup for ESD field test with the IEC ESD generator.

In Fig. 14(a), the duration of the input signal is 411 ns, and the output of the time discriminator is (1,1,1,0), indicating classification as an ESD event with a duration between 200 ns and 450 ns. Furthermore, in Fig. 14(b), V_{OUT_LOG} is decreased to 475.37 mV by the ESD event signal, and V_{OUT_LOG} is accurately defined within the 0.4 V to 0.5 V range by the magnitude discriminator. As the distance from the zapping point of the ESD generator to the monopole antenna increases, the ESD event signal will become smaller.

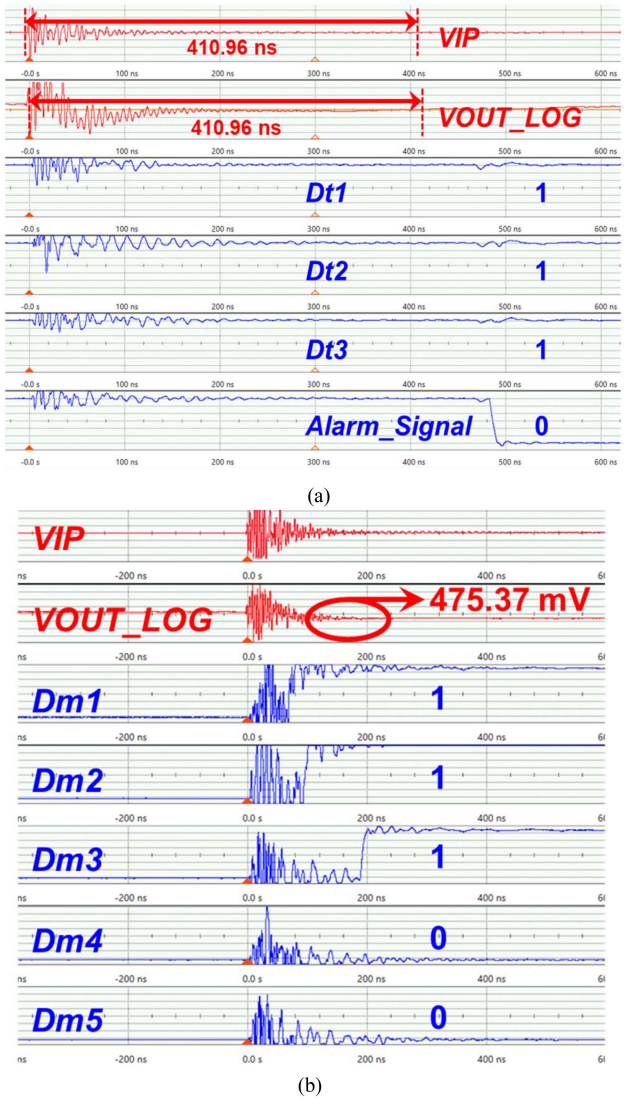


FIGURE 14. ESD field test with ESD generator of 500 V. The outputs of (a) time discriminator and (b) magnitude discriminator, with the reference voltage set at 1 V.

Consequently, the output of the magnitude discriminator will also be decreased. The relationship between the production of the magnitude discriminator and the distance from the zapping point of the ESD generator to the antenna is plotted in Fig. 15. while the ESD voltage is zapping at 1000V.

B. HBM TESTER

ESD events are generated by the HBM Tester HCE-5000 under the JS-001-2017 standard [5]. The generation and analysis of ESD events are facilitated by the measurement setup depicted in Fig. 16. Detailed waveforms corresponding to the measurements are provided in Fig. 17(a) and (b), offering insights into the characteristics and behavior of the ESD events generated by the HBM Tester.

In Fig. 17, a reference voltage of 1 V is established for comparison with the ESD event produced by the ESD generator. Furthermore, the same distance of 15 cm between the ESD event detector and the ESD zapping

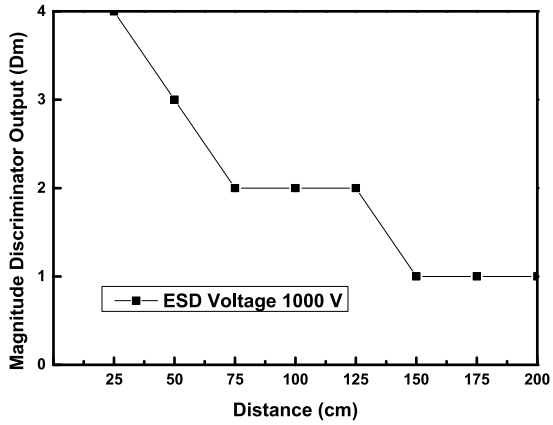


FIGURE 15. Relationship between the magnitude discriminator output and the distance from the zapping point of the ESD generator to the antenna with an ESD voltage of 1000 V.

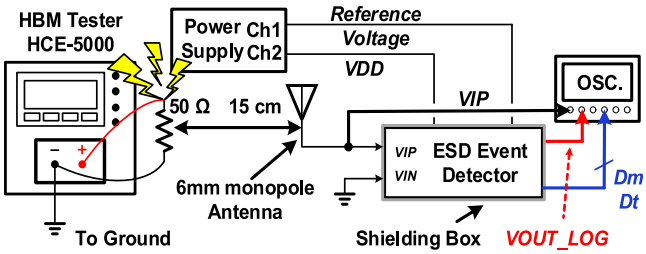


FIGURE 16. Experimental setup for ESD field test with HBM Tester HCE-5000.

point is maintained, enabling a comparative analysis of the electromagnetic waves between the ESD generator and the HBM Tester.

In Fig. 17(a), the input signal V_{IP} has a duration of 101.37 ns, and the output of the time discriminator is (1,1,0,0), classifying it as an ESD event with a duration between 100 ns and 200 ns. Additionally, in Fig. 17(b), V_{OUT_LOG} is reduced to 832.91 mV by the ESD event signal, and V_{OUT_LOG} is correctly identified within the 0.7 V to 0.9 V range by the magnitude discriminator

C. CDM ESD EVENT

CDM is a standard test method to simulate ESD events [6]. Real-world ESD occurrences in production environments, such as during die peeling, package assembly, IC function testing, and other back-end processes, are represented by CDM. Recently, a growing trend towards Multi-Chip Modules (MCMs) and Systems-in-Package (SiP) has been observed in the semiconductor industry [31]. These MCMs and SiPs integrate multiple dies, chiplets, sensors, and often fragile optoelectronic components, which usually have limited protection against ESD events [31]. During the assembly of MCMs, components are vulnerable to ESD stress due to handling. Therefore, ignoring CDM-related issues can result in significant yield loss. Thus, minimizing, controlling, and eliminating CDM ESD hazards is crucial in semiconductor manufacturing environments [31].

The test setup for CDM ESD is illustrated in Fig. 18, and its schematic is shown in Fig. 19. In Fig. 18, the newly

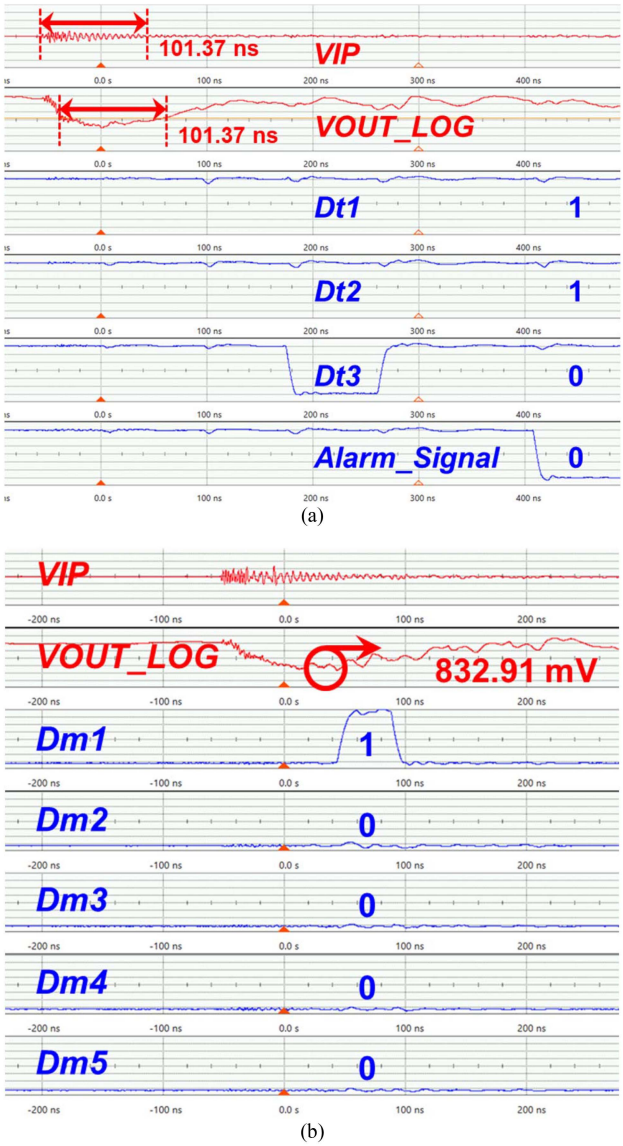


FIGURE 17. ESD field test with HBM Tester HCE-5000 of 500 V. The outputs of (a) time discriminator and (b) magnitude discriminator, with the reference voltage set at 1 V.

proposed prototype of the ESD event detector is represented by the blue circle, and the CDM Tester Onion3 is depicted by the red circle.

The measured waveforms are shown in Fig. 20(a) and 20(b) under CDM level 100 V. In Fig. 20(a), the duration of the input signal is 47 ns, and the output of the time discriminator is (0,0,0,0), indicating classification as an ESD event with a duration of less than 50 ns. Furthermore, in Fig. 20(b), V_{OUT_LOG} is decreased to 800 mV by the ESD event signal, and V_{OUT_LOG} is accurately defined within the 0.9 V to 0.7 V range by the magnitude discriminator.

D. FIELD APPLICATION

An ESD event detector has been successfully integrated into a single chip to monitor ESD events in IC manufacturing environments. The outputs of this ESD event detector measured under different types of ESD events are summarized

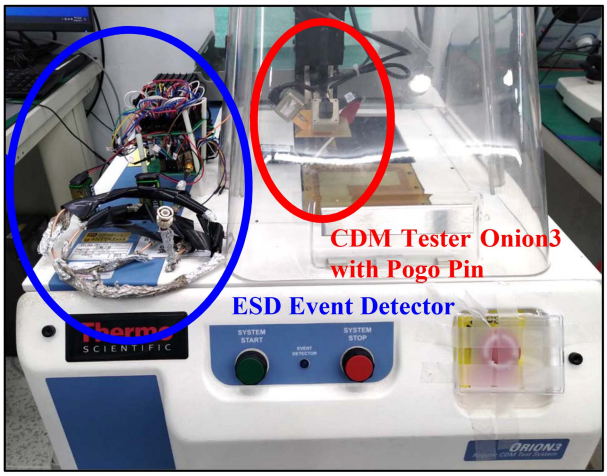


FIGURE 18. Experimental setup for ESD field test with the Onion3 CDM Tester.

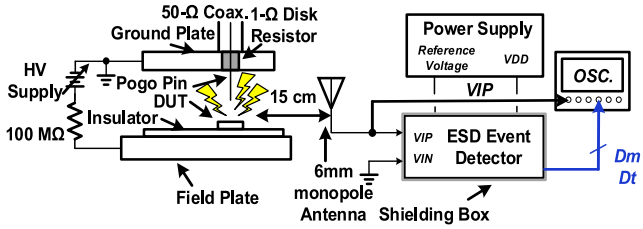
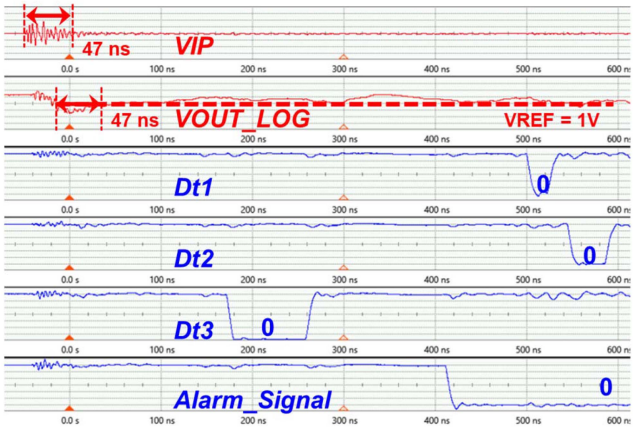


FIGURE 19. Schematic of the experimental setup for the ESD field test with the Onion3 CDM Tester with antenna 15 cm away from the Pogo pin zapping point.

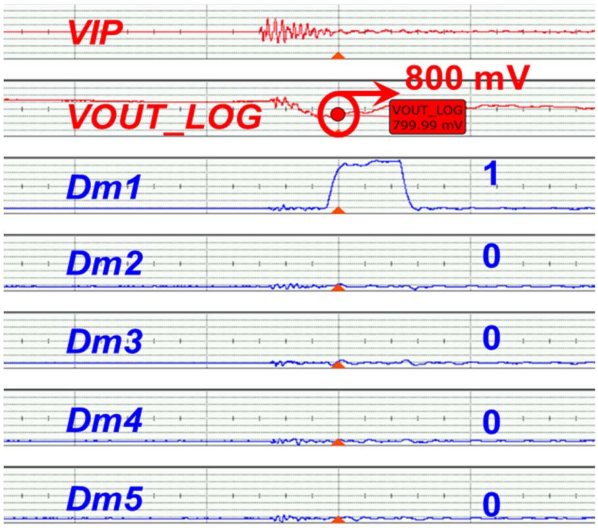
in Table 4. Real-time ESD information is uploaded to the cloud or an ESD event processing center by a simple wireless communication module, which supports IEEE 802.11b/g/n in the 2.4 GHz ISM band, enabling real-time monitoring of ESD occurrences within the IC production and assembly areas. As shown in Fig. 21, multiple ESD event detectors can be positioned around IC manufacturing and packaging equipment to form the ESD event detection system.

When an ESD event occurs, the ESD information is immediately transmitted to the control center by the ESD event detector and RF Wi-Fi module. As shown in Fig. 22, the responses of all ESD event detectors can be simultaneously monitored by the ESD detection system, providing information on the duration (*Dt*) and type of ESD events. By analyzing how the signal strength (*Dm*) received by different ESD detectors varies with distance, concentric circles can be formed to pinpoint the location of the ESD event. The origin of the ESD event is indicated by the center of the highest signal strength. The severity of the ESD event is suggested by the magnitude discriminator's maximum output. Continuous monitoring of electrostatic discharge events in IC production areas is allowed by this ESD event detection system, enhancing the safety of IC manufacturing.

The test setup for the ESD event detection system is shown in Fig. 22, where the ESD event detector is indicated by the red circle, the electrostatic gun generating the ESD events is indicated by the orange circle, and the control center



(a)



(b)

FIGURE 20. ESD field test with CDM level 100 V. The outputs of (a) time discriminator and (b) magnitude discriminator, with the reference voltage set at 1 V.

TABLE 4. Outputs of the proposed ESD event detector across various ESD event models.

Output of time discriminator (*Dt*) \ Output of magnitude discriminator (*Dm*)	0	1	2	3	4
0	CDM <50 V	CDM 50 V-200 V			
1					
2	HBM <500 V	HBM 500 V-2000 V	HBM 2000 V-3000 V		
3	ESD Gun <200 V	ESD Gun 200 V	ESD Gun 300 V	ESD Gun 300 V-500 V	
4	Non-ESD Event				

monitoring devices (computers) are indicated by the blue circle. The ESD event detector is operated with two batteries and an SMA cable as the antenna, offering a low-cost, high-functional solution.

The results wirelessly uploaded to the cloud after detecting an ESD event through Wi-Fi are shown in Fig. 23. In Google Sheets, the exact time the ESD event occurred is recorded in column A, the identification number of the ESD event detector is reported in column B, the output from

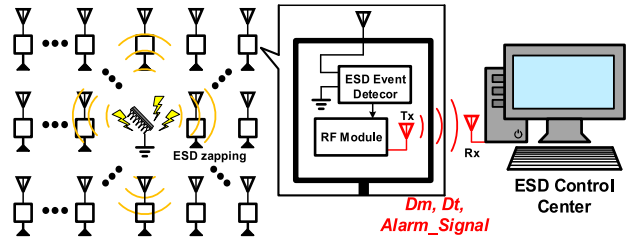


FIGURE 21. Multiple ESD event detectors can be positioned around IC manufacturing environments. Once an ESD event occurs, the RF Wi-Fi module on each ESD event uploads the information to the ESD control center.

FIGURE 22. Experimental setup for ESD event detector field application.

	A	B	C	D
1	Date and time	No. of detector	Magnitude Discriminator Ouput (Dm)	Time Discriminator Output (Dt)
2	2024-04-09 18:36:25	Detector1	2	3
3	2024-04-09 18:36:38	Detector1	4	3
4	2024-04-09 18:36:46	Detector1	2	3
5	2024-04-09 18:36:55	Detector1	2	3
6	2024-04-09 18:37:04	Detector1	4	3
7	2024-04-09 18:37:13	Detector1	5	3

FIGURE 23. Results of ESD event detection listed on Google Sheets.

the magnitude discriminator is shown in column C, and the output from the time discriminator is shown in column D. When an ESD event occurs, detailed information about the ESD event, including the exact time of occurrence and the reporting detector's ID (No. of detector), is uploaded to Google Cloud by the ESD event detector. For example, at 18:36:25, an ESD event is reported by detector 1 with *Dm* equal to "2" and *Dt* equal to "3", while at 18:36:38, another ESD event is reported by detector 1 with a larger magnitude, as its *Dm* is "4". The most significant ESD events occur at 18:37:13 because *Dm* is "5". Furthermore, in Fig. 22, the testing condition is under ESD generator zapping, so the time discriminator output *Dt* is always "3", following the result of IEC ESD in Fig. 14.

The time and location of the ESD event are defined by this information. Additionally, the ESD event's magnitude (*Dm*) and duration (*Dt*) are provided by the magnitude and time discriminators, offering more detailed insights into the ESD event.

E. ESD DETECTION PRODUCTS

Recently, numerous detection products and detection techniques have been developed to detect and alert ESD events [27], [28], [29], [30]. In [27] and [28], LED indicators are employed to classify the magnitude of ESD events, representing 10-level ESD event strength. A CDM simulator for calibration, alongside a logarithmic amplifier, high-speed comparator, and time discriminator blocks, is utilized in [29] and [30] to alarm ESD events, discriminating the ESD event from the EMI noise. In this work, the ESD event alarming capabilities are expanded to include the discrimination of magnitude and time duration. Furthermore, an adaptive ESD detection system is also proposed in this work by integrating an RF Wi-Fi module to enhance versatility and functionality on real-time ESD event monitoring. A brief summary of the comparisons among this work and the ESD detection products is shown in Table 5.

TABLE 5. Comparisons among ESD event detectors.

	This Work	[27], [28]	[29], [30]
System-on-a-chip (SoC)	Yes	No	No
Power Consumption	2.58 mW	N/A	270 mW
Alarm ESD Event	Yes	Yes	Yes
Adjustable Reference	Yes	Yes	Yes
Time Discrimination Codes	Yes 3-bit code	No	Yes*
Magnitude Discrimination Codes	Yes 5-bit code	Yes 10-bit code	No
Integrated with Wireless RF Module for Real-Time Monitoring	Yes	No	No

***Note:** Instead of real-time classification of ESD event duration, ESD events are discriminated from a given time duration by the time discriminator in [29] and [30].

VI. CONCLUSION

A novel ESD event detector with magnitude and time discriminators has been developed and fabricated in a 0.18-μm CMOS process to monitor ESD events. The amplitude of an ESD event can be detected and converted to 5-bit digital output codes, whereas the time duration of an ESD event can be converted to 3-bit digital output codes. The ESD field test proves that entirely different characteristics of ESD events can be observed through the time and magnitude discriminators. The magnitude and duration of the ESD event can be accurately identified by the ESD event detector, and the output codes are successfully transmitted to the ESD control center via the RF Wi-Fi module. ESD events can be precisely monitored by this newly developed detector, which efficiently facilitates real-time ESD control in semiconductor manufacturing environments.

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