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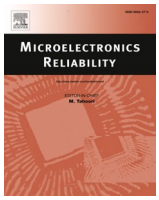

Improved device structure for electrical safe operating area in SiC 1700-V VDMOSFET

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ABSTRACT

This study provides significant advancements in SiC power device technology, improving the balance between high voltage, current handling, and reliability. The improved layout design of a SiC 1700-V vertical double-implanted MOSFET (VDMOSFET) with enhancing the characteristics of electrical safe operating (eSOA) and unclamped inductive switching (UIS) was carefully verified in this study. The experimental results show that the improved structure with an extended P+ region has a wider eSOA boundary. Furthermore, the improved structure can also tolerate higher power supply V_{CC}, higher switching current, and higher overshooting V_{DS} voltage. While the improved design sacrifices some DC performance, such as a slight increase in threshold voltage and on-resistance, it significantly boosts dynamic-switching reliability. All of the benefits can be attributed to the lower base resistance achieved by the layout design of an extended P+ region. Moreover, the experimental results from the double pulse test demonstrate that the proposed method did not compromise any switching speed or switching loss. Therefore, the improved structure without increasing manufacturing costs is recommended to enhance the robustness of dynamic switching in SiC 1700-V VDMOSFET.

1. Introduction

Because emerging high-power applications, such as electric vehicles, data centers, green-power infrastructures, and railway electric tractions, have sprung up in recent years, SiC power MOSFET has been widely developed. Among the most commercially available products of SiC power MOSFET, the vertical double-implanted MOSFET (VDMOSFET) is the most widely used structure. The VDMOSFET often operates in high-current and high-voltage operating conditions. The reliability of dynamic switching in VDMOSFET is strongly correlated to the reliability of the whole power system.

Regarding the design of the power MOSFET, a concept of the design triangle of the power MOSFET was proposed [1], which means the trade-off among safe operating area (SOA), drain-to-source breakdown voltage (BV_{DSS}), and specific on-resistance ($R_{on,sp}$), as illustrated in Fig. 1. The three key indexes are all contradictory to each other. Therefore, it is important to consider all of the key indexes when designing a power MOSFET with sufficient blocking voltage, low on-resistance, and robust reliability. This study focused on the two reliability issues of dynamic switching: the electrical safe operating area (eSOA) and the unclamped inductive switching (UIS).

The characteristics of eSOA can be measured by the transmission line pulse system (TLP) with different gate-bias conditions. Since the TLP system can generate a rapid pulse with a 10-ns rising time and a 100-ns pulse width, it is suitable for investigating the switching locus of a power device under different gate-bias conditions. Suppose the eSOA boundary of the VDMOSFET is well-verified; the designer can optimize the circuit operation to prevent the VDMOSFET from operating out of the eSOA and prevent the parasitic NPN BJT from being triggered. The UIS test can simulate the switching operation of the VDMOSFET in the power system. The international standards about UIS test have been established in *Joint Electron Device Engineering Council* (JEDEC) standard [2]. In the high-power system, because there is usually a large external inductance in series with the drain side of the VDMOSFET, the drain side is inevitable to sustain high overshooting voltage due to the large dI/dt of the inductance. If the overshooting voltage is high enough, the avalanche breakdown will occur, and the parasitic NPN BJT of the VDMOSFET will be triggered. Thus, the UIS robustness is also an essential reliability issue.

Few studies have been published so far regarding the research on eSOA of SiC-based devices [3–6]. Concerning the research of UIS test, some previous studies were conducted with SiC VDMOSFET [4,5,7–13].

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