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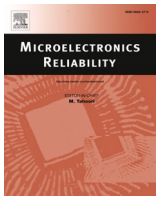

Research Paper

Gate-to-source ESD protection design for GaN-on-silicon power HEMT

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ABSTRACT

A monolithic integrated bidirectional gate-to-source ESD protection circuit for power high-electron-mobility transistor (HEMT) in GaN-on-Si process is proposed. The proposed circuit is incorporated with a voltage detection mechanism to ensure that the ESD protection circuit is selectively activated only under ESD stress conditions, thereby minimizing the unwanted interference and standby leakage current during normal device operation. It has been demonstrated that the proposed design can significantly enhance the robustness against ESD events with human-body-model (HBM) ESD level exceeding ±8 kV and IEC ESD level beyond ±2.5 kV.

1. Introduction

GaN-based power high-electron-mobility transistors (HEMTs) have attracted significant attention in high-frequency and high-power-density electronic systems due to their fast-switching speed and capability to sustain high drain-to-source voltages [1]. However, electrostatic discharge (ESD) remains a primary reliability concern, because ESD events can induce severe damage to GaN-based power HEMT. In particular, the gate terminal is highly susceptible to ESD failures. Due to the presence of back-to-back diodes in the gate structure, which cannot effectively dissipate electrostatic charges, the gate was often damaged under ESD stress [2–4]. Therefore, improving the ESD robustness of GaN-based power HEMT, especially at the gate terminal, is essential for ensuring device reliability for safe applications.

To fully turn off the GaN-based power HEMT in the field applications, the gate voltage was often biased to the negative voltage level around -5 ~ -10 V. Therefore, the gate-to-source ESD protection circuit must be designed with a bidirectional structure. Several bidirectional gate-to-source ESD protection circuits to enhance ESD robustness of GaN-based power HEMT were reported [5,6]. In Fig. 1(a), the ESD protection circuit consists of two ESD protection HEMTs ($HEMT_{ESD1}$ and $HEMT_{ESD2}$) along with two resistors (R_1 and R_2) [5]. During an ESD event, the parasitic capacitances between the gate to drain (C_{GD}, C_{GD1}, and C_{GD2}) and the gate to source (C_{GS}, C_{GS1}, and C_{GS2}) enable voltage coupling from the gates of $HEMT_{ESD1}$, $HEMT_{ESD2}$, and the protected HEMT. This coupled voltage, in conjunction with the series resistor (R_1 or R_2), generates a transient response governed by the RC time constant. As a result, the gate voltage of $HEMT_{ESD1}$ and $HEMT_{ESD2}$ increases momentarily, activating their channels to provide a temporary turn-on path to discharge ESD current [5].

In Fig. 1(b), the ESD protection circuit is implemented by using eight diode-connected HEMTs (D_1 ~ D_8), two resistors (R_1 and R_2), and a dual-gate HEMT (DG-HEMT) [6]. The operation of the circuit is controlled by two distinct triggering mechanisms: the forward trigger circuit and the reverse trigger circuit, which independently control the two gates of the DG-HEMT. The forward trigger circuit is composed of four diode-connected HEMTs (D_1 ~ D_4) and a resistor (R_1), while the reverse trigger circuit consists of the remaining four diode-connected HEMTs (D_5 ~ D_8) and a resistor (R_2). During a forward gate-to-source ESD event, a large transient voltage turns on D_1 ~ D_4, allowing current to flow through R_1. This current flow induces a voltage increase across G_1 and S_1, thereby activating the gate G_1. Simultaneously, since D_5 ~ D_8 remain in off state, the voltage difference between G_2 and S_2 remains minimal. Consequently, the upper HEMT within the DG-HEMT functions as a forward-biased diode in series with a resistor, effectively providing a turn-on path to discharge ESD current. The reverse ESD event can be discharged in the same manner [6].

In this work, a novel monolithic integrated bidirectional gate-to-source ESD protection circuit is proposed to enhance the ESD robustness of GaN-based 650-V power HEMT. The proposed circuit has been fabricated in a GaN-on-Si process, and its performance is systematically evaluated through transmission line pulse (TLP), human-body-model

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